TFP501 EEPROM Considerations

Connectivity Solutions

ABSTRACT

The user has a variety of EEPROMs to select for use with the TFP501. This report describes some considerations for selecting an EEPROM for use with the TFP501. Examination of the I2C activity of the TFP501 can provide an understanding of the power on requirements for the device in test. Comparison of EEPROM activity to known results can aid in diagnosis of board problems.

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Overview

HDCP (high-bandwidth digital content protection) keys are required for operation of a HDCP device. For the TFP501 these are stored in an external EEPROM with I2C interface. The TFP501 must load keys from the external EEPROM each time power is applied. After an internal power-on reset and short delay, the TFP501 begins to read from the EEPROM. It checks to see that the EEPROM acknowledges access, and reads a header in the first locations of the EEPROM to learn what data is stored in the EEPROM. The following sections describe considerations for selecting an EEPROM and system operation. Normal operational waveforms are shown as examples for comparison to a new application. Some other typical waveforms are shown for diagnosis of unexpected system behavior.

EEPROM Selection and Application

Size Considerations

HDCP requires a device to have a 40-bit key selection vector and 40 keys each 56 bits in length. This requires 2280 bits of data. The required indicator value and formatting requirements for the keys requires 336 bytes or 2688 bits total memory. This will typically require a 4K bit I2C EEPROM. Unused memory locations beyond these bytes do not need to be written.

The page size for write operations must accommodate 8 byte page writes. These are aligned on 8-byte boundaries by the TFP501.

Addressing

The TFP501 is always a bus master. It addresses an I2C memory device at slave address 0xA0. The TFP501 provides one address byte as a data word after the slave address. Since one byte of address only provides 256 bytes of address range, the TFP501 uses bit 1 of the slave address as a page address (see Figure 1).

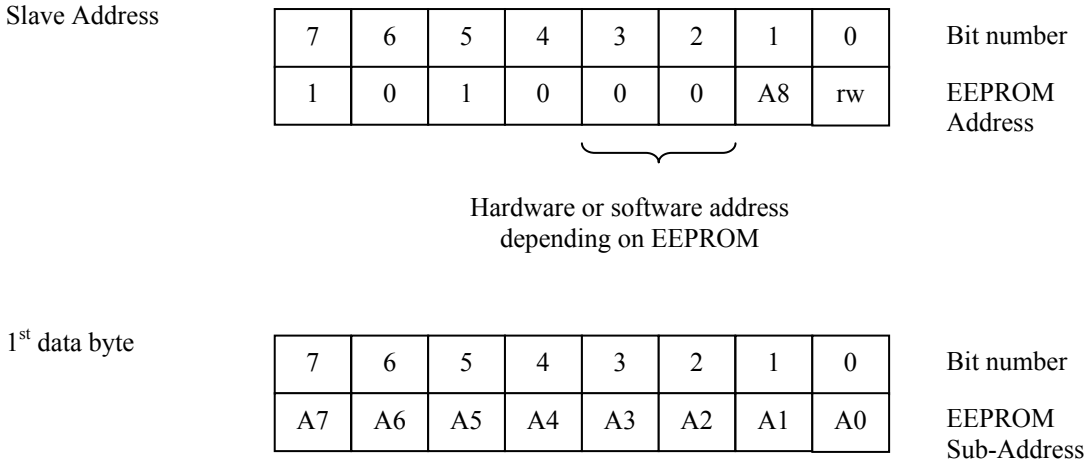

Figure 1. EEPROM Address

This addressing is compatible with I2C interface serial EEPROMs from 4K to 16K bits from several manufacturers. Typical device types are 24xx04, 24xx08, and 24xx16. Byte addresses are in the range of 0x000 to 0x14F.

Memories that require two address bytes following the slave address such as typically found on 32K-bit and larger devices do not work with the TFP501. The TFP501 provides only one address byte for the device. The large memory is expecting a second address byte and either uses a data value for the write or is reset before completing the address.

Voltage Selection

The TFP501 contains an internal reset, which operates at approximately 1.8 V. When the supply voltage rises above the reset threshold, the device begins to read from EEPROM after a short delay. It is recommended that the EEPROM and the TFP501 use the same power supply. The power supply should transition quickly to a stable level. However, since the TFP501 can begin downloading at 1.8 V, if the power rise time is delayed, a 1.8-V capable EEPROM is recommended. An alternate method of ensuring the EEPROM is functional before power is applied to the TFP501 can be used.

I2C Speed

The TFP501 operates the EEPROM I2C bus at approximately 40 kHz.

Byte Ordering

The least significant byte of a multiple byte value must be stored in the lowest memory address allocated for the multiple byte value. Refer to the memory map in the key programming document.

Write Protection

The EEPROM is a serial device with its own power-up reset controller. Write protection of the EEPROM after key encryption is recommended. Write protection may reduce the chance of an EEPROM misinterpreting normal bus activity as a write command if a system transient event should occur.

EEPROM Access and Timing

When power is applied to the TFP501 and its reset completes, the TFP501 makes two attempts to address the EEPROM at A0 with an arbitrary sub-address. If the device fails to respond, the TFP501 stops. If it detects the EEPROM, it continues to read an indicator value from the first 8 bytes of the memory. Depending on the indicator value, it stops, encrypts the EEPROM data or decrypts the data for use with HDCP processing. The TFP501 does not retry the EEPROM or the indicator value until the next power-on cycle.

Encryption

Encryption begins as soon as the appropriate indicator value is read. The data is read from the EEPROM, encrypted and written back to the EEPROM. The duration of the encryption process depends on the write time of the EEPROM selected. This typically completes in 400ms, but the user should evaluate this time in their implementation. Power should be stable during the encryption process to avoid the possibility of data errors in the EEPROM. Write protection for the EEPROM must be disabled during the encryption process. Only the 336 memory byte locations are overwritten. Write protection for the EEPROM may be re-enabled after the process completes. The encryption process does not retain the BKSV or keys for internal use, BKSV reads all 0s during and after this process.

Decryption

Decryption begins as soon as the appropriate indicator value is read. Data is read from the EEPROM and prepared for use in the device. This time varies with the I2C speed, depending on the device and operating voltage. The BKSV is not available from the TFP501 until it has been read from the EEPROM.

Sharing the EEPROM

The TFP501 expects to be the only controller on the bus and the bus to be available on request. However, it only accesses the bus during the time after power-up and leaves the bus idle when its operation is completed. Only the defined memory locations are used or altered. Although not recommended, system design may accommodate other access or use of the memory.

One access of the bus other than the TFP501 is to program the memory in circuit. Once the TFP501 has completed its operation, an external controller can take control of the bus and read or write the EEPROM. This can be useful for programming the keys, re-programming the keys, or confirmation that the encryption process has completed properly.

CAUTION:

The TFP501 should not be exposed to voltages beyond the maximum stated in the datasheet due to bus sharing or access.

Normal Operation

Keys are initially programmed into the EEPROM unencrypted with the appropriate indicator. The device recognizes the indicator value for unencrypted keys and writes encrypted keys back to the device. The time for this process varies with the device, EEPROM, and voltage, but typically completes in approximately 400 ms (see Figure 2). The test system powering the application board should provide enough time with power applied to allow this process to complete to avoid the possibility of having only a portion of the keys encrypted. As part of the encryption process, the indicator value is over written.

Note: In the waveform figures in this document, waveform 2 is Vdd, waveform 3 is PROM_SCL, waveform 4 is PROM_SDA. Unless otherwise noted, these waveforms were taken at nominal voltage and temperature on a random device sample.

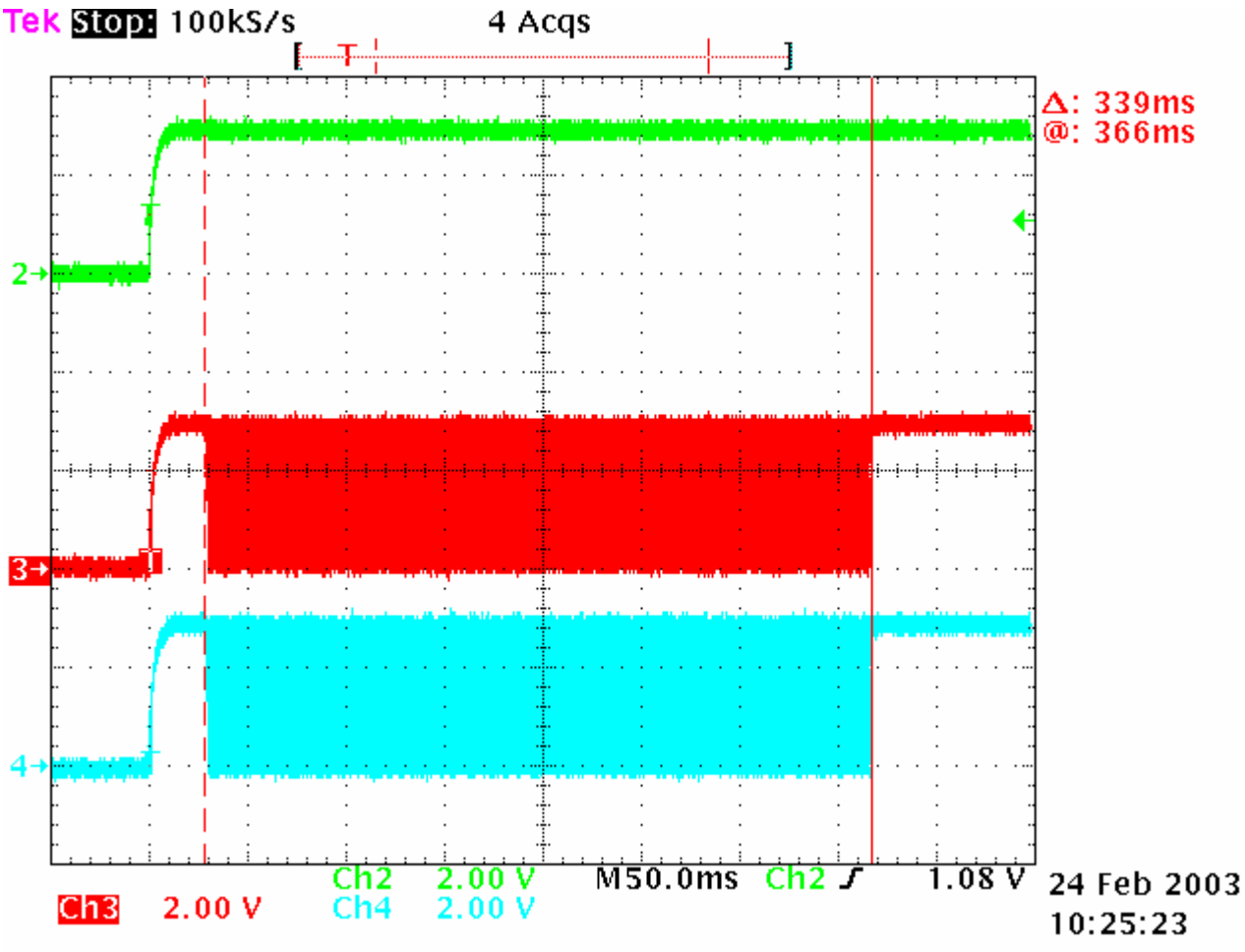

Figure 2. Typical EEPROM Programming

Once the EEPROM has been written with encrypted keys, on the next power cycle the device reads the keys, recognizes the indicator value for encrypted keys, and loads the keys for use. This process typically takes less than 150 ms (see Figure 3).

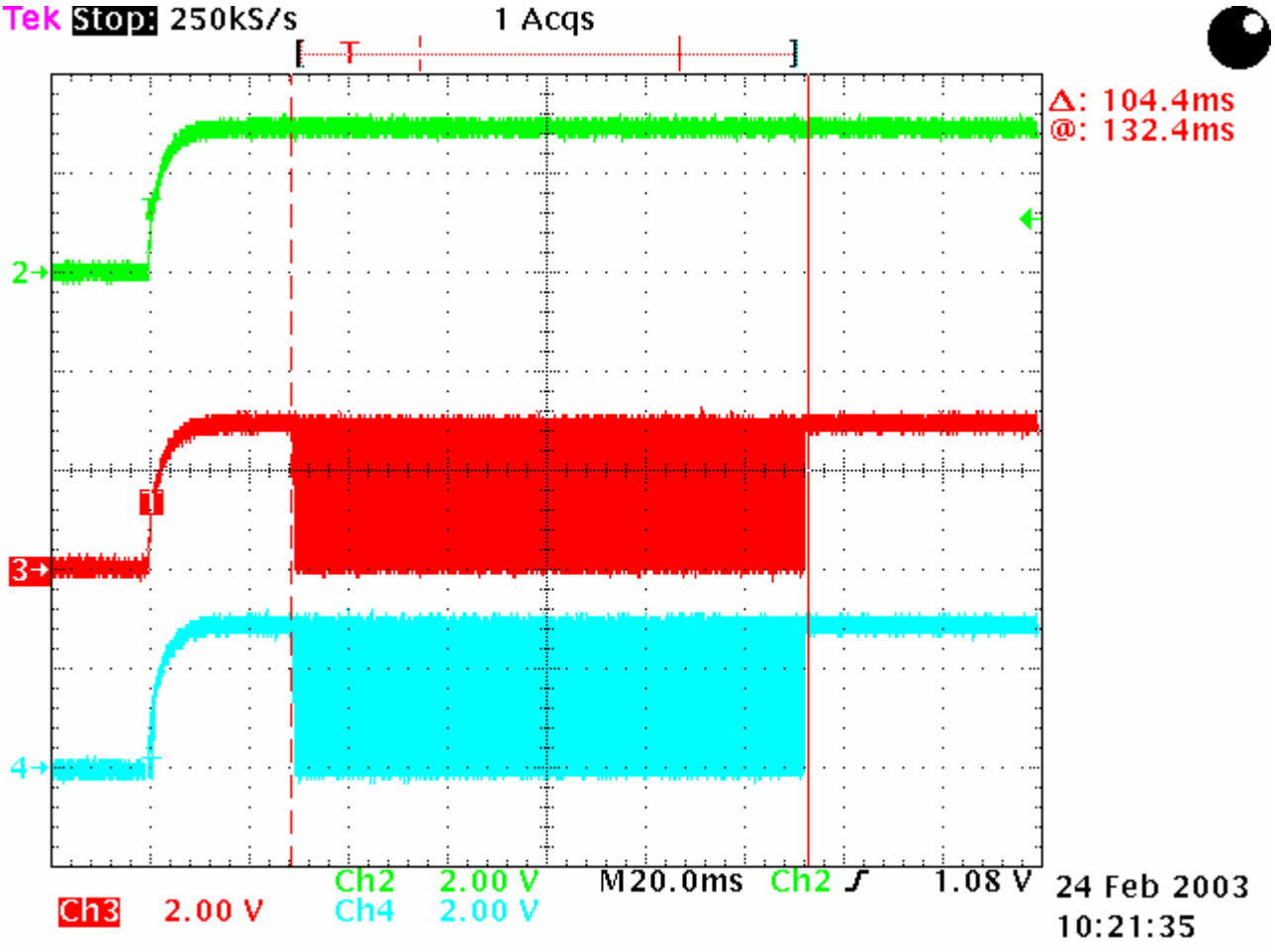

Figure 3. Typical EEPROM Read

The clock speed of the read from the TFP501 varies with device, temperature and voltage, but is approximately 40 kHz. Figure 4 shows an example clock period.

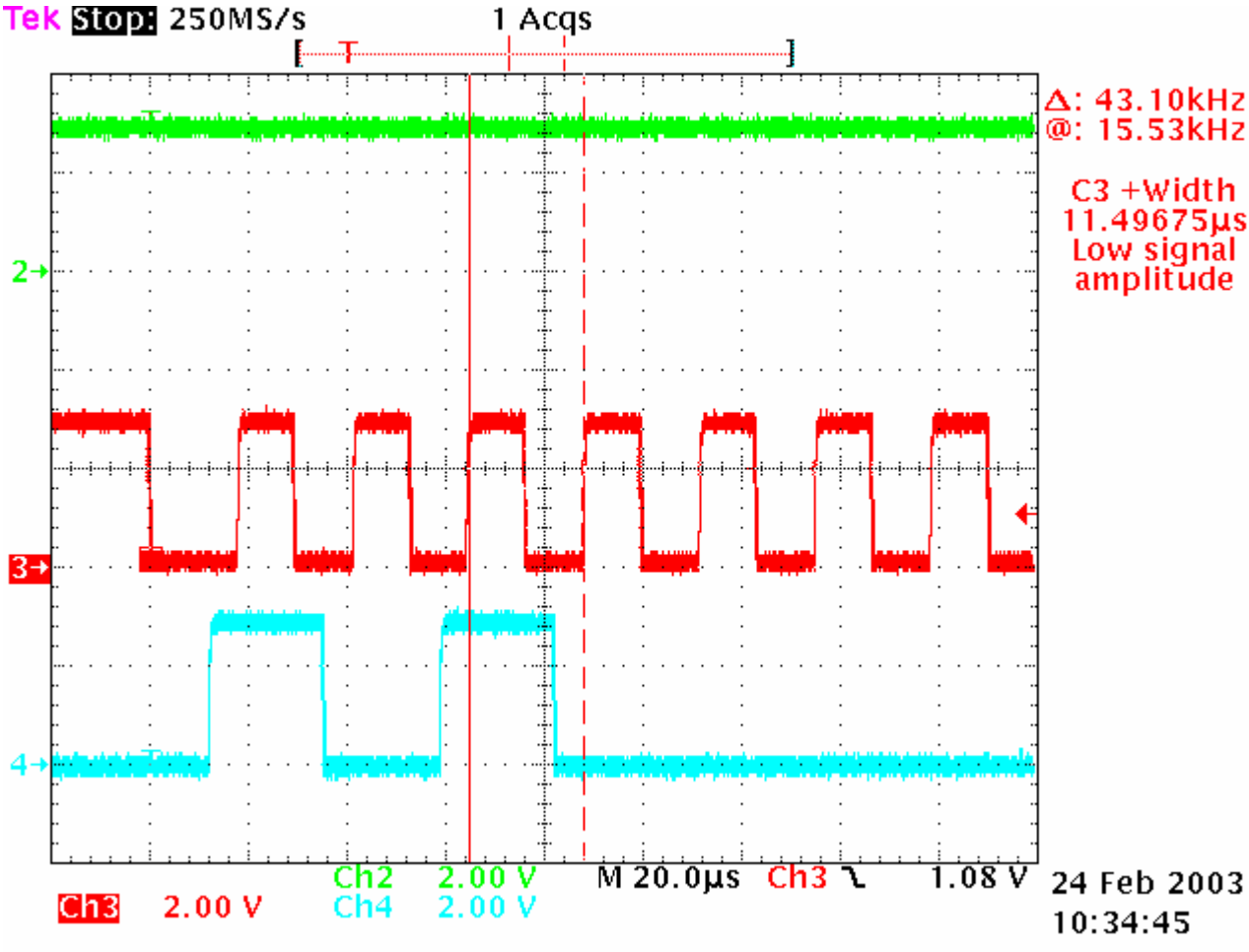

Figure 4. Example Clock Frequency

Write Protected EEPROM

When the EEPROM is write protected during the encryption process, the data can not be changed by the TFP501. Each power cycle, the TFP501 will try to write to the EEPROM. Each waveform will look much like Figure 2. The device is not able to authenticate with a HDCP transmitter since the keys are not loaded.

Other EEPROM sequences

The TFP501 initially makes two attempts to address the EEPROM with an arbitrary address. If the EEPROM does not acknowledge, activity on the EEPROM lines stops quickly. Figure 5 shows activity when no EEPROM is installed in the board. While there may be some variations in the activity, Figure 6 shows a detail where no acknowledge can be observed on the bus.

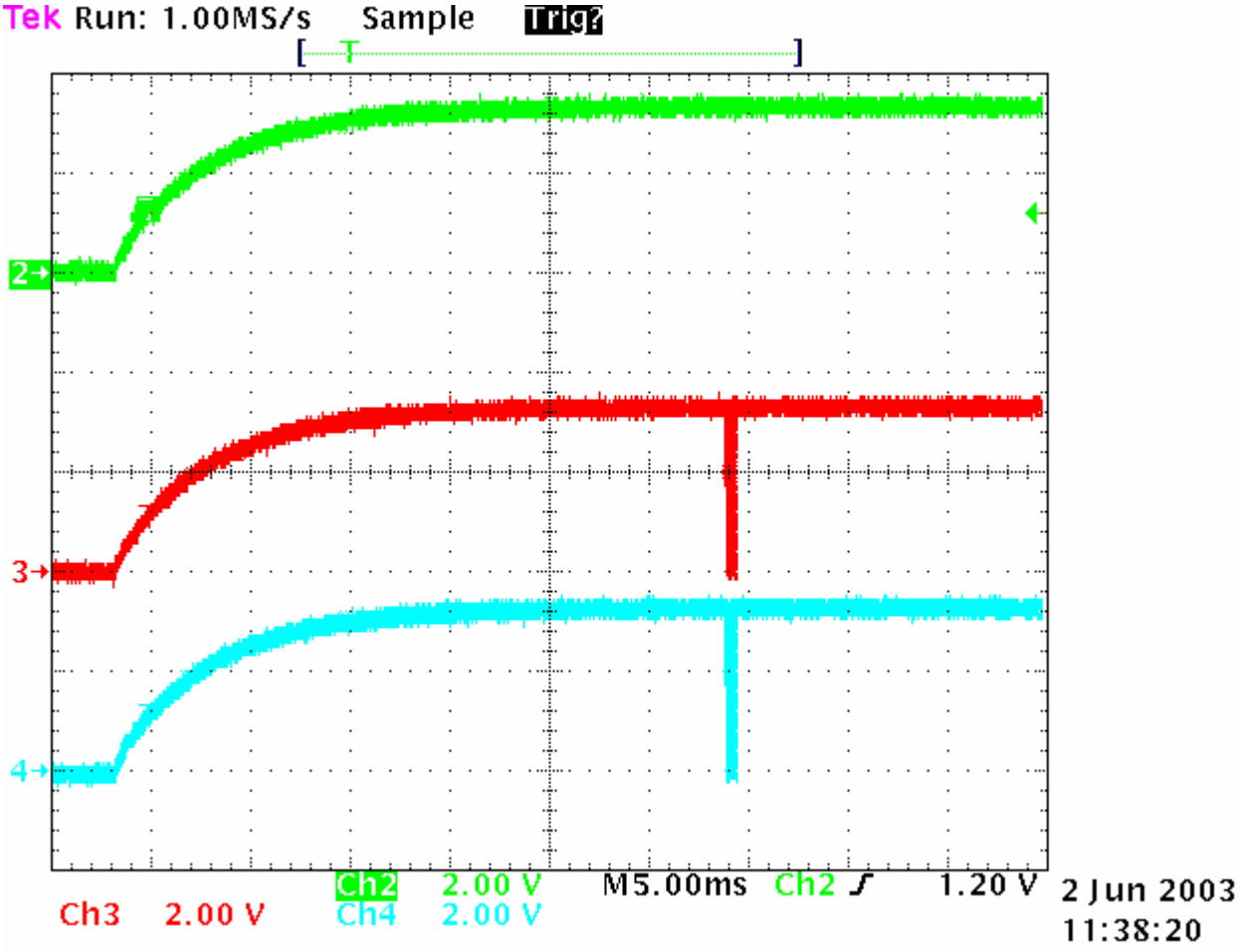

Figure 5. No EEPROM Present

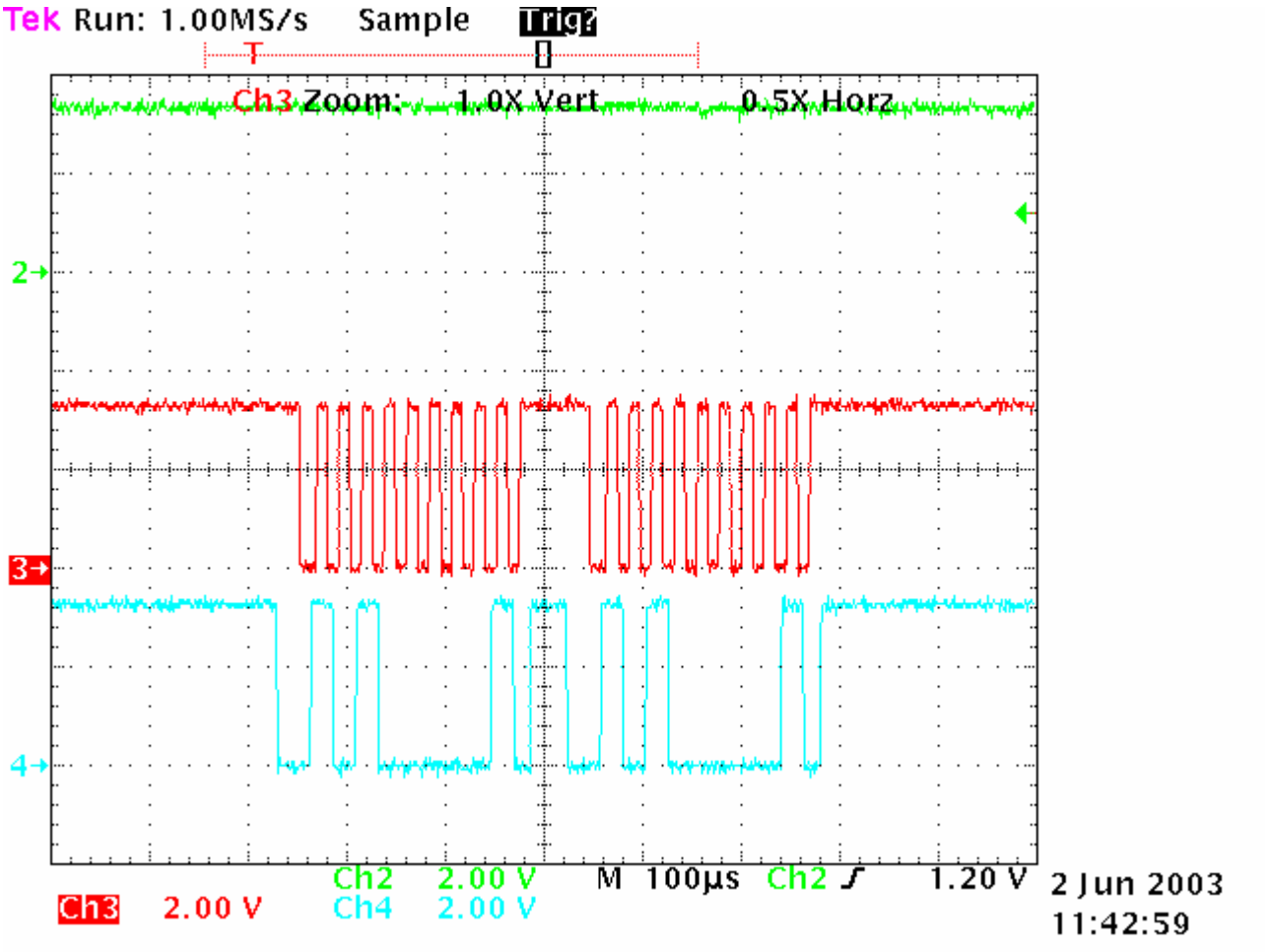

Figure 6. Detail of No EEPROM Present

When the EEPROM acknowledges but contains the wrong value, the EEPROM read stops after read of the indicator value. Figure 7 shows a read of a blank EEPROM. Figure 8 shows a detail of the initial address of the EEPROM with acknowledge present. Figure 9 shows an example read duration for the blank EEPROM.

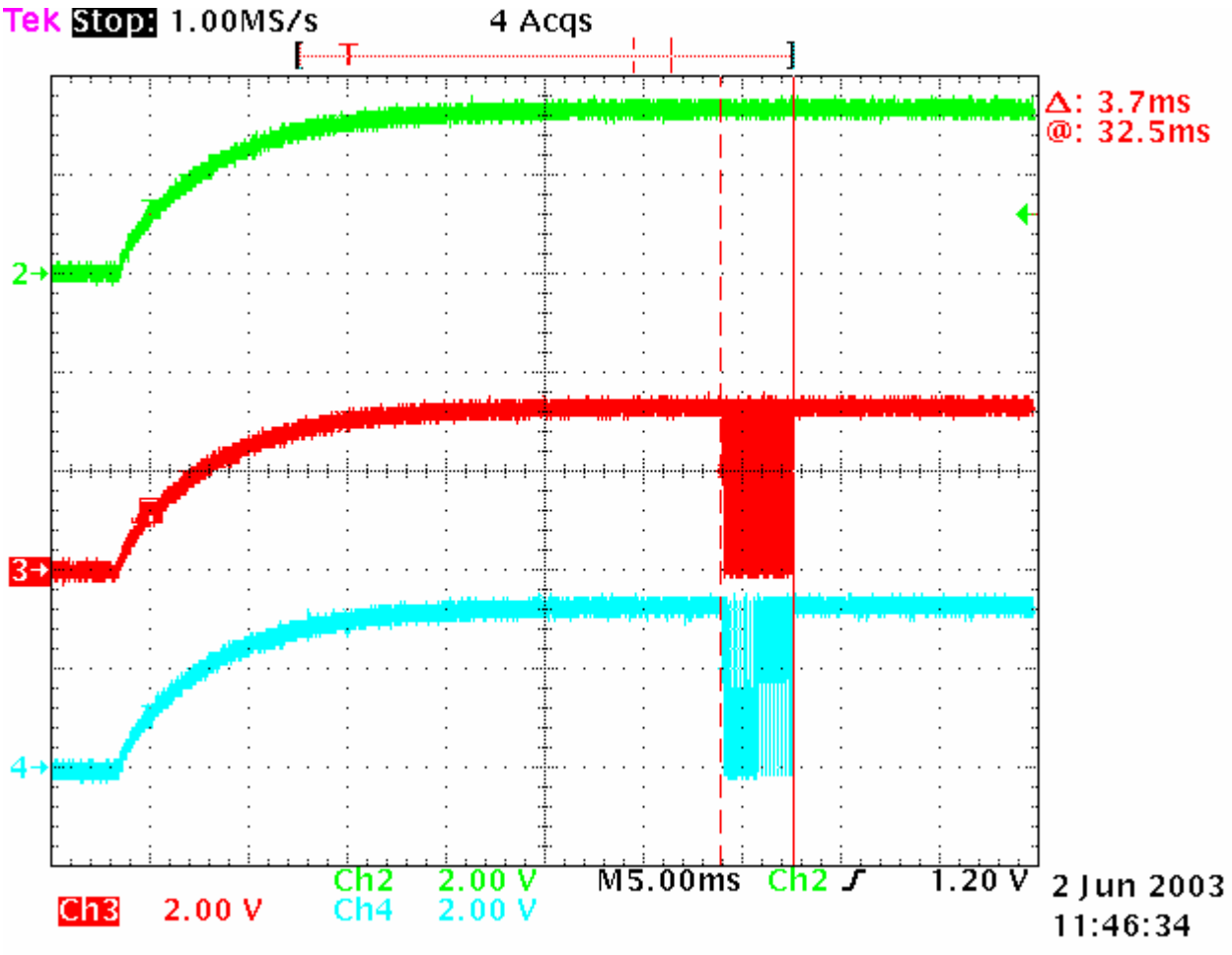

Figure 7. Blank EEPROM Read

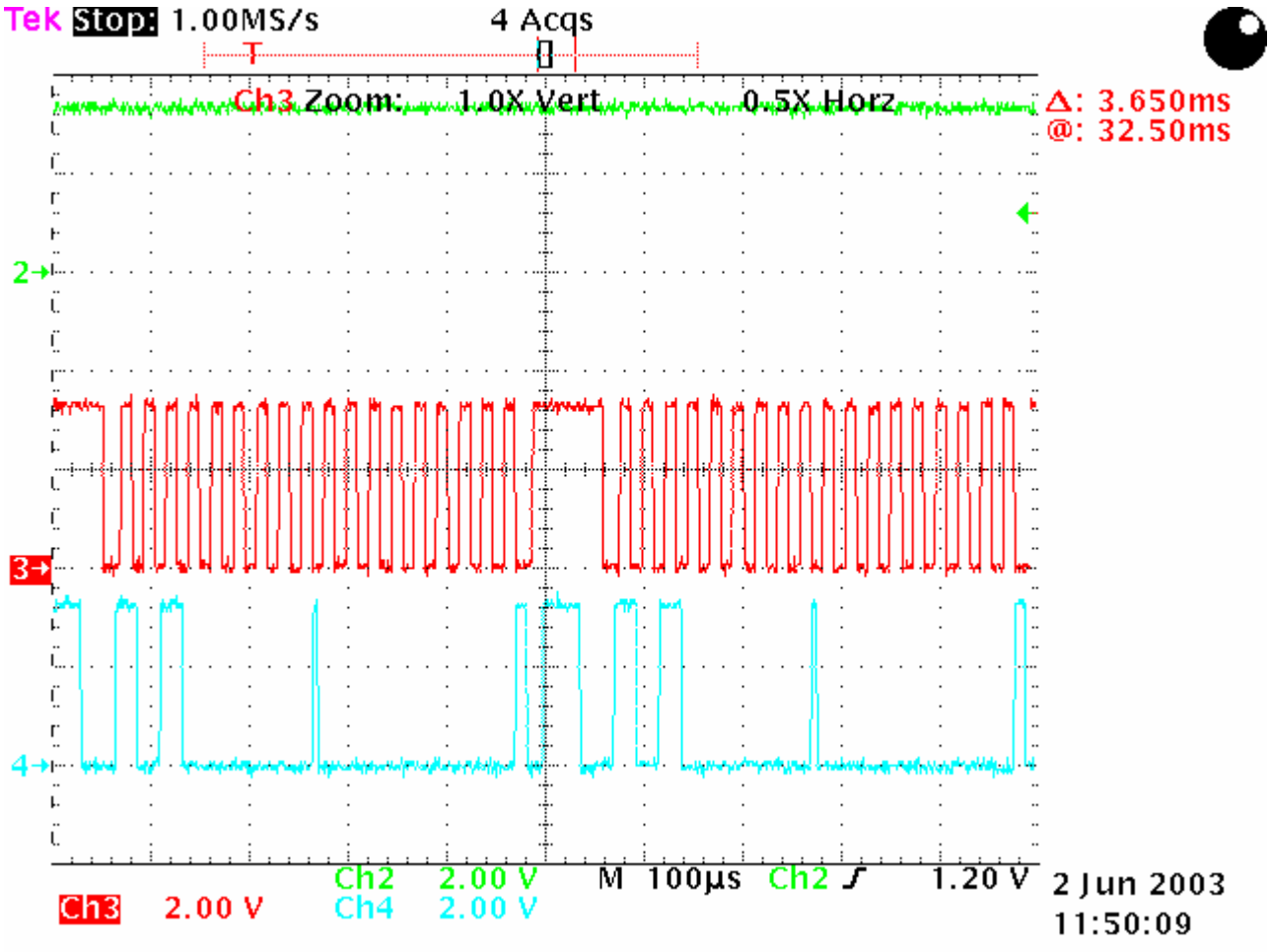

Figure 8. Blank EEPROM Initial Address

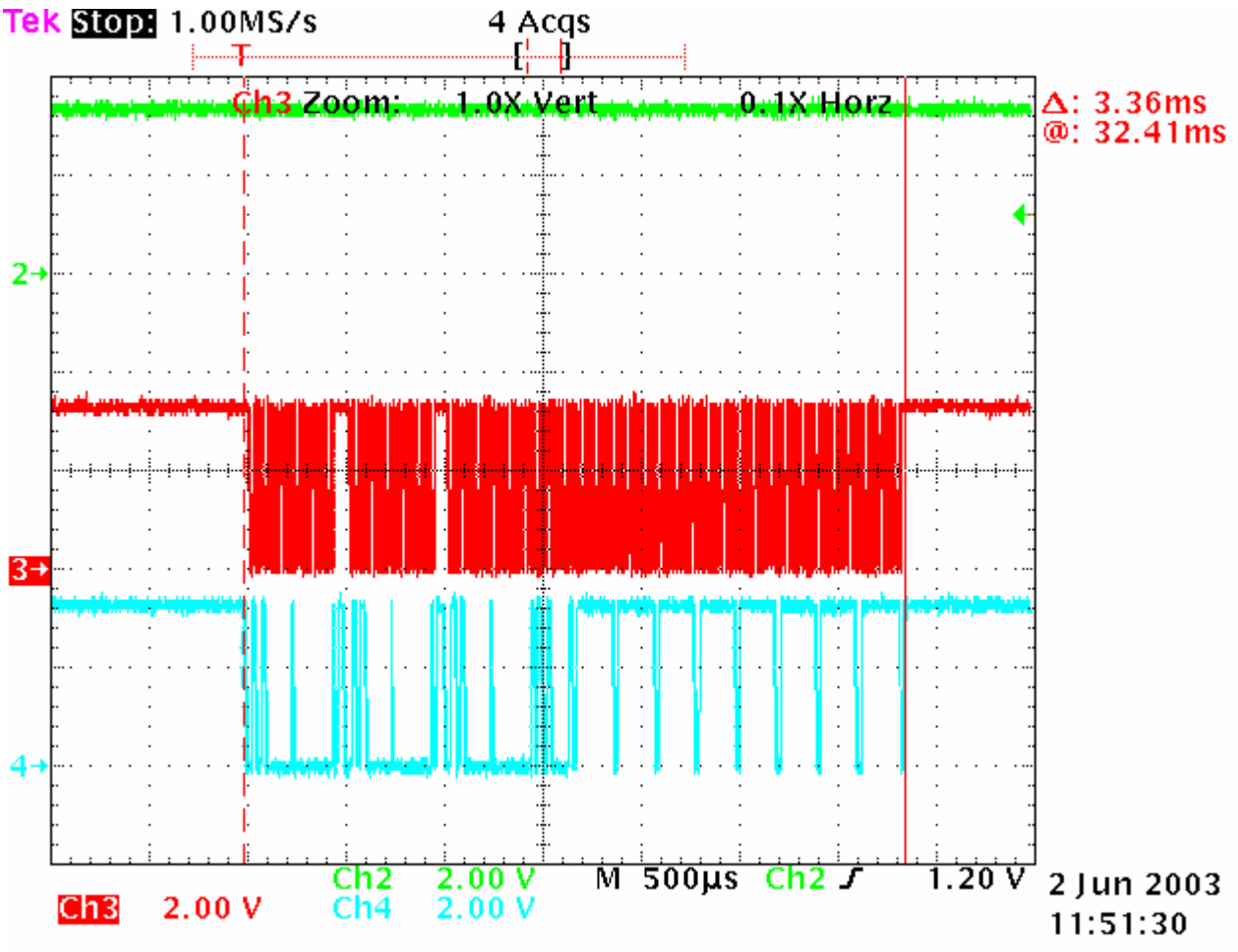

Figure 9. Blank EEPROM Read Duration

When there is a board fault that shorts the SCL and SDA lines together, the EEPROM can not be encrypted or read. Figure 10 shows a read sequence where SCL and SDA are shorted together. Figure 11 shows detail where both lines have a combination of the expected activity.

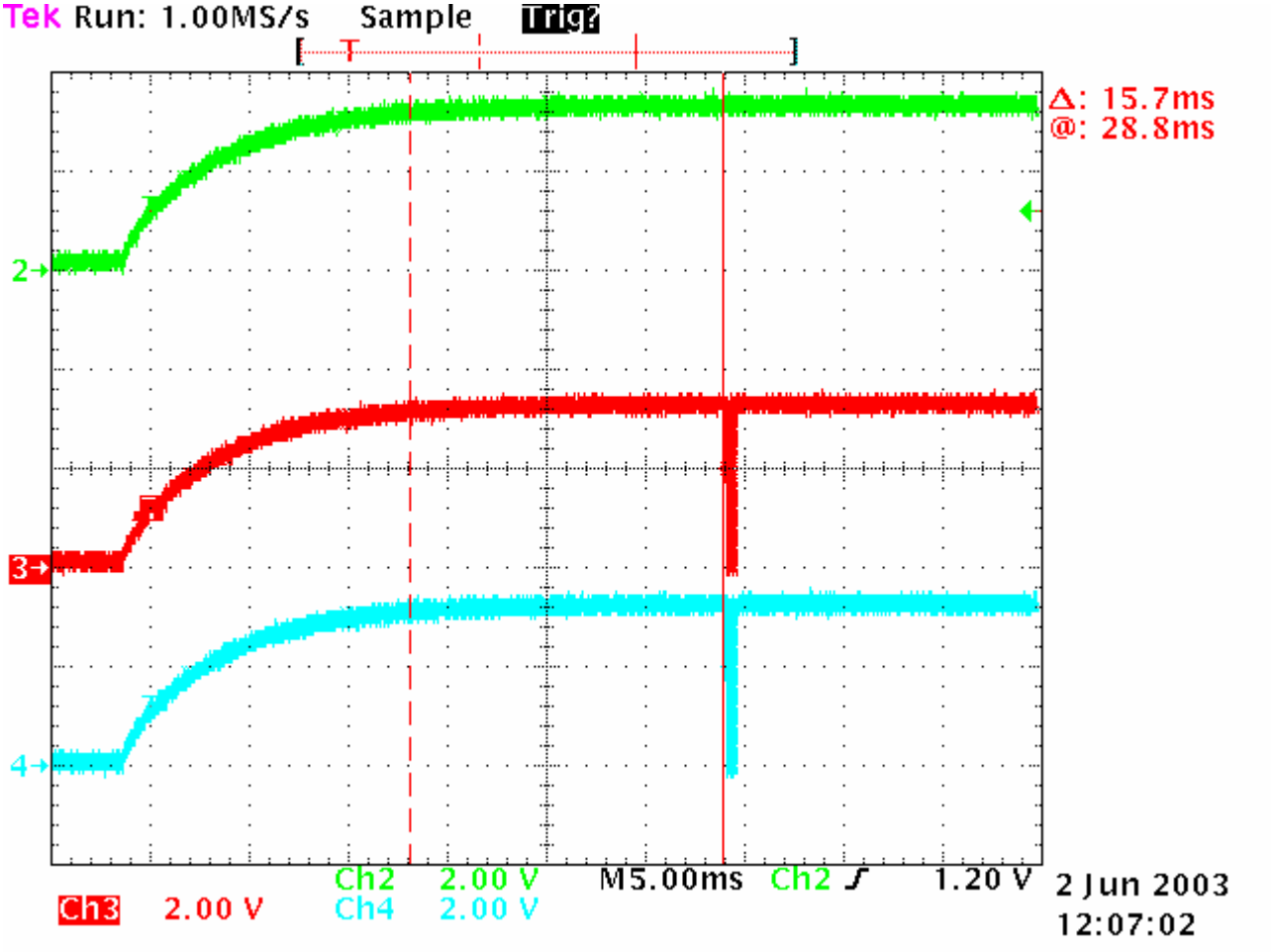

Figure 10. Shorted SCL and SDA

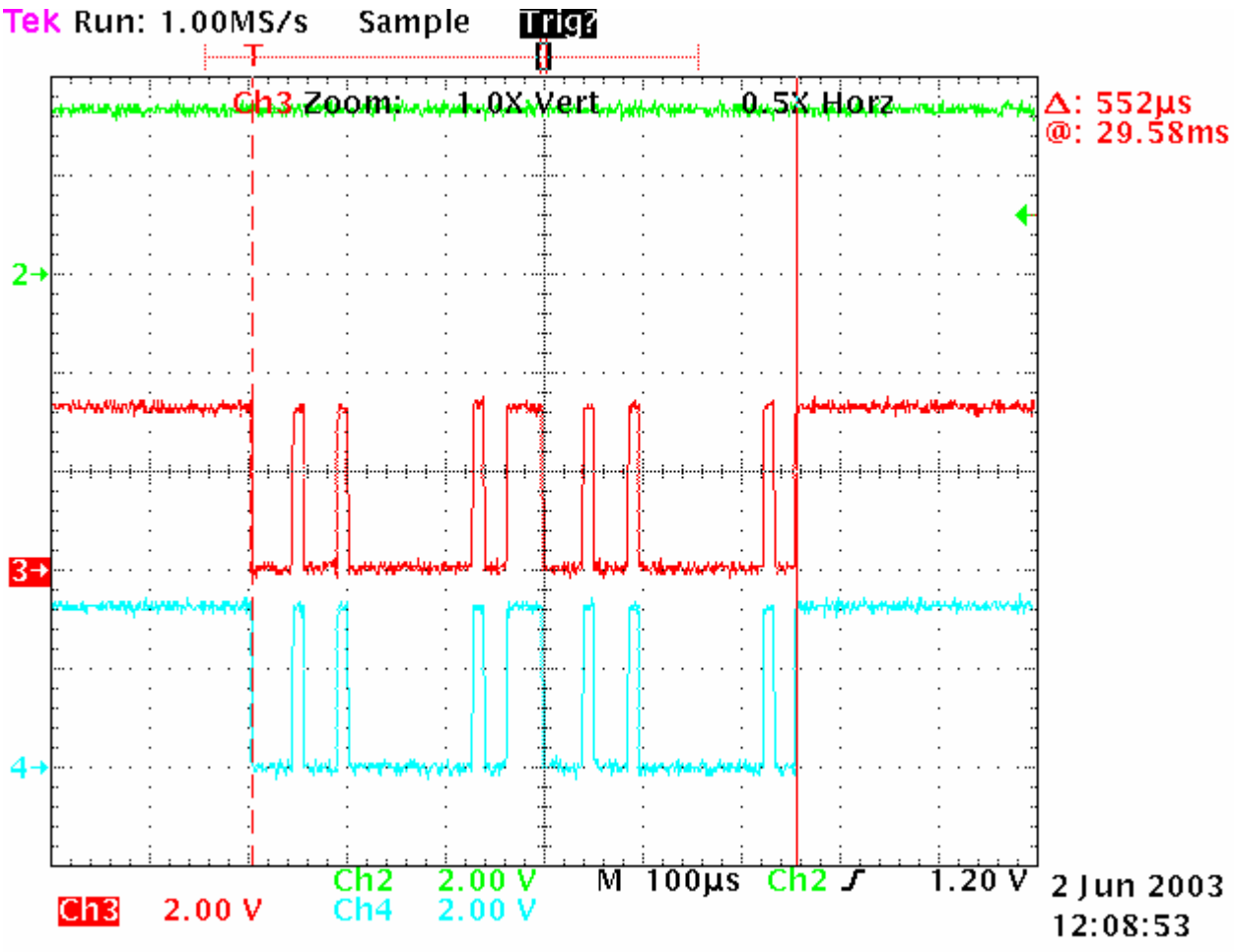

Figure 11. Shorted SDA and SCL Detail

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