Using the CDCL6010 as a Frequency Synthesizer and Jitter Cleaner

Madhu Balasubramanian *Serial Link Products*

ABSTRACT

This application report provides general guidelines for using the Texas Instruments' 1.8V LVDS/LVCMOS clock receiver CDCL6010 as a frequency synthesizer and/or jitter cleaner. This report reviews the basic device functionality and most efficient methods of use. The document also includes a detailed discussion of generating multiple frequencies with a common input frequency as well as a practical example of this technique. The report concludes with a brief description of recommendations on line terminations and power supply decoupling.

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1 Introduction

A phase-locked loop (PLL) is a closed-loop system that generates a signal related to the frequency and phase of an input reference signal. It typically involves locking its output (derived from a high-Q device) to its input, which is usually from a low-Q device. The PLL responds to frequency and phase variations of the input by automatically raising or lowering the frequency of the controlled oscillator through feedback, until the output is aligned with the phase and frequency of the system. A practical phase PLL usually assures lock in phase, but a lock in frequency with 0ppm error has not been demonstrated so far. Typical commercial PLLs demonstrate ensured frequency lock with a margin of error.

PLLs are widely used for synchronization purposes in several communication and consumer domains, including radio transmission, clock recovery and deskewing, spread spectrum, clock jitter reduction, clock generation, and clock distribution. PLLs typically used in high-performance, high-speed systems are required to have low noise/jitter clock outputs and low clock skew, among other requirements.

1.1 Past High-Performance PLL Trends

High-performance, high-speed systems demand components that exhibit close-to-ideal characteristics, such that the precision is not compromised while ensuring that the systems themselves do not get overly complicated. In electronic systems, this approach has led to shifting all processing from the analog domain to the digital domain while the signal transmitting and receiving are performed in the analog domain. This shift means that the high-performance systems generally have both analog and digital blocks as well as additional blocks to perform the analog-to-digital (A/D) and digital-to-analog (D/A) signal conversions. All the digital, A/D and D/A blocks also require high-precision clocking that involves high-performance clock generation and distribution circuitry; typically, this circuitry is a high-performance PLL. In the past, as a result of silicon process and chip design limitations, high-performance PLLs have generally relied on off-chip, high-Q mechanical devices such as (voltage-controlled) crystal oscillators to complete the feedback system in order to ensure high-quality outputs. Technology has not advanced enough to ensure a high-Q oscillator on silicon that integrates successfully with the rest of the PLL components.

Crystal oscillators are not without drawbacks, however. Traditional, fundamental-mode crystals are very difficult to cut, and are therefore very expensive at frequencies beyond 200MHz. Moreover, long frequency lines produce undesirable effects (such as electromagnetic interference, or EMI); to reduce these effects, multiple crystal oscillators are required at the point of clocking, greatly increasing system costs. For applications that require a variety of high frequencies, the use of multiple programmable-frequency synthesizers or fixed-frequency (voltage-controlled) crystal oscillators also drives up the system cost.

1.2 Recent High-Performance PLL Trends

Recent advances in silicon process technology have made possible the design of an on-chip, high-Q, inductor-based oscillator that costs just a fraction of a similar PLL that includes an off-chip (voltage-controlled), crystal-based oscillator. The performance difference between these two types of devices is negligible and insignificant for most applications. This new trend in silicon technology also allows for all PLL operations to be done on-chip without the need for external components. Moreover, the use of a programming on-chip oscillator and dividers enables the PLL to track a wide range of frequencies that are useful for many test applications.

TI's CDCL6010 is an example of this advanced device. The CDCL6010 PLL components are all on-chip; it requires no additional off-chip components for device operation. It provides an option of switching to an external loop filter if used as a jitter cleaner. The CDCL6010 also includes a programming interface, enabling the PLL to cover wide frequency ranges at its output while ensuring very low noise and jitter over the entire device operating range.

2 Functional Description

The CDCL6010 is a high-performance, low-jitter clock synchronizer and jitter cleaner that synchronizes the reference clock to its on-chip, voltage-controlled oscillator (VCO) frequency. The input reference clock should be ac-coupled from an LVDS buffer or directly coupled to any input from a 1.8V LVCMOS signal. The programmable input divider, feedback divider, and output divider give high flexibility to the frequency

ratio of the reference clock to the output clock that operates from 15MHz to 1.25GHz. Through user selection between the wideband, on-chip loop filter and the narrowband, off-chip loop filter components, the PLL bandwidth can be adjusted to meet different application requirements. Device programming is done through an I²C™ interface. The CDCL6010 is characterized for operation from 1.7V to 1.9V and from –40°C to +85°C.

2.1 Clock Synchronizer

As Figure 1 shows, the CDCL6010 PLL consists of an internal phase frequency detector, charge pump, passive loop filter, a liquid crystal (LC)-oscillator based VCO, input dividers and feedback dividers. Through the PLL operation, the VCO output synchronizes with the input reference clock. The VCO output is then sent through the 10 programmable output dividers and is available in CML type, which is also synchronized in phase and frequency with the input reference clock. The 10 outputs are available in two banks. Each bank can also be programmed to any phase adjustment that has fine adjust capabilities which increase as the bank output divide increases.

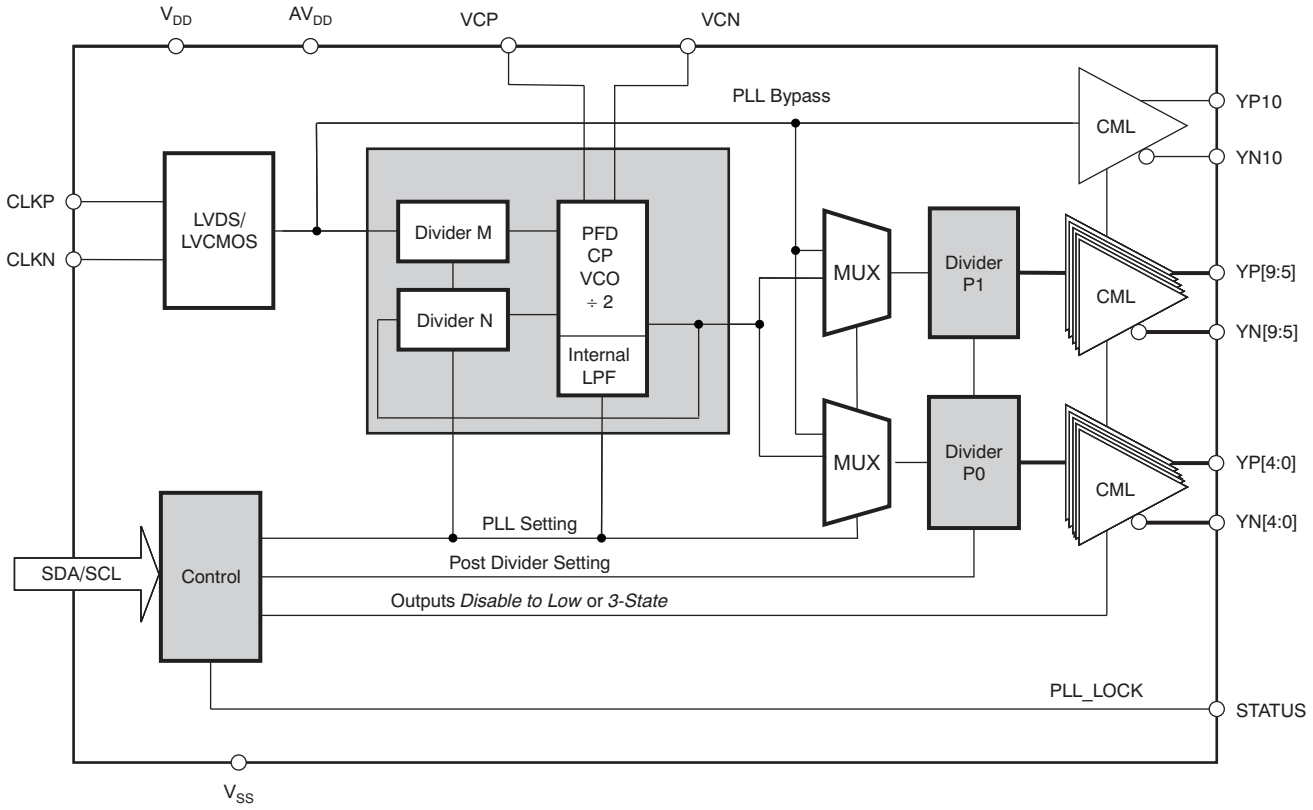

Figure 1. CDCL6010 Block Diagram

2.2 Frequency Multiplication and Division

Through the I²C interface, the input divider (***M***) can be set to 1, 2, 4, or 8; the feedback divider (***N***) can be set to 32 or 40; and the output dividers (***P0, P1***) can be set to 1, 2, 4, 5, 8, 10, 16, 20, 32, 40, or 80. The input divider and the feedback divider must be chosen such that the PFD update frequency is between 30MHz and 40MHz and the VCO frequency is between 2.4GHz and 2.55GHz. The VCO frequency is always divided by 2 within the PLL and before the N and P dividers. The loop filter settings can be chosen from the on-chip or off-chip passives. The output type is CML; the frequencies are set by the chosen output divider setting for a bunch of five outputs per each of the two banks.

2.3 Output Phase Adjustment

Each output bank can also have its phase adjusted, with granularity that depends on the bank output divide. For an output divide of 5, 10, 20, 40, or 80, the number of phase setting options (including the current zero phase shift) is (P/5); the phase adjust granular step size is (10π/P), where *P* is the output divide. For an output divide of 1, 2, 4, 8, 16, or 32, the number of phase setting options (including the current zero phase shift) is P; the phase adjust granular step size is (2π/P), where *P* is the output divide.

For example, if P is chosen as 20, the total number of phase offsets that can be chosen for a bank of outputs is 4, and the phase adjust granular step size is π/2, or 90 degrees.

2.4 Jitter Cleaner

The advantage of having programmable components for the PLL loop filter is that a wide range of PLL bandwidths can be selected, depending on both the jitter requirements of the particular system and the end application of the given device. The jitter cleaning action depends on the PLL bandwidth. All the noise present in the input reference clock up to the loop bandwidth passes into the output and beyond; the internal VCO noise also passes into the output. In the case of an extremely noisy input, for example, with 2ps and beyond RMS jitter in an integration limit of 200kHz to 20MHz, it might be wise to set the PLL bandwidth at 50kHz or less in order to achieve reduced jitter at the output across the same integration limits. With a proper loop bandwidth, the CDCL6010 operates as a jitter cleaner.

3 CDCL6010 Frequency Synthesis

This section reviews relevant aspects of choosing the proper input frequency, divider, and VCO settings needed to obtain a set of output frequencies using the multiple outputs of the CDCL6010 device.

3.1 Multiple Frequency Synthesis Example

Assume a typical application, where a total of five 156.25MHz and five 125MHz output clocks are desired and must be phase locked to a single back-plane input reference clock. We must identify the M, N, and P dividers as well as the input frequency to lock to and any related PLL settings needed to derive the two output frequencies from the common input frequency. These steps may be followed to solve this example.

Step 1. From Figure 1, we can infer that the relationship between the output frequency and the input frequency can be described in Equation 1:

$$F_{OUT} = F_{IN} \times \frac{N}{(M \times P)} \quad (1)$$

Provided that:

$30MHz < (F_{IN} / M) < 40MHz$

and

$1200MHz < (F_{OUT} \times P) < 1275MHz$

Step 2. Keep these parameters in mind while resolving Equation 1:

- The P divider can be chosen from 1, 2, 4, 5, 8, 10, 16, 20, 32, 40 or 80
- The on-chip VCO tuning range is from 2.4GHz to 2.55GHz
- The M divider can be chosen from 1, 2, 4 or 8
- The N divider can be chosen from 32 or 40

Step 3. Given multiple desired output frequencies, the first step is to establish a common input frequency, by selecting M and N dividers for different P divider settings to satisfy Equation 2 through Equation 4:

$$F_{IN} = F_{OUT1} \times \frac{(M \times P_1)}{N} \quad (2)$$

$$F_{IN} = F_{OUT2} \times \frac{(M \times P_2)}{N} \quad (3)$$

$$F_{OUT1} \times P_1 = F_{OUT2} \times P_2 \quad (4)$$

So that the common input frequency always lies between 30MHz and 40MHz and the VCO frequency is the same for deriving both outputs. For our example of 156.25MHz and 125MHz outputs, in order to use a common VCO frequency, the P dividers to be used are (*P0 = 8*, *P1 = 10*) and the common VCO frequency is 2500MHz. Moreover, the N divider to be used is (*N = 40*), ensuring that the (F_{IN} / M) ratio is within the allowable range of 30MHz–40MHz.

Step 4. Recall that the M divider can be 1, 2, 4 or 8, as shown in Step (2). Therefore, for the current example, the possible combinations of the input frequency and the M divider are:

- M = 1, F_{IN} = 31.25MHz
- M = 2, F_{IN} = 62.5MHz
- M = 4, F_{IN} = 125MHz
- M = 8, F_{IN} = 250MHz

Figure 2 shows the programming settings and required input frequency necessary to achieve 156.25MHz and 125MHz outputs.

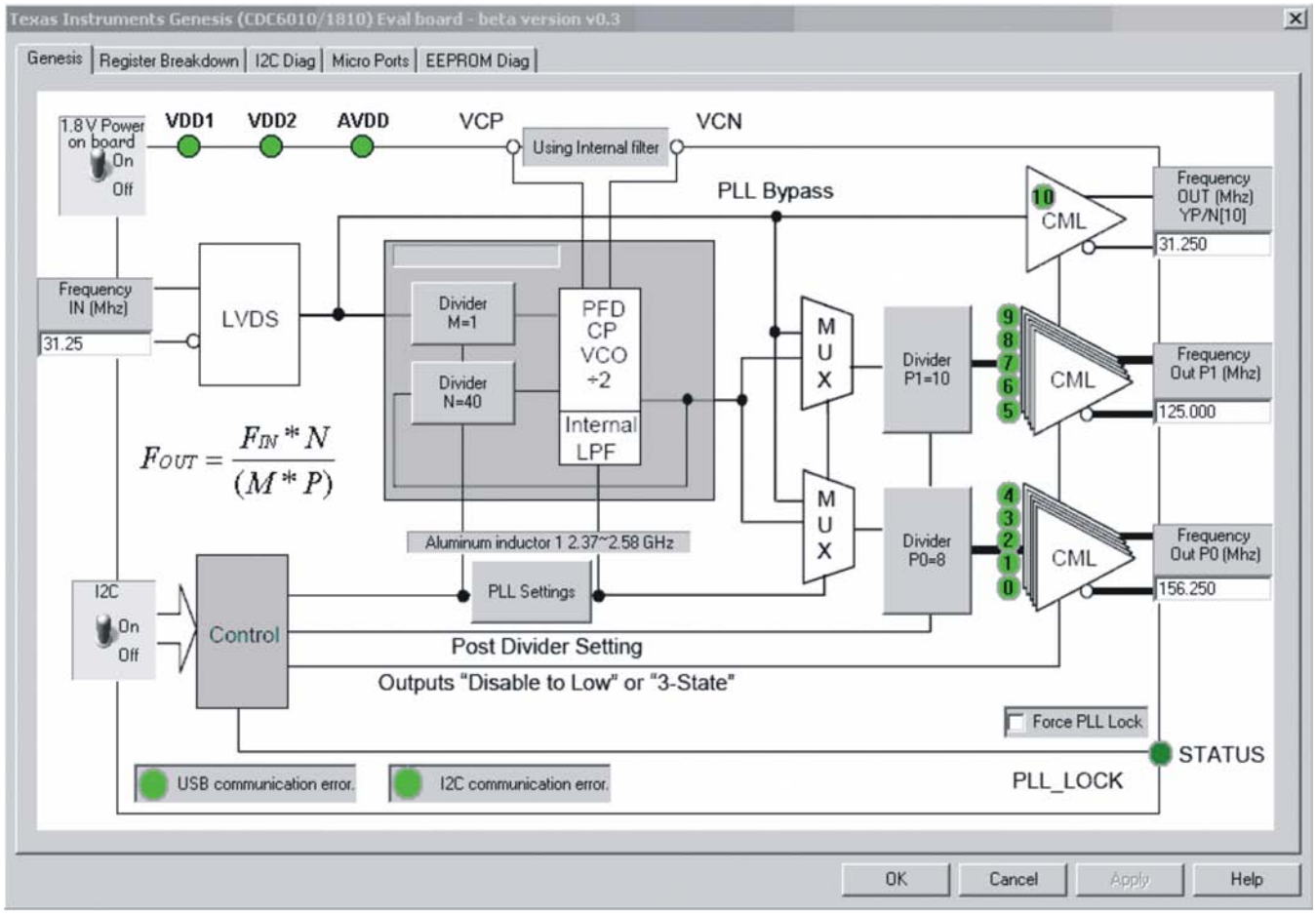

Figure 2. CDCL6010 Programming Settings and Required Input Frequency

4 PLL Bandwidth Selection

Unlike other PLLs, the CDCL6010 loop filter components are not fixed. It is possible to choose a loop bandwidth from 10kHz to 400kHz through the programming interface.

4.1 Loop Bandwidth

The PLL bandwidth depends on the loop filter, charge pump current, VCO gain, and PFD update frequency. In the CDCL6010, the VCO gain and the PFD update frequency are fixed values, as illustrated in Figure 3.

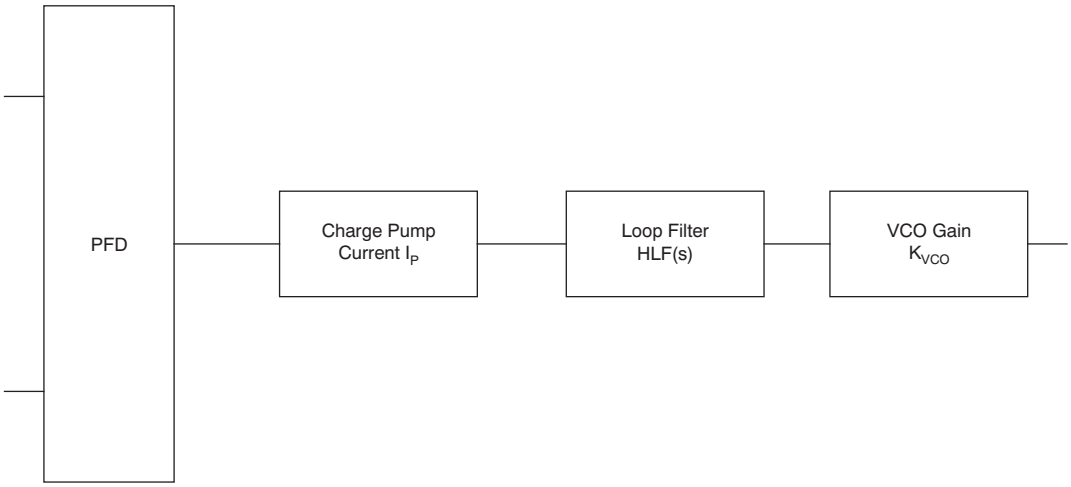

Figure 3. PLL Bandwidth Dependencies

4.2 Jitter Peaking

Around the loop bandwidth, the incoming jitter from the reference clock may be amplified. This phenomenon is called *jitter peaking*. For some applications, jitter peaking has an adverse effect on jitter performance, if the jitter peaking occurs within the band of interest. If the jitter peaking occurs outside the band of interest, applications generally do not suffer any unusual effects. In any case, limit the jitter peaking to within 10dB to prevent the loop from becoming unstable. Figure 4 shows an example of a PLL phase response with jitter peaking of 2dB.

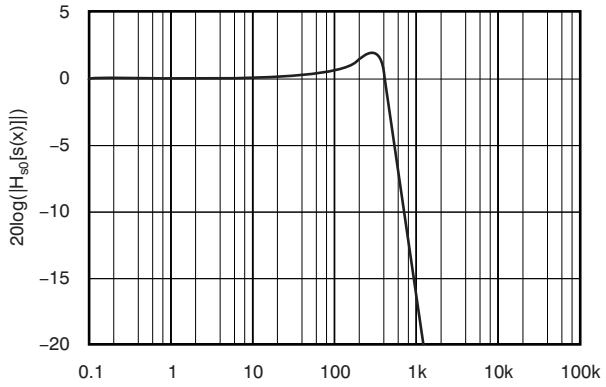

Figure 4. Jitter Peaking Around PLL Bandwidth

4.3 Phase Margin

Phase margin is important for PLL stability, and influences the PLL lock time. As a rule of thumb, no less than a 50 degree phase margin is recommended for a stable clock operation.

5 CDCL6010 Noise Performance with Varying PLL Bandwidths

Figure 5 illustrates the on-chip, fixed passive loop filter structure of the CDCL6010. The device also allows for switching to an off-chip, passive loop filter of the same structure. R, C_1 and C_2 generate a complex pole and zero in the closed loop response. Table 1 (from the CDCL6010 datasheet) contains the recommended loop filter element values for achieving a particular loop bandwidth.

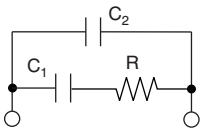

Figure 5. CDCL6010 On-Chip Active Loop Filter

Table 1. PLL Bandwidth Setting

PLL Bandwidth(1) (kHz)	SEL (BW)				C_1 (nF)	R (Ω)	C_2 (nF)	On-Chip Loop Filter ON/OFF	Notes
	[3]	[2]	[1]	[0]					
400	0	0	0	0	N/A	N/A	N/A	ON	Default
350	0	0	1	0	2.2	8660	0	OFF	
300	0	0	1	1	3.3	7500	0	OFF	
250	0	1	0	0	4.7	6200	0	OFF	
200	0	1	1	0	8.2	4990	0	OFF	
175	1	0	0	0	10	4300	0	OFF	
150	1	0	1	0	15	3740	0	OFF	
125	1	1	1	1	22	3090	0	OFF	
100	1	1	1	1	33	2490	0.24	OFF	
75	1	1	1	1	56	1870	0.82	OFF	
50	1	1	1	1	150	1210	2.70	OFF	
20	1	1	1	1	680	470	18	OFF	
10	1	1	1	1	3300	220	68	OFF	

(1) Refer to CDCL6010 Functional Block Diagram for the external low pass filter architecture.

Depending on the target application for the CDCL6010, the PLL bandwidth can be reduced by programming the device to use the external passive loop filter and adjusting the loop filter components such that the resulting jitter peaking appears outside the band of interest.

5.1 Test and Measurements Setup

Figure 6 shows the block diagram of the test setup. An input reference from an HP8133 signal generator is fed into TI's fractional multi-PLL chip (CDCE706) for media applications that are deemed noisy for a communication chain. The output jitter from the CDCE706 varies according to the number of fractional steps needed to achieve the output frequency from an input frequency and also according to the number of PLLs concurrently operating. The output of this block is fed to the Aeroflex PN9000 to measure its phase noise. This line is also damped down to about 1.8V, and then fed to the input of the CDCL6010; its output is fed to the Aeroflex PN9000 to measure its phase noise. The CDCL6010 PLL bandwidth is programmed appropriately, according to the target application required band of interest, to check its jitter attenuation capabilities. All measurements are taken at nominal process, temperature and voltage conditions.

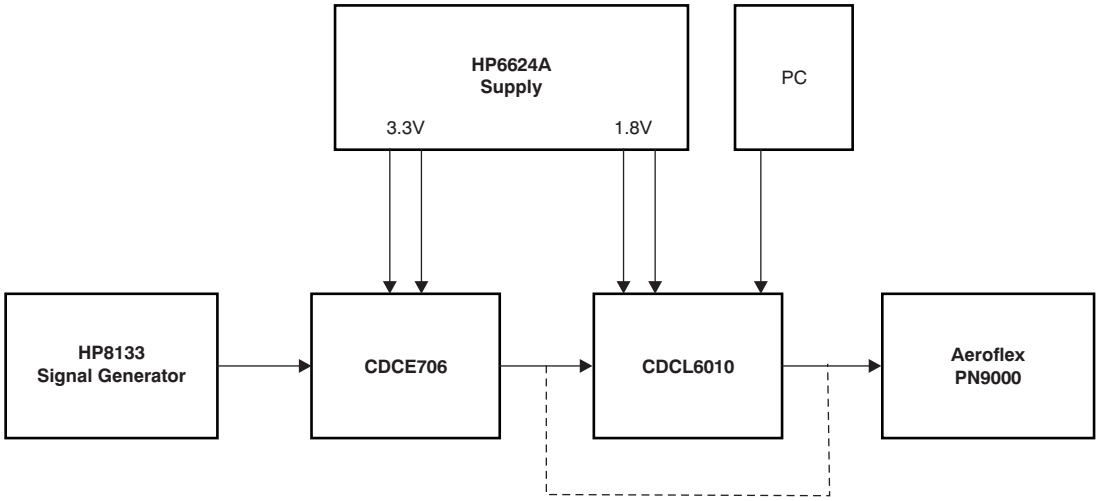

Figure 6. CDCL6010 Jitter Attenuation Test Setup

5.2 CDCL6010 Jitter Attenuation in 200kHz–20MHz Band

For certain mid- to high-end communications applications, the typical signal bandwidth of devices that deal with the digital signal is about 200kHz or higher around the carrier to which the devices are tuned. These signal-chain devices include DSPs, ASICs, and so forth. Currently, these units tend to be 1.8V devices, and need clocks with jitter requirements of 2ps RMS or less, and therefore can be clocked with the CDCL6010. For such applications, the jitter peaking (if any) as a result of PLL bandwidth reduction should be made to fall outside the band of interest (typically much lower than 200kHz). To achieve this outcome, the device must be programmed to use the off-chip, passive loop filter, and the loop filter components R, C1, and C2 should be modified. The lowest PLL bandwidth of 10kHz as set by the passive loop filter components, chosen according to the ***PLL Bandwidth Setting*** section of the CDCL6010 datasheet, results in the highest jitter attenuation and jitter peaking out-of-band.

Table 2 lists the CDCL6010 input and output jitter results of the test performed. We can conclude that for signal bandwidths of 200kHz with jitter requirements of 2ps RMS or less, the CDCL6010 can act as an efficient jitter cleaner and meets the specifications for input references having up to 25ps RMS jitter. Figure 7 through Figure 9 show the phase noise plots of inputs and outputs of the CDCL6010 during some tests shown in Table 2. Figure 10 shows a plot of input jitter versus output jitter that highlights the jitter cleaning capabilities of the CDCL6010.

Table 2. CDCL6010 Input Jitter and Output Jitter for All Inputs and Outputs at 122.88MHz

Input Jitter (ps, RMS), 200kHz–20MHz	Output Jitter (ps, RMS), 200kHz–20MHz
0.90	1.48
1.90	1.54
4.66	1.56
9.64	1.59
13.98	1.63
16.40	1.87
20.43	1.90
25.05	1.96
35.12	2.14
40.00	2.25

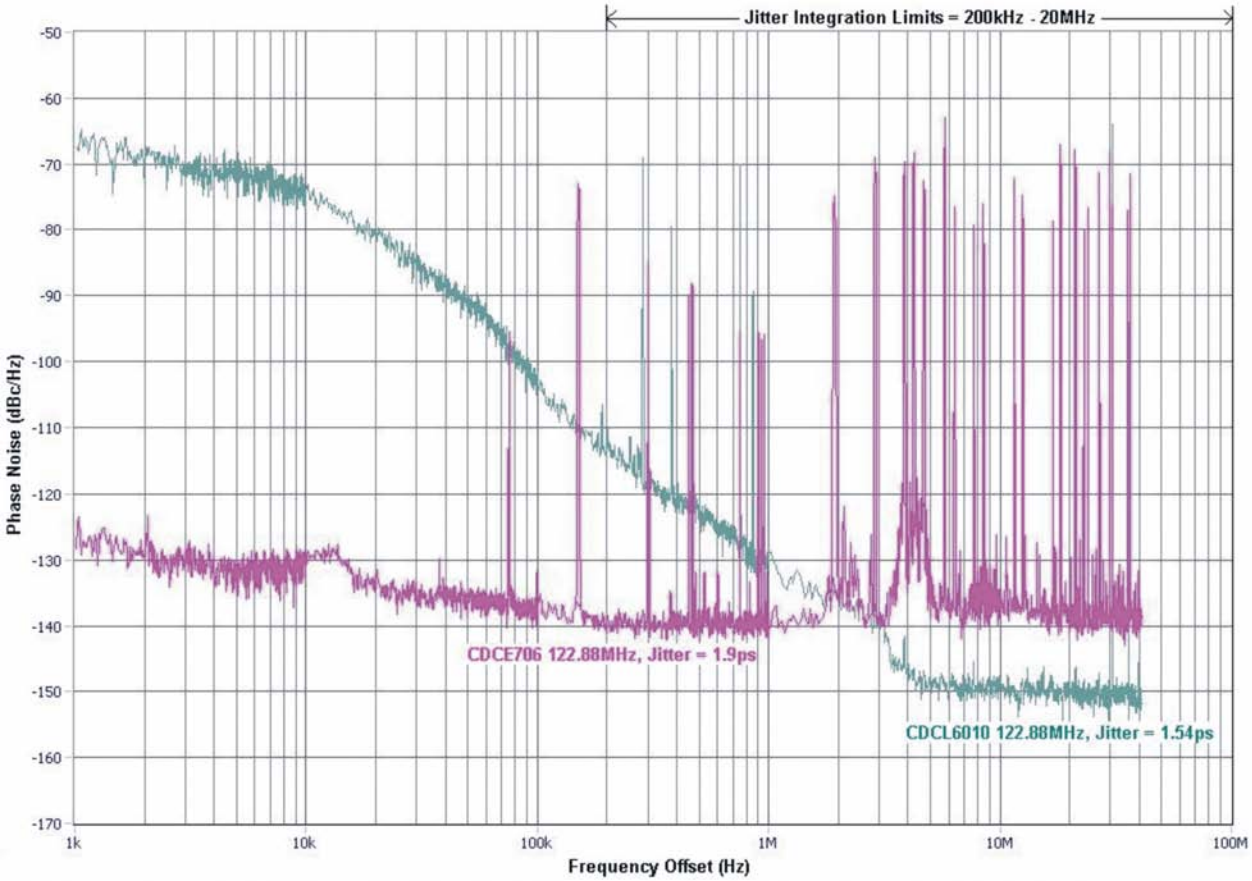

Figure 7. CDCL6010 Input and Output Phase Noise (122.88MHz), Input Jitter = 1.9ps RMS

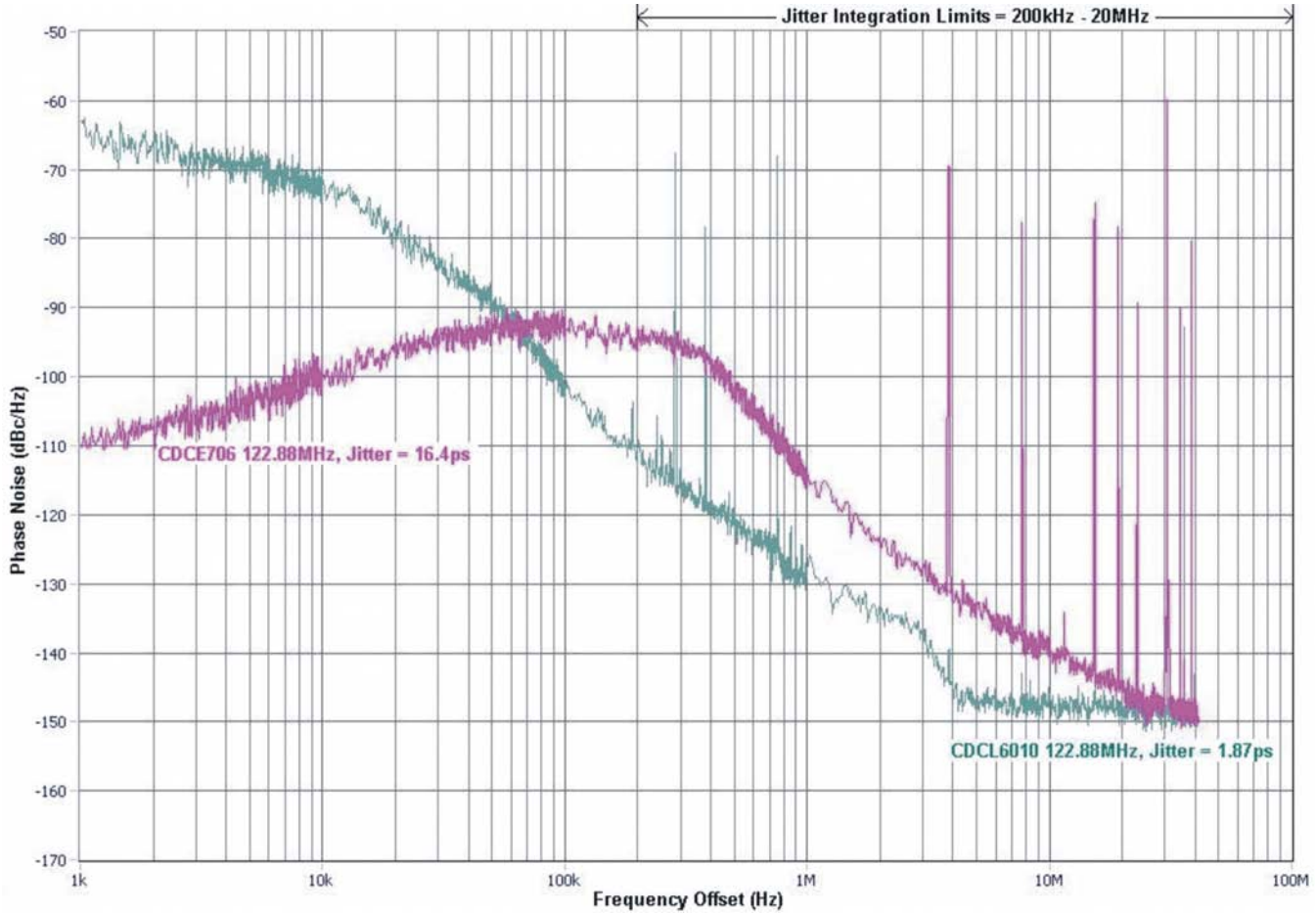

Figure 8. CDCL6010 Input and Output Phase Noise (122.88MHz), Input Jitter = 16.4ps RMS

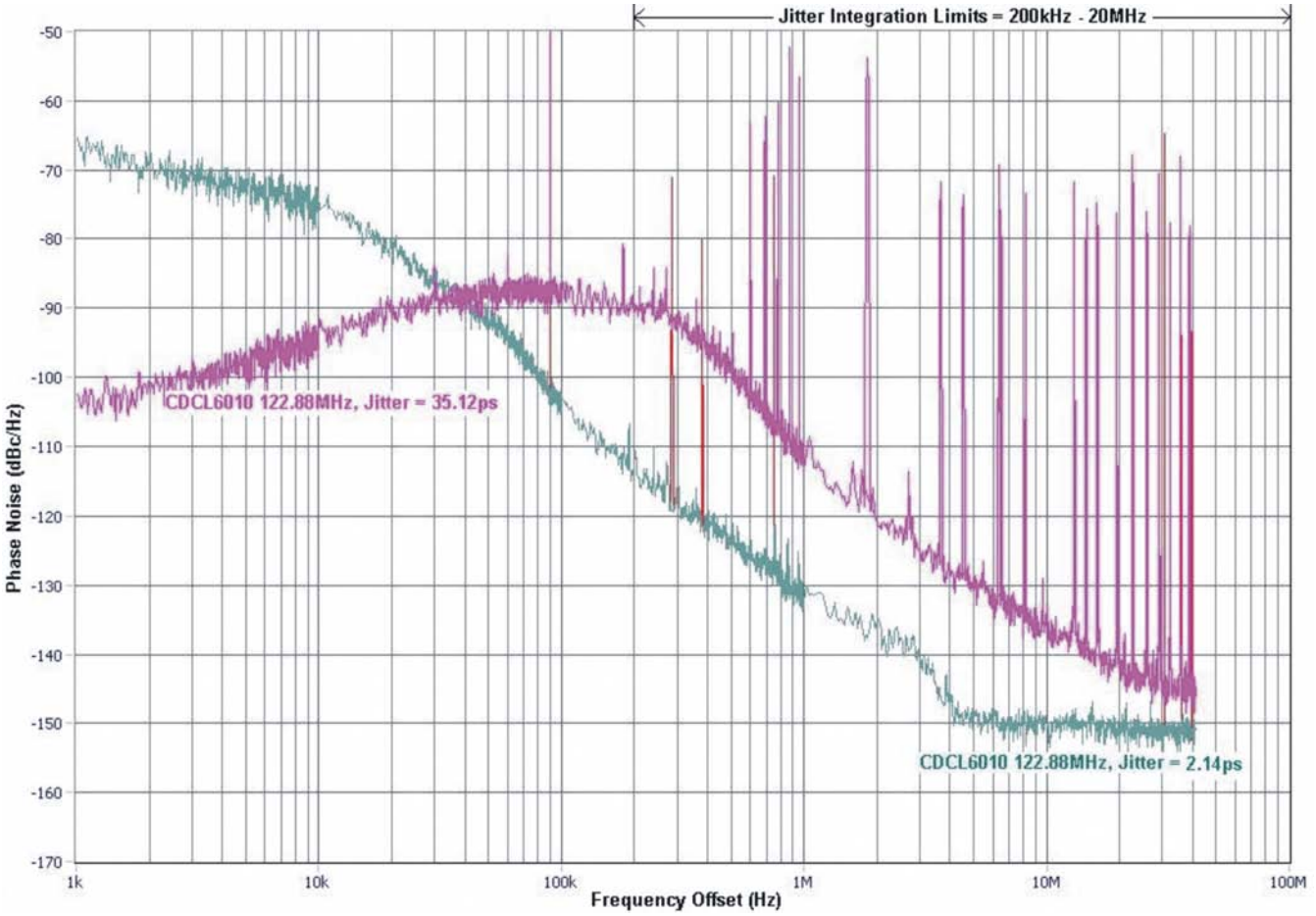

Figure 9. CDCL6010 Input and Output Phase Noise (122.88MHz), Input Jitter = 35.2ps RMS

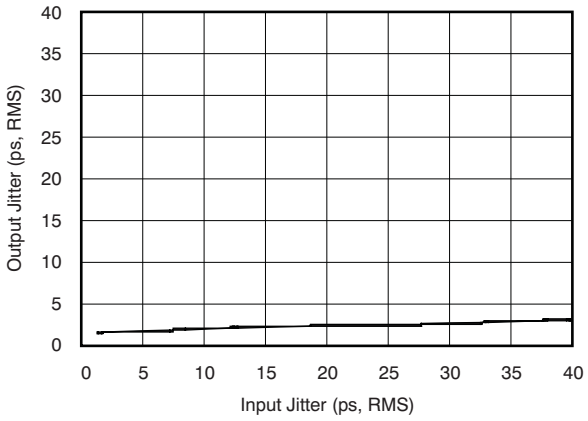

Figure 10. CDCL6010 Jitter Cleaning Capability

6 Output Termination

The CDCL6010 is a 1.8V, CML-type clock driver.

6.1 CML Termination

The CDCL6010 has on-chip, 50Ω termination to V_{CC} for each CML output. Either direct termination or terminations for ac-coupling can be used with the CML outputs. If the supply voltage of the driver and the receiver are different, ac-coupling is required.

6.1.1 Direct-Coupled CML Termination

Figure 11 shows a termination circuit that is generally recommended for direct termination. An optional 100Ω resistor can also be placed at the receiver end to terminate the lines at both ends of the differential signal.

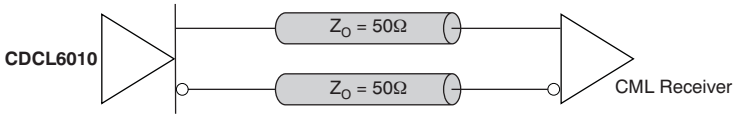

Figure 11. Direct-Coupled Output Termination Circuit

6.1.2 AC-Coupled CML Termination

Figure 12 shows a termination circuit that is generally suggested for ac-coupled termination. The CML receiver is assumed to have on-chip, 50Ω termination resistors on each line.

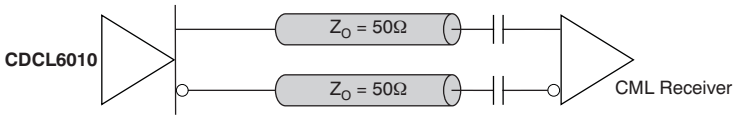

Figure 12. AC-Coupled Output Termination Circuit

7 Input Termination

The CDCL6010 is a 1.8V LVDS/LVCMOS clock receiver. The sense circuit within the CDCL6010 differentiates between LVDS and LVCMOS input types and automatically adjusts its input impedance to 100Ω between the differential inputs in case of LVDS, and a high impedance in case of LVCMOS.

7.1 LVDS Termination

For LVDS inputs, the CDCL6010 has on-chip, 100Ω termination resistors between the differential inputs. AC-coupling is recommended for the LVDS inputs.

7.1.1 AC-Coupled LVDS Termination

Figure 13 shows a general termination circuit that is recommended for ac-coupled termination.

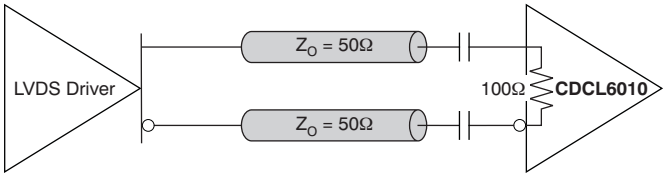

Figure 13. AC-Coupled Input Termination Circuit

7.2 Input LVCMOS Termination

The CDCL6010 can also accept a direct-coupled, single-ended LVCMOS signal with a signal strength that does not exceed 1.8V.

7.2.1 Driven From 1.8V LVCMOS Driver

Figure 14 shows a termination circuit, recommended for a 1.8V LVCMOS driver interfacing with the CDCL6010 input.

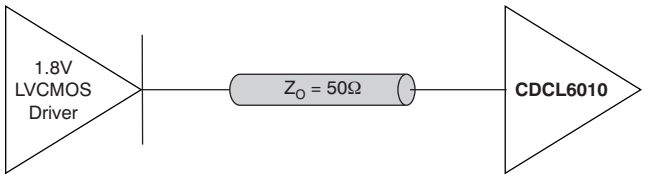

Figure 14. 1.8V Single-Ended LVCMOS Interface to CDCL6010

7.2.2 Driven From 3.3V LVCMOS Driver

If a 3.3V LVCMOS driver, such as the CDCE706, is used to drive the single-ended input of the CDCL6010, the line should be damped to reduce the swing from 3.3V to 1.8V or less as well as to ensure close-to-optimal termination to minimize signal integrity. Figure 15 illustrates a general recommendation for using the CDCE706 to drive the CDCL6010.

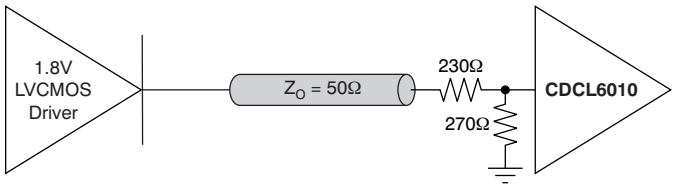

Figure 15. Single-Ended LVCMOS Interface from CDCE706 to CDCL6010

8 Power-Supply Decoupling

PLL-based frequency synthesizers are very sensitive to noise on the power supply that can dramatically increase the PLL jitter. This sensitivity is especially true for analog-based PLLs. It is essential, then, to reduce noise from the system power supply, especially when jitter/phase noise is very critical to applications. A PLL often has attenuated jitter because of power-supply noise at frequencies beyond the PLL bandwidth arising from attenuation by the loop response. It is also recommended to use separate power supplies for the analog PLL core and I/Os, if such an option is provided.

Filter capacitors can eliminate the low-frequency noise from the power supply, whereas the bypass capacitors provide the very low impedance path for high-frequency noise and guard the power-supply system against any induced fluctuations. Inserting a ferrite bead between the board power supply and the chip power supply isolates the high-frequency switching noise generated by the clock driver, preventing this noise from leaking into the board supply. Choosing an appropriate ferrite bead with low dc resistance is important because it is imperative to maintain a voltage at the CDCL6010 power-supply pin that is greater than the minimum voltage needed for its proper operation. At dc, the ferrite bead should have a voltage drop across itself; the maximum drop depends on the maximum dc resistance of the bead and the maximum dc current that the CDCL6010 draws out of the 1.8V power supply.

For example, assume the CDCL6010 uses separate power supplies for its PLL core and I/Os, or AV_{DD} and V_{DD} respectively. For proper operation, the CDCL6010 requires a minimum power-supply voltage of 1.7V on both AV_{DD} and V_{DD}, and draws 85mA from AV_{DD} and 270mA from V_{DD}. Assuming a 1.8V supply regulated from a 3.3V board supply, the ferrite bead maximum dc resistance on AV_{DD} and V_{DD} can be 1.17Ω and 0.37Ω, respectively. Figure 16 shows a general recommendation for decoupling the power supply.

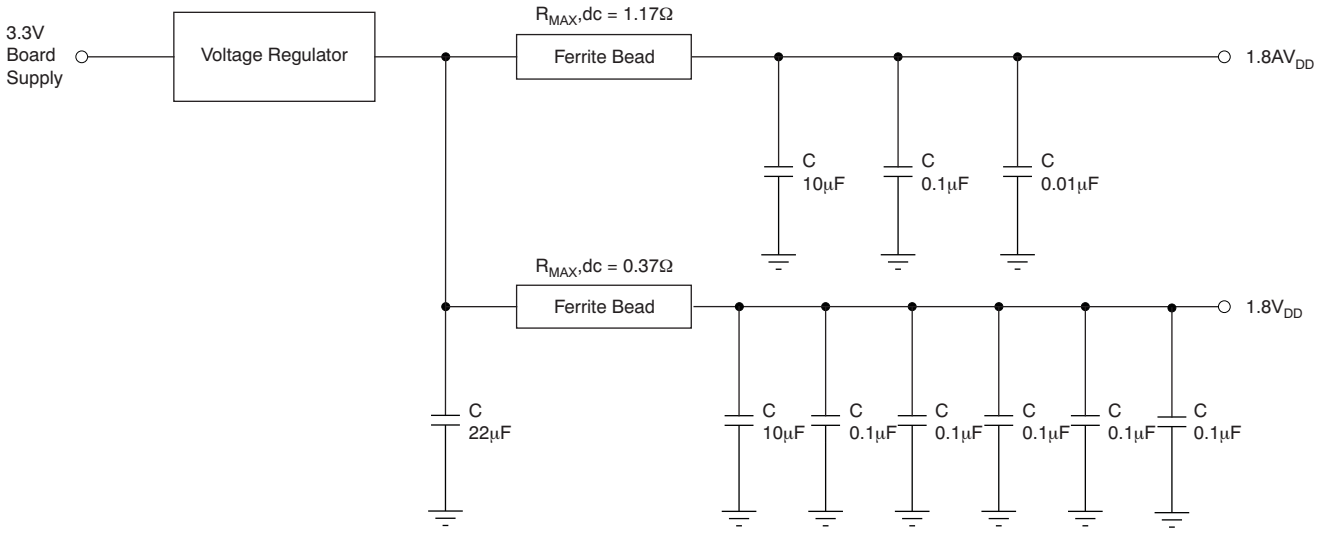

Figure 16. Power-Supply Decoupling Recommendation

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Post Office Box 655303 Dallas, Texas 75265