

Clock Distribution Selection Table

PLL-Based Clock Distribution Circuit Products

Device	Description	# Pins/Pkg	Input Level	Output Level	Frequency (MHz)	V _{CC} (V)	Jitter (Peak-to-Peak [P-P] or Cycle-to-Cycle [C-C])	Phase Error ¹	Output Skew (max) (ps)	Char. Temp. (°C)
CDC5801	Multiplier/divider with programmable delay and phase alignment	24/SSOP	LVC MOS	LVPECL/LVDS/LVTTL	150 to 500/12.5 to 62.5	3.3	P-P: PA bypassed = 40 ps, PA active = 70 ps, Division mode = 75 ps	–	–	–40 to 85
CDC7005 ²	Jitter cleaner, 5 LVPECL outputs, synchronizer, programmable divider	64/BGA	LVC MOS	LVPECL	10 to 800	3.3	–	–	200	–40 to 85
CDC509	1:9 PLL clock	24/TSSOP	LV TTL	LV TTL	25 to 125	3.3	P-P: ±100 ps (>66 MHz)	100/+480 ps (typ)	200	0 to 70
CDC516	1:16 PLL clock	48/TSSOP	LV TTL	LV TTL	25 to 125	3.3	P-P: ±100 ps (>66 MHz)	–80/+400 ps (typ)	200	0 to 70
CDC536	1:6 PLL clock with 1/2x or 2x output, 3-state outputs	28/SSOP	TTL	LV TTL	25 to 100	3.3	P-P: 200 ps	±500 ps	500	0 to 70
CDC582	1:12 LV diff PECL with 1/2x or 2x output	52/TQFP	LVPECL	LV TTL	25 to 100	3.3	P-P: 200 ps	±500 ps	500	0 to 70
CDC586	1:12 clock with 1/2x or 2x output, 3-state outputs	52/TQFP	LV TTL	LV TTL	25 to 100	3.3	P-P: 200 ps	±500 ps	500	0 to 70
CDC857-2/-3	1:10 SSTL-2 differential clock	48/TSSOP	SSTL-2/LV TTL	SSTL-2	66 to 167	2.5	P-P: 75 ps (100 to 167 MHz) C-C: 65 ps (100 to 167 MHz)	±150 ps	100	0 to 85
CDC2509B ³	1:9 PLL clock with SSC	24/TSSOP	LV TTL	LV TTL	25 to 125	3.3	P-P: ±80 ps (66 to 100 MHz)	±200 ps	200	0 to 70
CDC2509C ³	1:9 PLL clock with SSC	24/TSSOP	LV TTL	LV TTL	25 to 125	3.3	C-C: max 100 ps (66 to 100 MHz)	±150 ps	200	0 to 85
CDC2510B ³	1:10 PLL clock with SSC	24/TSSOP	LV TTL	LV TTL	25 to 125	3.3	P-P: ±80 ps (66 to 100 MHz)	±200 ps	200	0 to 70
CDC2510C ³	1:10 PLL clock with SSC	24/TSSOP	LV TTL	LV TTL	25 to 125	3.3	C-C: max 100 ps (66 to 100 MHz)	±150 ps	200	0 to 85
CDC2516 ³	1:16 PLL clock	48/TSSOP	LV TTL	LV TTL	25 to 125	3.3	P-P: ±100 ps (>66 MHz)	–700/+180 ps (typ)	200	0 to 70
CDC2536 ³	1:6 PLL clock with 1/2x or 2x output, 3-state outputs	28/SSOP	TTL	LV TTL	25 to 100	3.3	P-P: 200 ps	±500 ps	500	0 to 70
CDC2582 ³	1:12 LV diff PECL PLL clock with 1/2x or 2x output	52/TQFP	LVPECL	LV TTL	25 to 100	3.3	P-P: 200 ps	±500 ps	500	0 to 70
CDC2586 ³	1:12 PLL clock with 1/2x or 2x output, 3-state outputs	52/TQFP	TTL	TTL	25 to 100	3.3	P-P: 200 ps	±500 ps	500	0 to 70
CDCV850	1:10 PLL clock for DDR apps, SSC compatible with two-line serial interface	48/TSSOP	SSTL-2/universal	SSTL-2	60 to 140	2.5	C-C: ±30 ps (100 to 133 MHz)	–50/+180 ps (133 MHz)	75	–40 to 85
CDCV855	1:4 (plus feedback pair) PLL differential clock for DDR apps, SSC	28/TSSOP	SSTL-2/LV TTL	SSTL-2	60 to 180	2.5	C-C: ±50 ps (100 to 180 MHz)	±100 ps (100 to 180 MHz)	50	–40 to 85
CDCV857	1:10 PLL differential clock for DDR apps, SSC	48/TSSOP	SSTL-2/LV TTL	SSTL-2	60 to 200	2.5	C-C: ±75 ps (100 to 200 MHz)	±100 ps (66 to 167 MHz)	75	0 to 85
CDCV857A	1:10 PLL differential clock for DDR apps, SSC	48/TSSOP 56/μBGA ⁴	SSTL-2/LV TTL	SSTL-2	60 to 180	2.5	C-C: ±50 ps (100 to 180 MHz)	±100 ps (100 to 180 MHz)	75	0 to 85
CDCV857B	1:10 PLL differential clock driver for DDR apps, SSC	48/TSSOP 56/μBGA ⁴	SSTL-2/LV TTL	SSTL-2	60 to 200	2.5	C-C: ±50 ps (100 to 200 MHz)	±50 ps (min/max) (100 to 200 MHz)	70 (typ)	–40 to 85
CDCVF2505 ³	1:5 PLL clock driver for general-purpose, SSC	8/TSSOP/ SOIC	LV TTL	LV TTL	24 to 200	3.3	C-C: 70 ps (typ) (66 to 200 MHz)	–	150	–40 to 85
CDCVF25081 ³	1:8 low-power PLL clock with two banks, SSC	16/TSSOP/ SOIC	LV TTL	LV TTL	10 to 200	3.3	C-C: ±100 ps (66 to 200 MHz)	±150 ps (66 to 200 MHz)	150	–40 to 85
CDCVF2509 ³	1:9 low-power PLL clock for PC 133 and beyond apps, SSC	24/TSSOP	LV TTL	LV TTL	50 to 175	3.3	C-C: 65 ps (typ) (100 to 166 MHz)	±125 ps (66 to 166 MHz)	100	0 to 85

¹For more information regarding test conditions used to obtain measurements, see data sheets at www.ti.com/clocks

²Available 1Q03

⁴μBGA = MicroStar BGA™

³With series output resistors

⁵Rambus signaling levels

(Continued on the back)

PLL-Based Clock Distribution Circuit Products (Continued)

Device	Description	# Pins/Pkg	Input Level	Output Level	Frequency (MHz)	V _{CC} (V)	Jitter (Peak-to-Peak [P-P] or Cycle-to-Cycle [C-C])	Phase Error ¹	Output Skew (max) (ps)	Char. Temp. (°C)
CDCVF2510 ³	1:10 low-power PLL clock driver for PC 133 and beyond apps, SSC	24/TSSOP	LVTTTL	LVTTTL	50 to 175	3.3	C-C: 65 ps (typ) (100 to 166 MHz)	±125 ps (66 to 166 MHz)	100	0 to 85
CDCVF25084 ²	1:8 low-power 4x multiplier with two banks, SSC	16/TSSOP	LVTTTL	LVTTTL	10 to 180	3.3	C-C: ±100 ps (66 to 180 MHz)	–	150	–40 to 85
CDCR61A ⁵	400-MHz Direct Rambus™ clock generator-lite, SSC	16/TSSOP	CMOS	RSL ⁵	300/400	1.8/ 3.3	C-C: 100 ps (400 MHz)	–	–	0 to 85
CDCR83 ⁵	400-MHz Direct Rambus clock generator, SSC	24/SSOP	CMOS	RSL ⁵	267 to 400	3.3	C-C: 50 ps (400 MHz)	±100 ps	–	0 to 85
CDCFR83 ⁵	533-MHz Direct Rambus clock generator, SSC	24/SSOP	CMOS	RSL ⁵	267 to 533	3.3	C-C: 40 ps (533 MHz)	±100 ps	–	0 to 85

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²Available 1Q03

⁴μBGA = MicroStar BGA™

³With series output resistors

⁵Rambus signaling levels

Buffer-Based Clock Distribution Circuit Products

Device	Description	# Pins/Pkg	Input Level	Output Level	Frequency	V _{CC} (V)	Propagation Delay	Output Skew	Char. Temp. (°C)
CDCLVP110	1:10 LVPECL/HSTL with selectable input clock	32/LQFP	LVPECL/HSTL	LVPECL	0 to 3.5 GHz	2.5/3.3	230 to 370 ps	30 ps	–40 to 85
CDCLVD110	1:10 programmable LVDS clock	32/TQFP	LVDS	LVDS	0 to 900 MHz	2.5	3 ns (max)	30 ps (typ)	–40 to 85
CDCVF111	1:9 diff LVPECL clock	28/PLCC	LVPECL	LVPECL	0 to 650 MHz	3.3	450 to 600 ps	50 ps	0 to 70
CDC208	Dual 1:4 fanout, 3-state outputs	20/SOIC	TTL	CMOS	0 to 60 MHz	5	6.6 to 10.2 ns	1 ns	–40 to 85
CDC318A	1:18 clock with I ² C control interface	48/SSOP	LVTTTL	LVTTTL/TTL	0 to 100 MHz	3.3	1.2 to 4.5 ns	250 ps	0 to 70
CDC319	1:10 clock with I ² C control interface	28/SSOP	LVTTTL	LVTTTL/TTL	0 to 100 MHz	3.3	1.2 to 3.6 ns	250 ps	0 to 70
CDC328A	1:6 fanout with selectable polarity	16/SOIC/SSOP	TTL	TTL	0 to 100 MHz	5	1.5 to 5.0 ns	500 ps	–40 to 85
CDC329A	1:6 fanout with selectable polarity	16/SOIC	TTL	CMOS	0 to 80 MHz	5	1.7 to 5.9 ns	600 ps	–40 to 85
CDC337	1:8 clock with four 1x outputs, four 1/2x outputs, 3-state outputs	20/SOIC	TTL	CMOS	0 to 80 MHz	5	4 to 9 ns	900 ps	–40 to 85
CDC339	1:8 clock with four 1x outputs, four 1/2x outputs, 3-state outputs	20/SOIC/SSOP	TTL	TTL	0 to 80 MHz	5	3 to 9 ns	900 ps	–40 to 85
CDC340	1:8 with fast t _{pd} fanout	20/SOIC	TTL	TTL	0 to 80 MHz	5	2.8 to 4.8 ns	600 ps	0 to 70
CDC341	1:8 with fast t _{pd} fanout	20/SOIC	TTL	TTL	0 to 80 MHz	5	3.1 to 4.9 ns	600 ps	0 to 70
CDC351	1:10 with fast t _{pd} fanout, 3-state outputs	24/SOIC/SSOP	LVTTTL	LVTTTL	0 to 100 MHz	3.3	3 to 4 ns	500 ps	0 to 70
CDC391	1:6 clock with selectable polarity and 3-state outputs	16/SOIC	TTL	TTL	0 to 100 MHz	5	1.5 to 5.0 ns	500 ps	–40 to 85
CDCV304	1:4 fanout for PCI-X and general apps	8/TSSOP	LVTTTL	LVC MOS	0 to 140 MHz	3.3	1.8 to 3.0 ns	100 ps	–40 to 85
CDCVF2310 ¹	1:10 clock with 2 banks for general-purpose apps	24/TSSOP	LVTTTL	LVTTTL	0 to 170 MHz (V _{DD} = 2.5 V) 0 to 200 MHz (V _{DD} = 3.3 V)	2.5/3.3	1.3 to 2.8 ns (V _{DD} = 2.5 V) 1.5 to 3.5 ns (V _{DD} = 3.3 V)	100 ps @ 3.3 V 170 ps @ 2.5 V	–40 to 85
CDC2351 ¹	1:10 with fast t _{pd} fanout, 3-state outputs	24/SOIC/SSOP	LVTTTL	LVTTTL	0 to 100 MHz	3.3	3.6 to 4.8 ns	500 ps	0 to 70

For more information regarding test conditions used to obtain measurements, see data sheets at www.ti.com/clocks

¹With series output resistors

For application questions, email cdcapp@list.ti.com

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