CC981H Sensium™ User's Guide

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1 Device Description

The Sensium™ CC981H is an ultralow power wireless enabled sensor interface and transceiver platform for a wide range of applications in the medical and professional healthcare area. The device includes a reconfigurable sensor interface, digital block with embedded 8051 microprocessor , power efficient hardware MAC, and an RF transceiver. On-chip program and data memory permits local processing of signals which can significantly reduce the transmit data payload. The CC981H together with appropriate external sensors provides ultralow power monitoring of vital signs such as heart rate, temperature, and physical activity. It can also interface to pressure sensors, and includes a temperature sensor on chip.

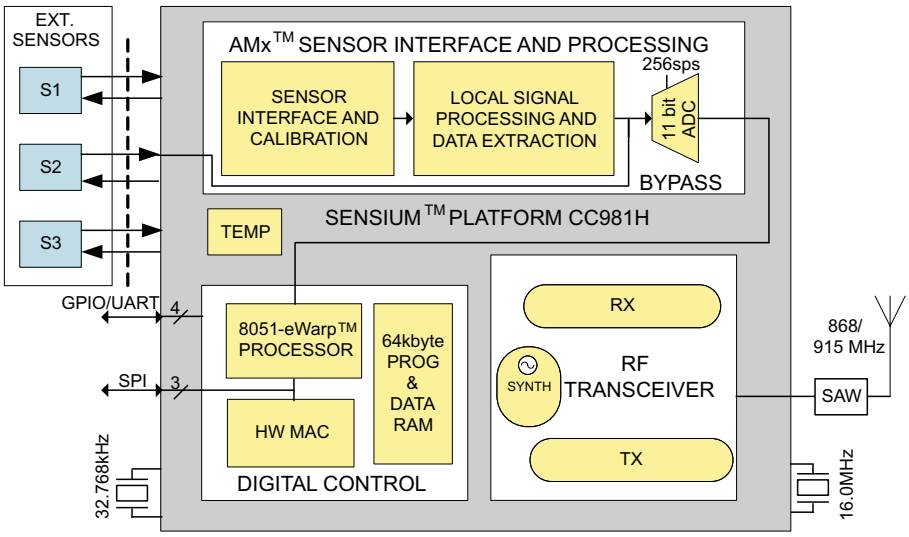


Figure 1. CC981H Block Diagram

1.1 16MHz and 32.768KHz crystals

The Sensium™ uses 2 crystals. A low power 32.768kHz oscillator maintains timing accuracy particularly during sleep mode. This is needed to ensure the Base station and target station can communicate without losing frames and prolonging communication times. This oscillator is always on. The 16MHz crystal is used for the transceiver synthesiser and also by the CPU for customer defined application processing. The 16MHz crystal is normally powered down when the radio or application CPU processing is not required.

Note: the 16MHz crystal should have a system (i.e., absolute + temperature) tolerance of ±15ppm over the required operating temperature range in both the target and Base station. The tolerance can be skewed so the Base station 16MHz crystal could have a tighter system tolerance of say ±10ppm allowing the targets to have a more relaxed system tolerance of ±20ppm. The Sensium™ is designed for use with a 16MHz crystal specified with a 6pF load capacitance. If a crystal intended for a different load capacitance is used this will result in a small deviation of the crystal frequency from 16MHz. This will not be noticeable if the same type of crystal at a similar temperature is used at both ends of the link but will mean a small deviation in the RF frequency. For this latter reason it is best to use 16MHz crystals designed for operation with 6pF load capacitance.

1.2 Boot Loader

There is a boot loader in ROM on the Sensium™. On power up the boot ROM configures the Sensium™ SPI as a master and loads the program from an external EEPROM using GPIO3 as the chip select. The boot ROM clocks the SPI at 500KHz to download the program from the external EEPROM. The first two bytes in the EEPROM tell the boot loader the number of bytes to load. The boot loader will work with the following EEPROMs:

a. Microchip 25AA256SN (surface mount 256kbit EEPROM)
b. Microchip 25AA256-I/P (8/PDIP)

1.3 GPIO Ports

The Sensium™ includes 4 GPIO ports on chip GPIO0 to GPIO3. GPIO0 and1 can be configured as a UART using bit SEL_UART of register SIGMUX. The boot loader uses GPIO3 as the SPI EEPROM chip select. The GPIO ports are controlled by register P2 and have weak pull ups (i.e. set the GPIOs to logic 1 if they are used as inputs). The Sensium™ can monitor the GPIO ports for a change of state using the CPU clocked at a slow clock speed.

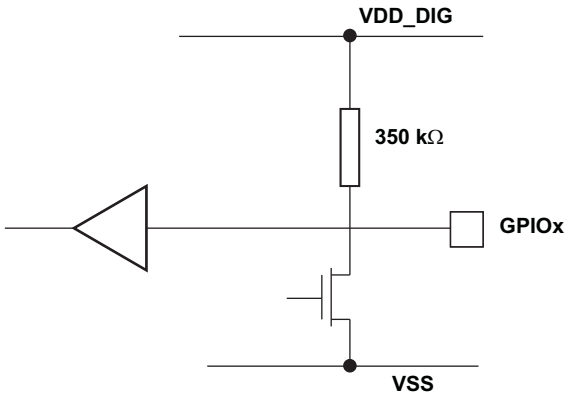


Figure 2. GPIOx on Chip Circuitry

NOTE:

Unused GPIOs should be set to logic 1 to minimize leakage current through the 350kΩ on chip weak pull up resistors.

The on chip weak pull resistors are not strong enough to drive some loads. In particular, some bidirectional logic level converters need to be driven harder for example to avoid the logic level converter unintentionally forcing a logic 0 on a GPIO set to output a logic 1.

1.4 XDATA

Sensor data is stored in the XDATA memory. The proportion of the total 64kbyte RAM used as XDATA can be configured by bits SRAM_SPLIT in register MAC_R12. The amount of memory required for the sensor data is defined in the source code in the TOMAC buffer. The location of this memory is allocated by the compiler.

1.5 SPI Bus

The Sensium™ includes an SPI bus. After a power on reset, the BootROM configures the Sensium™ into SPI master mode and downloads the program from an external EEPROM. The boot loader uses GPIO3 as the SPI EEPROM chip select. A logic level converter is required to interface the 1V logic Sensium SPI lines to the external EEPROM. After the program has been downloaded, the SPI can be either left in SPI master or switched under firmware control to SPI slave mode.

Sensium in slave mode:

- The Sensium has to be switched by the Sensium firmware into SPI slave mode.
- Note there is no SPI CS pin (chip select pin) on the Sensium™, so in slave mode the Sensium™ must be the only slave device on the SPI bus. The Sensium™ as an SPI slave outputs data on the SDO line on every SPI clock signal received.
- If there are multiple slave devices on the SPI bus, the slave Sensium SPI pins need to be isolated when the slave Sensium™ is not being addressed; otherwise, the slave Sensium™ clashs with other slave devices on the SPI bus.

1.6 UART

The Sensium™ includes a UART. This is typically used to connect to UART to USB driver chips in the HDK development kits or to communicate with other system processors. GPIO0 and1 can be configured as a UART using bit SEL_UART of register SIGMUX. A logic level converter is required to interface the 1V logic Sensium UART lines to other devices operating at higher voltage. Note: if the Sensium™ CPU clock is changed then the UART baud rate also changes. In particular, if the CPU clock is changed part way through receiving a byte via the UART, the UART timing is in error. The UART is typically used in Sensium basestations where the CPU is clocked at 16MHz. The Sensium example code is designed for UART operation with the CPU clock set to 16MHz.

2 Sensor Modes and Configuration

The interface circuitry is targeted towards sensors which are either commercially available or in advanced stages of development. These sensors are particularly attractive due to their small size, low cost, and suitability for external or implanted use which makes them compatible with the high-level requirements of the Sensium™ platform. However, all sensor types exhibit variations in characteristics due to manufacturing tolerances, thus some means of calibration needs to be included.

The block diagram illustrates the basic architecture of the front-end AMx interface block The signal processor block contains micro-power signal processing circuitry including amplification and filtering, level detection, reference generation and analogue-to-digital conversion.

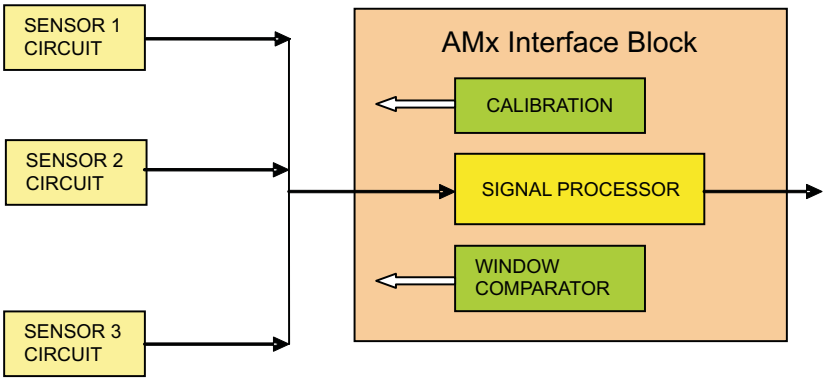


Figure 3. Block Diagram of the Sensor Interface Circuit

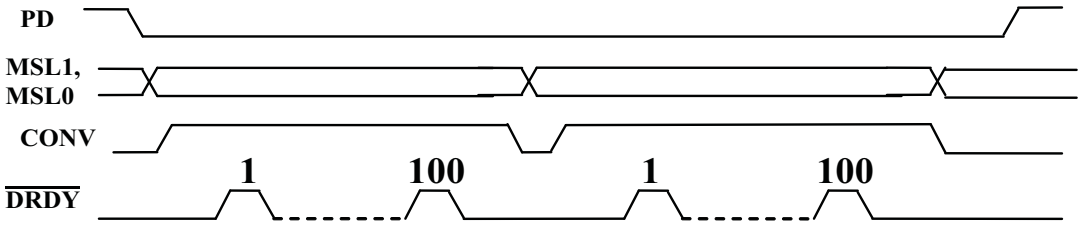
The interface is optimised to operate from a 32.768kHz clock signal which is provided by the watch crystal oscillator circuit. The interface operates from a 1.5V battery and can work down to 1.08V. The modes of operation and combinations of the interface are as follows, selected by the configuration register matrix:

- Mode 0 — ISFET (S1), thermal (ext) (S3)
- Mode 1 — ISFET (S1), thermal (int) (S3)
- Mode 2 — ISFET (S1)
- Mode 3 — AMPERO_N (S1), AMPERO_P (S2), thermal (ext) (S3)
- Mode 4 — AMPERO_N (S1), AMPERO_P (S2), thermal (int) (S3)
- Mode 5 — AMPERO_N (S1), thermal (ext) (S3)
- Mode 6 — AMPERO_N (S1), thermal (int) (S3)
- Mode 7 — AMPERO_N (S1)
- Mode 8 — Not used
- Mode 9 — ECG (S1), temperature (ext) (S3)
- Mode 10 — ECG (S1), temperature (int) (S3)
- Mode 11 —ECG (S1)
- Mode 12 — thermal (ext) (S3)
- Mode 13 — thermal (int) (S3)
- Mode 14 — pressure (S1)
- Mode 15 — AMPERO_P (S2), thermal (ext) (S3)
- Mode 16 — AMPERO_P (S2), thermal (int) (S3)
- Mode 17 — AMPERO_P (S2)
- Mode 18 — ADC (S1)

Depending on the mode selected, up to 3 of the on chip sensor interfaces are configured with programmable bias settings and sampled. Each sensor input is multiplexed in turn to the single on chip ADC. There is a short delay (tso) when switching from one sensor input to the next. tso is the time it takes to flush the ADC digital filter when switching from one analog input to another. It is programmable to 60ms, 80mS, 120 or 160mS. See register TARGET_REC_IN_R18. The default used is 80mS.

The sample rate, number of samples and interval for each sensor interface is programmable. The Sensium™ configurator allows the sensor mode to be configured in Base station mode – the Base station Sensium™ then configures the target Sensium™ by sending a BSENDCFG message over the radio.

For modes where more than 1 sensor interface is used, care needs to be taken when configuring the timing intervals for the different sensor interfaces. For example, in mode 9 ECG and external temperature, if the time interval for the ECG is set to 5 seconds with 1000 samples taken at 256sps (approx 4 seconds), then setting the temperature sensor interface to a time interval of 1 second would cause a clash, but setting the temperature time interval to 5 or multiples of 5seconds would be feasible. The Sensium™ configurator includes a *Show sensor interface time usage feature*, which graphically illustrates the SI timing based on the SI settings selected.

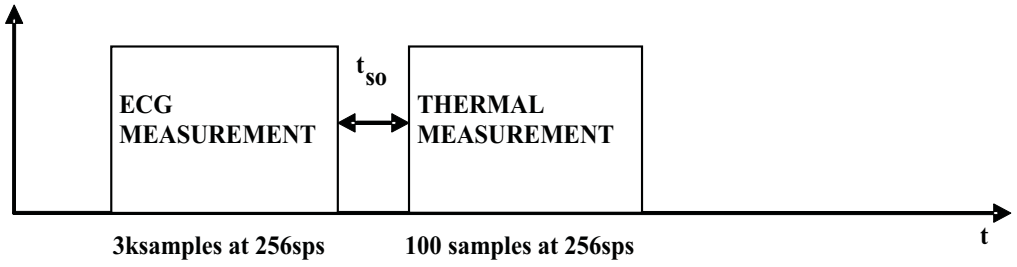


Timing diagram — Modes 2, 7, 11, 12, 13, 14, 17, and 18 with one sensor interface selected.

For SI modes using only 1 sensor input, a continuous sampling option is available.

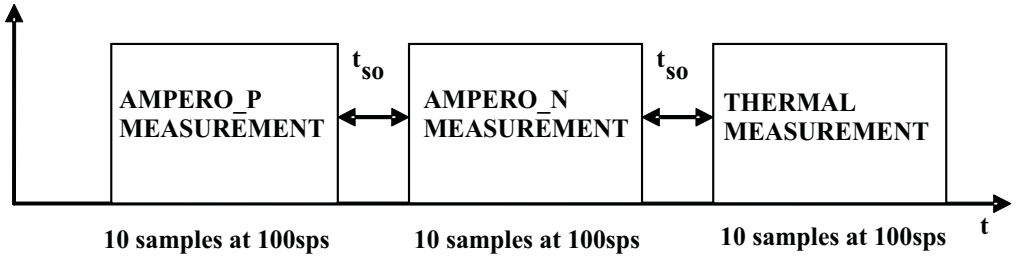
From the 3 seconds of ECG measurement, the user can determine the instantaneous heart rate and from the continuous stream, the user may apply a template to recognize a particular arrhythmia.

Timing Diagram - Modes 0, 1 ,5, 6, 9, 10, 15,16 with 2 sensor interfaces selected



tso — switch over time (time required before the first valid thermal reading can be taken). This will be defined in terms of number of cycles of 32.768kHz clock and is approximately 50ms min.

Timing Diagram — Modes 3, 4 with 3 sensor interfaces selected.



2.1 Sensor Interface Operation

The sensor interface has three operating states. These are start-up, conversion, and sleep. When power is first applied, the interface enters the start-up state. The first step is a power-on reset, which resets all of the logic in the interface. After the power-on reset, the interface enters the wake-up period. This allows the interface circuits (which are operating with low currents) to reach a stable bias condition prior to entering into the conversion states. Execution of input commands will not occur until the complete wake-up period has elapsed. If no command is given, the interface enters standby mode.

2.1.1 Conversion

Signal measurement is implemented using micropower amplification, filtering and analogue to digital conversion (ADC) circuitry. The ADC measures low level, low frequency (dc to 128Hz) signals, and operates on average with nanowatt power consumption. The ADC is a 11-bit converter sampling at a Nyquist rate of 256Hz, with three internal differential input channels selectable via a three-way differential multiplexer.

The conversion state can be entered at the end of the calibration cycle, or whenever the interface is idle in the standby mode. If CONV is taken high, the converter begins a conversion upon completion of the calibration period. The interface will perform a conversion on whichever input channel is selected by the MSL0 and MSL1 inputs when CONV transitioned high. Table 1 shows the multiplexer channel selection truth table for MSL0 and MSL1.

Table 1. Multiplexer Truth Table

MSL1	MSL0	Channel Selected
0	0	VIN1+, VIN1-
0	1	VIN2+, VIN2-
1	0	VIN3+, VIN3-

MSL1 and MLS0 are latched internally on a rising edge of CONV. If CONV is left high, continuous conversion will be performed on one channel at the maximum rate (256 samples/sec).

2.1.2 Amperometric Sensor 3V Supply

A 3V supply capable of delivering a low current (≈4μA) is required for the p and n type amperometric sensor interfaces. This supply voltage is generated internally from the 1V battery using a capacitive based dc-dc converter (Vboost). The ISFET interface also needs a 3V supply but this requires higher current (≈200μA) and must be supplied externally.

2.1.3 Sleep Mode

All blocks will be set into the off state so that no power is taken in this mode. The MAC will be functional and can transmit/receive data from XDATA and the radio independently of the sensor state.

3 Clock Domain

The clock generation unit (CGU) on the Sensium™ has 2 frequency domains A fast clock frequency domain based on the 16MHz crystal and a slow frequency domain derived from the 32.768kHz watch crystal. Switching to a fast clock ie a clock speed higher than 32kHz requires the 16MHz crystal to be switched on. The 16MHz VCXO takes 5ms worst case to turn on and settle. The CGU is controlled by settings in the SFR registers CLKSEL (0x8C) and CLKCON (0x9E) in SFR bank 0. The 32kHz watch crystal is on all the time and the slow clocks derived from this are used for controlling wakeup times for the MAC and the sensor interface. The ADC in the sensor interface is supplied by the 32kHz clock from the watch crystal. The 16MHz fast clock domain is switched on when the transceiver is active or local processing by the CPU is required.

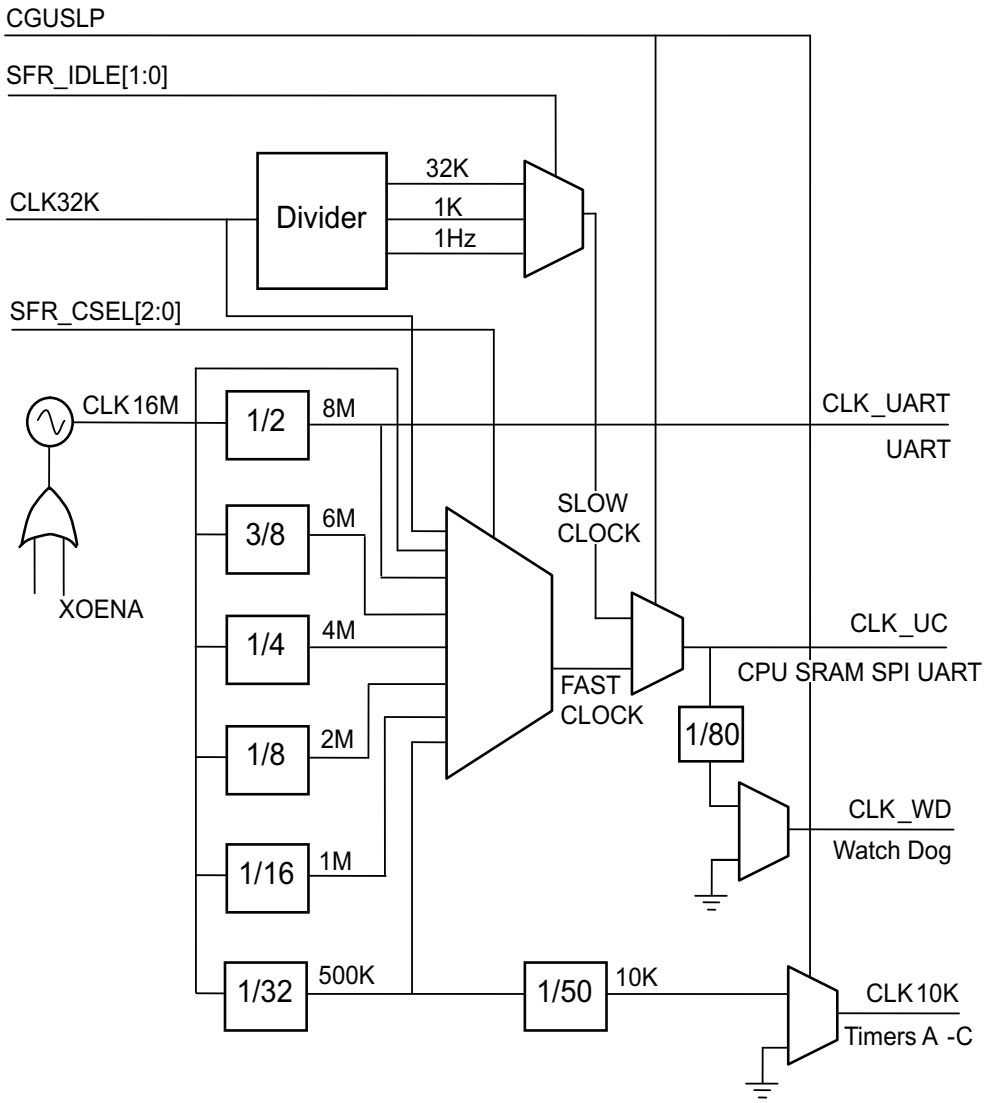


Figure 4. CLOCK GENERATION UNIT CGU

Clock Select Register					CLKSEL			Read/Write
Addr.	Bit7					Bit1	Bit0	R/W
0x8C	SLPEN	WKPEN	SIEN	FXO	CGUSLP	–	Reserved Write 00	R/W

This is a Bank 0 register. Default setting CLKSEL = 0x00

SLPEN	1	Turn off 16 MHz Crystal to deactivate the Fast Clock (Disable XOENA)
	0	No effect
WKPEN	1	Turn on 16 MHz Crystal to activate the Fast Clock
	0	No effect
SIEN		Sensor Interface Enable bit. Normally accessed via User code in the SI_Power_Control interrupt
	1	Turn on Sensor Interface
	0	Turn off Sensor Interface
FXO		Force XOENA (16MHz clock enable). This bit holds XOENA high when set.
	1	XOENA always asserted
	0	XOENA controlled normally
CGUSLP		Clock Domain Select bit. This controls whether the processor clock comes from the Fast (16 MHz) clock domain or the Slow (32 KHz) clock domain
	1	Slow Clock Domain
	0	Fast Clock Domain (Note: the 16MHz crystal must be on)
		When CGUSLP is 0, the selected clock is synchronized to the 16MHz clock. So if one selects 32kHz in this mode, this is also synchronized to the 16MHz clock. This means that when this bit is 0, the 16MHz XTAL must be turned on. If it is turned off, the user will lose control of the chip.
Reserved Bits 0 and 1	00	Always set to 0

3.1 Turning the 16MHz XTAL On and Off

Before turning the 16MHz XTAL off, the user must change to the slow clock domain, set CGUSLP=1 (Slow ck domain) before turning the 16MHz XTAL off by setting the SLPEN bit. To turn it back on, clear the SLPEN bit, then set the WKPEN bit. The user should then clear CGUSLP before changing to any clock in the 16MHz domain. Note the 16MHz VCXO takes 5ms worst case to turn on and settle.

Example Code to switch to Slow Clock domain and turn off 16 MHz Crystal.

```
SFR_BANK0;

/* Setup for 32 KHz in Slow domain & 16 MHz in Fast domain  */
        CLKCON = 0x47;

/* Switch to Slow Clock Domain                              */
        CLKSEL |= 0x08;

/* Allow clocks to settle. Good practice                    */
    _    nop_();
    _    nop_();
    _    nop_();
    _    nop_();


/* Turn off the 16 MHz Xtal
    CLKSEL &= 0x3F;
    CLKSEL |= 0x80; */
```

Example Code to turn on the 16 MHz Crystal and switch back to the Fast Clock domain.

```
/* Turn Xtal back on again      */

    CLKSEL &= 0x3F;
    CLKSEL |= 0x40;

/* Switch to Fast Clock Domain */
    CLKSEL &= 0xF7;

/* Allow clocks to settle. Good practice                    */
    nop_();
    nop_();
    nop_();
    nop_();
```

Clock Control Register				CLKCON						Read/Write
Addr.	Bit7							Bit0	Reg.	R/W
9Eh	SFTRST	BTMD	–	SRSLP	RFSLP	CSEL2	CSEL1	CSEL0	CLKCTR	R/W

This is a Bank 0 register. Default setting CLKCON = 0x47

SFTRST	1	Writing to this bit will generate a software reset, after 3 microprocessor clock cycles
	0	The reset value, read of this bit will always get 0
BTMD		Boot Mode, bit to specify the program source after reset. This bit is reset only by hardware reset.
	1	Boot from program RAM
	0	Boot from ROM loader
SNRSLP	1	Set Sensor Platform to sleep mode
	0	Set Sensor Platform is in normal mode
RFSLP	1	RF Platform is in sleep mode
	0	Clock for RF Platform is turned on
CSEL(2..0)		Clock frequency for 8051 core SRAM and SPI
	7	16MHz
	6	8MHz
	5	6MHz
	4	4MHz
	3	2MHz
	2	1MHz
	1	0.5MHz
	0	32 KHz

4 SFR Register Description

4.1 Register Banks

The Sensium™ contains 2 SFR register banks which can be written to and read from by the 8051 processor and the MAC. Register bank 0 includes the RF, MAC and Sensor Interface control registers. Register bank 1 includes TARGET REC IN, TARGET REC OUT and channel select registers. The Target REC IN and OUT registers enable a Sensium™ Base station to configure and keep track of the configuration status of multiple target Sensium™ devices. Only one register bank can be addressed at a time. To change the register bank selected, bit 7 has to be set in SFR BSEL (this is register 8Fh and is accessible from both register banks). Use the macro SFR_BANKx to select the SFR bank. It is easier to use and replaces the assembly code BSEL command.

- SFR_BANK0 is equivalent to BSEL &=0x8F
- SFR_BANK1 is equivalent to BSEL &=0x8F

4.2 Register Map

The following tables show registers which are allowed to be accessed by the user software. Note that there are more registers but access might damage circuit or might disturb the correct function of the device. Notice that bits which are not defined must be cleared!

Table 2. Overview of Special Function Registers Bank 0

Addr	Name	R/W	Description	Reset Value
80h				
81h	SP	R/W	Stack pointer	00h
82h	DPL	R/W	Data page pointer low byte	00h
83h	DPH	R/W	Data page pointer high byte	00h
84h				
85h	SI_R0	R/W	Channel A control voltage settings	00h
86h	SI_R1	R/W	Channel B control voltage settings	00h
87h	PCON	R/W	Power Control register	00h
88h	SIGMUX	R/W	GPIO/UART select	00h
89h	SI_R2	R/W	Channel A ISFET current settings	00h
8Ah	SI_R3	R/W	Channel B ISFET current settings	00h
8Bh	ECON	R/W	Enable clock register	00h
8Ch	CLKSEL	R/W	Clock Frequency selection register	00h
8Dh	WDTCON	R/W	Watchdog Register	00h
8Eh	WDTOVL	R/W	Watchdog Register	FFh
8Fh	BSEL	R/W	Register for bank switching	00h
90h				
91h	SI_R4	R/W	Channel A Measuring period settings	00h
92h	SI_R5	R/W	Channel B Measuring period settings	00h
93h	SI_R6	R/W	Channel A Measuring capacitor settings	
94h	SI_R7	R/W	Channel B Measuring capacitor settings	
95h	TACON	R/W	Timer A configuration	00h
96h	TAL	R/W	Timer A low byte	00h
97h	TAH	R/W	Timer A high byte	00h
98h	TBCON	R/W	Timer B configuration Register	00h
99h	TBL	R/W	Timer B low byte	00h
9Ah	TBH	R/W	Timer B high byte	00h
9Bh	TCCON	R/W	Timer C configuration Register	00h
9Ch	TCL	R/W	Timer C low byte	00h
9Dh	TCH	R/W	Timer C high byte	00h
9Eh	CLKCTR	R/W	Clock Control register	00h
9Fh	IREQ0	R/W	interrupt request register 0	00h
A0h	P2	R/W	GPIO pins	00h
A1h				
A2h	EOR	R/W	Extended operations	00h
A3h	SI_R8	R/W	Channel A and B mode settings, Channel A and B ISFET ref voltage settings	00h
A4h	SI_R9	R/W	Channel A and B Circuit Enables Channel A and B Measurement Enables Channel A and B Test Mode 1 Enable Channel A and B Test Mode 2 Enable	
A5h	SI_R10	R/W	Test current settings	00h
A6h	SI_R11	R/W	Test Current Settings	00h
A7h	SI_R12		Spare	
A8h	IE0	R/W	Interrupt enable Register	00h

Table 2. Overview of Special Function Registers Bank 0 (continued)

Addr	Name	R/W	Description	Reset Value
A9h	IREQ1	R/W	Interrupt request Register 1	00h
AAh	SI_R13	R/W	Sensor Config Mode setting, Gain Setting for ECG Preamplifier, Bias Current for SC LPF	00h
ABh	SI_R14	R/W	Gain Setting for pressure amplifier, Multiplexer selection ADC, Calibration Control function	00h
ACh	SI_R15	R/W	General Purpose Analog Input 1 bias voltage and gain	00h
ADh	SI_R16	R/W	General Purpose Analog Input 2 bias voltage and gain	00h
AEh	SI_R17	R/W	General Purpose Analog Input 3 bias voltage and gain	00h
AFh	SI_R18	R/W	ALARMHI(7:0)	00h
B0h				
B1h	SI_R19	R/W	ALARMHI(11:8), ALARMLO(3:0)	00h
B2h	SI_R20	R/W	ALARMLO(11:4)	00h
B3h	SI_R21	R	ADC_OUT(7:0)	00h
B4h	SI_R22	R	ADC_OUT(11:8), MSL(1:0)- sensor input, Alarm interrupt readback	00h
B5h	RF_R0	R/W	PD0	FFh
B6h	RF_R1	R/W	PD1	FFh
B7h	RF_R2	R/W	PD2	FFh
B8h	IPL0	R/W	Interrupt Priority low part	00h
B9h	IPH0	R/W	Interrupt Priority high part	00h
BAh	RF_R3	R/W	SY0	17h
BBh	RF_R4	R/W	SY1	00h
BCh	RF_R5	R/W	SY2	00h
BDh	RF_R6	R/W	RF0	04h
BEh	RF_R7	R/W	RF1	04h
BFh	RF_R8	R/W	BB0	07h
C0h	RF_R9	R/W	BB1	04h
C1h	RF_R10	R/W	BB2	00h
C2h	RF_R11	R/W	BB3	00h
C3h	RF_R12	R/W	BB4	00h
C4h	RF_R13	R/W	Test	00h
C5h	RF_R14	R	STAT0	N/A
C6h	RF_R15	R	STAT1	N/A
C7h	RF_R16	R/W	AGC Configuration	00h
C8h	RF_R17	R/W	AGC Configuration	00h
C9h	RF_R18	R/W	AGC Configuration	00h
CAh	RF_R19	R/W	Spare	00h
CBh	RF_R20	R/W	Readback Register	00h
CCh	MAC_R0	R/W		00h
CDh	MAC_R1	R/W		00h
CEh	MAC_R2	R/W		00h
CFh	MAC_R3	R/W		00h
D0h	PSW	R	Program status word	00h
D1h	SATUNE	R/W	UART register	D5h
D2h	MAC_R4	R/W		00h
D3h	MAC_R5	R/W		00h
D4h	MAC_R6	R/W		00h
D5h	MAC_R7	R/W		00h

Table 2. Overview of Special Function Registers Bank 0 (continued)

Addr	Name	R/W	Description	Reset Value
D6h	MAC_R8	R/W		00h
D7h	SCON0	R/W	UART register	00h
D8h	SCON1	R/W	UART register	00h
D9h	SCON2	R	UART register	00h
DAh	SBUF	R/W	UART register	00h
DBh	SASCAL	R/W	UART register	08h
DCh	MAC_R9	R/W		00h
DDh	MAC_R10	R/W		00h
DEh	MAC_R11	R/W		00h
DFh	MAC_R12	R/W		00h
E0h	A	R/W	Accumulator	00h
E1h	SSCTB	W	SSC Register	00h
E2h	SSCRB	R	SSC Register	00h
E3h	SSCCON	R/W	SSC Register	00h
E4h	SSCBRI	R/W	SSC Register	00h
E5h	SSCSTC	R/W	SSC Register	00h
E6h	MAC_R13	R		00h
E7h	MAC_R14	R		00h
E8h	IE1	R/W	Interrupt Enable Register	00h
E9h	MAC_R15	R		00h
Eah	MAC_R16	R		00h
Ebh	MAC_R17	R		00h
Ech	MAC_R18	R/W		00h
Edh	MAC_R19	R/W		00h
Eeh	MAC_R20	R/W		00h
Efh	MAC_R21	R/W		00h
F0h	B	R/W	B Register	00h
F1h	MAC_R22	R/W		00h
F2h	MAC_R23	R/W		00h
F3h	MAC_R24	R/W		00h
F4h	MAC_R25	R		00h
F5h	MAC_R26	R		00h
F6h	MAC_R27	R/W		00h
F7h	MAC_R28	R/W		00h
F8h	IPL1	R/W	Interrupt-Priority low part	00h
F9h	IPH1	R/W	Interrupt-Priority high part	00h
FAh	MAC_R29	R		00h
FBh	MAC_R30	R		00h
FCh	MAC_R31	R/W		00h
FDh	MAC_R32	R/W		00h
FEh	MAC_R33	R		00h
FFh	MAC_R34	R		00h

Table 3. Overview of Special Function Registers Bank 1

Addr	Name	R/W	Description	Reset Value
80h				
81h	SP	R/W	Stack pointer	07h
82h	DPL	R/W	Data page pointer low byte	00h
83h	DPH	R/W	Data page pointer high byte	00h
84h				
85h	SRAM_CNTRL_R15A	R/W		00h
86h	SRAM_CNTRL_R15B	R/W		00h
87h	PCON	R/W	Power Control register	00h
88h	TARGET REC IN _R0	R/W		00h
89h	TARGET REC IN _R1	R/W		00h
8Ah	TARGET REC IN _R2	R/W		00h
8Bh	TARGET REC IN _R3	R/W		00h
8Ch	TARGET REC IN _R4	R/W		00h
8Dh	TARGET REC IN _R5	R/W		00h
8Eh	TARGET REC IN _R6	R/W		00h
8Fh	BSEL	R/W	register for bank-switching	00h
90h				00h
91h	TARGET REC IN _R7	R/W		00h
92h	TARGET REC IN _R8	R/W		00h
93h	TARGET REC IN _R9	R/W		00h
94h	TARGET REC IN _R10	R/W		00h
95h	TARGET REC IN _R11	R/W		00h
96h	TARGET REC IN _R12	R/W		00h
97h	TARGET REC IN _R13	R/W		00h
98h	TARGET REC IN _R14	R/W		00h
99h	TARGET REC IN _R15	R/W		00h
9Ah	TARGET REC IN _R16	R/W		00h
9Bh	TARGET REC IN _R17	R/W		00h
9Ch	TARGET REC IN _R18	R/W		00h
9Dh	TARGET REC IN _R19	R/W		00h
9Eh	TARGET REC IN _R20	R/W		00h
9Fh	IREQO	R/W	interrupt request register 0	00h
A0h	P2	R/W	Port 2 general purpose port	FFh
A1h	TARGET REC IN _R21	R/W		00h
A2h	EOR	R/W	Extended Operations	00h
A3h	TARGET REC IN _R22	R/W		00h
A4h	TARGET REC IN _R23	R/W		00h
A5h	TARGET REC IN _R24	R/W		00h
A6h	TARGET REC IN _R26	R/W		00h
A7h	CH_SEL_R0	R/W	Channel Selection Register	00h
A8h	IEO	R/W	Interrupt enable Register	00h
A9h	IREQ1	R/W	Interrupt request Register 1	00h
AAh	CH_SEL_R1	R/W	Channel Selection Register	00h
ABh	CH_SEL_R2	R/W	Channel Selection Register	00h
ACh	CH_SEL_R3	R/W	Channel Selection Register	00h
ADh	CH_SEL_R4	R/W	Channel Selection Register	00h

Table 3. Overview of Special Function Registers Bank 1 (continued)

Addr	Name	R/W	Description	Reset Value
AEh	CH_SEL_R5	R/W	Channel Selection Register	00h
AFh	CH_SEL_R6	R/W	Channel Selection Register	00h
B0h				
B1h	CH_SEL_R7	R/W	Channel Selection Register	00h
B2h	CH_SEL_R8	R/W	Channel Selection Register	00h
B3h	CH_SEL_R9	R/W	Channel Selection Register	00h
B4h	CH_SEL_R10	R/W	Channel Selection Register	00h
B5h	CH_SEL_R11	R/W	Channel Selection Register	00h
B6h	CH_SEL_R12	R/W	Channel Selection Register	00h
B7h	CH_SEL_R13	R/W	Channel Selection Register	00h
B8h	IPL0	R/W	Interrupt-Priority low part	00h
B9h	IPH0	R/W	Interrupt-Priority high part	00h
BAh	CH_SEL_R14	R/W	Channel Selection Register	00h
BBh	CH_SEL_R15	R/W	Channel Selection Register	00h
BCh	CH_SEL_R16	R/W	Channel Selection Register	00h
BDh	CH_SEL_R17	R/W	Channel Selection Register	00h
BEh	CH_SEL_R18	R/W	Channel Selection Register	00h
BFh	CH_SEL_R19	R/W	Channel Selection Register	00h
C0h	CH_SEL_R20	R/W	Channel Selection Register	00h
C1h	CH_SEL_R21	R/W	Channel Selection Register	00h
C2h	CH_SEL_R22	R/W	Channel Selection Register	00h
C3h	CH_SEL_R23	R/W	Channel Selection Register	00h
C4h	CH_SEL_R24	R/W	Channel Selection Register	00h
C5h	CH_SEL_R25	R/W	Channel Selection Register	00h
C6h	CH_SEL_R26	R/W	Channel Selection Register	00h
C7h	CH_SEL_R27	R/W	Channel Selection Register	00h
C8h	SRAM_CTRL_R0	R/W		00h
C9h	SRAM_CTRL_R1	R/W		00h
CAh	SRAM_CTRL_R2	R/W		00h
CBh	SRAM_CTRL_R3	R/W		00h
CCh	SRAM_CTRL_R4	R/W		00h
CDh	SRAM_CTRL_R5	R/W		00h
CEh	SRAM_CTRL_R6	R/W		00h
CFh	SRAM_CTRL_R7	R/W		00h
D0h	PSW	R	Program status word	00h
D1h	SRAM_CTRL_R8	R/W		00h
D2h	SRAM_CTRL_R9	R/W		00h
D3h	SRAM_CTRL_R10	R/W		00h
D4h	SRAM_CTRL_R11	R/W	Sensor data, BYTE0	00h
D5h	SRAM_CTRL_R12	R/W	Sensor data, BYTE1	00h
D6h	SRAM_CTRL_R13	R/W	Sensor data, BYTE2	00h
D7h	SRAM_CTRL_R14	R/W	Sensor data, BYTE3	00h
D8h	SRAM_CTRL_R15	R/W	Sensor data, BYTE4	00h
D9h	SRAM_CTRL_R16	R/W		00h
DAh	SRAM_CTRL_R17	R/W	mac start address, BYTE0	00h
DBh	SRAM_CTRL_R18	R/W	mac start address, BYTE1	00h

Table 3. Overview of Special Function Registers Bank 1 (continued)

Addr	Name	R/W	Description	Reset Value
DCh	SRAM_CTRL_R19	R/W	Sensor start address, BYTE0	00h
DDh	SRAM_CTRL_R20	R/W	Sensor start address, BYTE1	00h
DEh	SRAM_CTRL_R21	R/W	Sensor end address, BYTE0	00h
DFh	SRAM_CTRL_R22	R/W	Sensor end address, BYTE1	00h
E0h	A	R/W	Accumulator	00h
E1h	SRAM_CTRL_R23	R/W		00h
E2h	TARGET_REC_OUT_R0	R		00h
E3h	TARGET_REC_OUT_R1	R		00h
E4h	TARGET_REC_OUT_R2	R		00h
E5h	TARGET_REC_OUT_R3	R		00h
E6h	TARGET_REC_OUT_R4	R		00h
E7h	TARGET_REC_OUT_R5	R		00h
E8h	IE1	R/W	Interrupt enable Register	00h
E9h	TARGET_REC_OUT_R6	R		00h
EAh	TARGET_REC_OUT_R7	R		00h
EBh	TARGET_REC_OUT_R8	R		00h
ECh	TARGET_REC_OUT_R	R		00h
EDh	TARGET_REC_OUT_R1	R		00h
EEh	TARGET_REC_OUT_R11	R		00h
EFh	TARGET_REC_OUT_R12	R		00h
F0h	B	R/W		00h
F1h	TARGET_REC_OUT_R13	R		00h
F2h	TARGET_REC_OUT_R14	R		00h
F3h	TARGET_REC_OUT_R15	R		00h
F4h	TARGET_REC_OUT_R16	R		00h
F5h	TARGET_REC_OUT_R17	R		00h
F6h	TARGET_REC_OUT_R18	R		00h
F7h	TARGET_REC_OUT_R19	R		00h
F8h	IPL1	R/W	Interrupt-Priority low part	00h
F9h	IPH1	R/W	Interrupt-Priority high part	00h
FAh	TARGET_REC_OUT_R20	R		00h
FBh	TARGET_REC_OUT_R21	R		00h
FCh	TARGET_REC_OUT_R22	R		00h
FDh	TARGET_REC_OUT_R23	R		00h
FEh	TARGET_REC_OUT_R24	R		00h
FFh	TARGET_REC_OUT_R25	R		00h

4.3 RF SFR Registers (Transceiver Static Registers)

There are 21 RF related SFR registers RF_R0 to RF_R20. These are located in register bank 0. Hardware Reset values are hard coded as shown in the following tables. Hardware reset values are not relevant since register settings are loaded from EPROM at hardware reset. HDK (Hardware Development Kit) default values are shown as typical settings for EU usage.

4.3.1 RF_R0 to R3 Transceiver Power Down Control

Table 4. Register RF_R0 Settings Addr: B5h

Bit	Name	Description	R/W	Hardware Reset
0	PD_LNA	Power down LNA	RW	0
1	PD_MIX1	Power down MIX1	RW	0
2	PD_MIX2	Power down MIX2	RW	0
3	PD_BBAMP	Power down BBAMP	RW	0
4	PD_BBFILT	Power down BBFILT	RW	0
5	PD_BBLIM	Power down BBLIM	RW	0
6	PD_RSSI	Power down RSSI	RW	0
7	PD_DEMOD	Power down DEMOD	RW	0

Table 5. Register RF_R1 Settings Addr: B6h

Bit	Name	Description	R/W	Hardware Reset
0	PD_AFC	Power down AFC	RW	0
1	PD_XOFASTSTART	Power down XO fast start circuit	RW	0
2	PD_VCO	Power down VCO	RW	0
3	PD_CP	Power down synthesizer CP	RW	0
4	PD_DIVN	Power down synthesizer DIVN	RW	0
5	PD_DIV4	Power down synthesizer DIV4	RW	0
6	PD_BGPBUF	Power down bandgap buffer	RW	0
7	PD_BBDETECT	Power down detect circuit: AGC mode=01	RW	0

Table 6. Register RF_R2 Settings Addr: B7h

Bit	Name	Description	R/W	Hardware Reset
0	PD_DAC	Power down DAC	RW	0
1	PD_DACFILT	Power down DACFILT	RW	0
2	PD_MIX3	Power down MIX3	RW	0
3	PD_MIX4	Power down MIX4	RW	0
4	PD_PA	Power down PA	RW	0
5	PD_DLY0	PA Enable delay 0	RW	0
6	PD_DLY1	PA Enable delay 1	RW	0
7	GFSK_ENABLE	Enable GFSK BT=1.0 Data Filter	RW	0

Table 7. Register RF_R3 Settings Addr: BAh

Bit	Name	Description	R/W	Hardware Reset
0	PD_BGPTAT	Power down Bandgap PTAT	RW	0
1	PD_BGCTAT	Power down Bandgap CTAT	RW	0
2	PD_BGCON	Power down Bandgap CON	RW	0
3	PD_VCOREG	Power down VCO regulator	RW	0
4	PD_BATTLOW	Power down battery low circuit	RW	0
5	iSYNTH_EN_DLY0	SYNTH_EN delay 0	RW	0
6	iSYNTH_EN_DLY1	SYNTH_EN delay 1	RW	0
7	FORCE_XO_EN	Force XO enable	RW	0

Power down bits are gated with MAC generated dynamic control words. Circuits can only be enabled with the corresponding signal from the MAC (SYNTH_EN, RX_EN or TX_EN) being high.

RF_R0<7:0> = PD0 <7:0> are gated with RX_EN from the MAC.

RF_R1<0> and RF_R1<7> are gated with RX_EN from the MAC.

RF_R1<5:2> are gated with iSYNTH_EN which is a delayed SYNTH_EN from the MAC.

RF_R2<4:0> are gated with TX_EN from the MAC.

RF_R3<4:0> are gated with SYNTH_EN from the MAC.

4.3.2 RF_R4 to R12 Synthesizer, RF and Analogue Base-band Configuration Control

Table 8. Register RF_R4 Settings Addr: BBh

Bit	Name	Description	R/W	Hardware Reset
0	EN_VTUNE_HILO	Enable VCO VTUNE Comparator for Tank select	RW	0
1	SPARE	SPARE	RW	0
2	SPARE	SPARE	RW	0
3	SPARE	SPARE	RW	0
4	SPARE	SPARE	RW	0
5	SPARE	SPARE	RW	0
6	SPARE	SPARE	RW	0
7	SPARE	SPARE	RW	0

Table 9. Register RF_R5 Settings Addr: BCh

Bit	Name	Description	R/W	Hardware Reset
0	SPARE	SPARE	RW	0
1	SPARE	SPARE	RW	0
2	SPARE	SPARE	RW	0
3	SPARE	SPARE	RW	0
4	SPARE	SPARE	RW	0
5	SPARE	SPARE	RW	0
6	CPFSTLCK_OVRD	Charge pump fast lock override	RW	0
7	SYMODE	Select PLL Reference Freq	RW	1

Table 10. Register RF_R6 Settings Addr: BDh

Bit	Name	Description	R/W	Hardware Reset
0	CPISEL<0>	Charge pump current set 0	RW	0
1	CPISEL<1>	Charge pump current set 1	RW	0
2	CPFSTLCK<0>	Charge pump fast lock time 0	RW	
3	CPFSTLCK<1>	Charge pump fast lock time 1	RW	0
4	CPTST<0>	Charge pump test 0	RW	0
5	CPTST<1>	Charge pump test 1	RW	0
6	LK_DLY<0>	Lock Detect delay 0	RW	0
7	LK_DLY<1>	Lock Detect delay 1	RW	0

Table 11. Register RF_R7 (RF0) Settings Addr: BEh

Bit	Name	Description	R/W	Hardware Reset
0	VCOTNK<0>	VCO tank select 0	RW	1
1	VCOTNK<1>	VCO tank select 1	RW	1
2	VCOTNK<2>	VCO tank select 2	RW	1
3	VCOPWR	VCO power control	RW	0
4	SPARE	SPARE	RW	0
5	PA_PWR<0>	PA power control 0	RW	0
6	PA_PWR<1>	PA power control 1	RW	0
7	PA_PWR<2>	PA power control 2	RW	0

Table 12. Register RF_R8 Settings Addr: BFh

Bit	Name	Description	R/W	Hardware Reset
0	LNATNK<0>	LNA tank select 0	RW	0
1	LNATNK<1>	LNA tank select 1	RW	0
2	MIX4TNK<0>	MIX4 tank select 0	RW	0
3	MIX4TNK<1>	MIX4 tank select 1	RW	0
4	SPARE	SPARE	RW	0
5	LNAGAIN_TRIM	LNA Gain Trim	RW	0
6	LNAGAIN	LNA Gain	RW	0
7	BBAMP_GAIN	BBAMP Gain select 0	RW	1

Table 13. Register RF_R9 Settings Addr: C0h

Bit	Name	Description	R/W	Hardware Reset
0	BBFILTTRIM<0>	BBFILT trim select 0	RW	0
1	BBFILTTRIM<1>	BBFILT trim select 1	RW	0
2	BBFILTTRIM<2>	BBFILT trim select 2	RW	0
3	SPARE	SPARE	RW	0
4	SPARE	SPARE	RW	0
5	BBDACFILTTRIM<0>	BBDACFILT trim select 0	RW	0
6	BBDACFILTTRIM<1>	BBDACFILT trim select 1	RW	0
7	SPARE	SPARE	RW	0

Table 14. Register RF_R10 Settings Addr: C1h

Bit	Name	Description	R/W	Hardware Reset
0	RSSI_TRIM<0>	RSSI trim select 0	RW	0
1	RSSI_TRIM<1>	RSSI trim select 1	RW	0
2	RSSI_TRIM<2>	RSSI trim select 2	RW	0
3	SPARE	SPARE	RW	0
4	MOD_CONFIG<0>	FSK modulator configuration 0	RW	0
5	MOD_CONFIG<1>	FSK modulator configuration 1	RW	0
6	MOD_CONFIG<2>	FSK modulator configuration 2	RW	0
7	MOD_CONFIG<3>	FSK modulator configuration 3	RW	0

Table 15. Register RF_R11 Settings Addr: C2h

Bit	Name	Description	R/W	Hardware Reset
0	AFC_IQ_ACT_CNT<0> >	Preamble found count trigger 0	RW	0
1	AFC_IQ_ACT_CNT<1	Preamble found count trigger 1	RW	0
2	AFC_FD_CNT	AFC target count	RW	0
3	FCMODE_LOW	Width of LEAD pulse FC_LOW	RW	0
4	FCMODE_HIGH	Width of LEAD pulse FC_HI	RW	0
5	DMD_INVERT	Demodulator Output Invert	RW	0
6	AFC_FD_CHK_LOW	Check for too few IQ pulses	RW	0
7	AFC_FD_CHK_HIGH	Check for too many IQ pulses	RW	0

Table 16. Register RF_R12 Settings Addr: C3h

Bit	Name	Description	R/W	Hardware Reset
0	DLL_LENGTH_RDBK	DLL readback length control	RW	0
1	DLL_DELAY	Enable 7 dealys per cell	RW	0
2	DLL_CHNG_MDE	DLL update period change mode	RW	0
3	DLL_RESHAPE	Reshape DLL comparison	RW	0
4	DLL_DELAY2	Enable 8 delays per cell	RW	0
5	SPARE	SPARE	RW	0
6	SPARE	SPARE	RW	0
7	SPARE	SPARE	RW	0

4.3.3 RF_R13 Test Mode Configuration Control

Table 17. Register RF_R13 Settings Addr: C4h

Bit	Name	Description	R/W	Hardware Reset
0	TIN 0	Test mode In select 0	RW	0
1	TIN 1	Test mode In select 1	RW	0
2	TIN 2	Test mode In select 2	RW	0
3	TIN 3	Test mode In select 3	RW	0
4	TOUT 0	Test mode Out select 0	RW	0
5	TOUT 1	Test mode Out select 1	RW	0
6	TOUT 2	Test mode Out select 2	RW	0
7	TOUT 3	Test mode Out select 3	RW	0

4.3.4 RF_R14 to R15 Read-Back Registers

Table 18. Register RF_R14 Status Readout Addr: C5h

Bit	Name	Description	R/W	Hardware Reset
0	DLL_LENGTH<0>		R	N/A
1	DLL_LENGTH<1>		R	N/A
2	DLL_LENGTH<2>		R	N/A
3	DLL_LENGTH<3>		R	N/A
4	DLL_LENGTH<4>		R	N/A
5	VSS	Ground	R	N/A
6	VSS	Ground	R	N/A
7	VSS	Ground	R	N/A

Table 19. Register RF_R15 Status Readout Addr: C6h

Bit	Name	Description	R/W	Hardware Reset
0	RSSI_OUT 0	RSSI output bit 0	R	N/A
1	RSSI_OUT 1	RSSI output bit 1	R	N/A
2	RSSI_OUT 2	RSSI output bit 2	R	N/A
3	VSS	Ground	R	N/A
4	LOCK_DET	PLL Lock detect Output	R	N/A
5	VCOREG_READY	VCO Regulator ready flag	R	N/A
6	BATTERY_LOW	Battery low flag	R	N/A
7	VSS	Ground	R	N/A

For the RSSI bits, RSSI_OUT<0:2> 000 represents a small signal, and 111 represents a large signal. To estimate the absolute received signal strength, the receiver gain settings (LNA_GAIN and BBAMP_GAIN see register RF_R20) needs to be taken into account. The RSSI step is nominally 6dB and sensitive down to about -100dBm (i.e. sensitivity). The RSSI level can be calculated using Equation 1.

$$\text{RSSI level} = \text{RSSI\_OUT} < 0{:}2 > + (1 - \text{LNA\_GAIN}) \times 3 + (1 - \text{BBAMP\_GAIN}) \times 3 \quad (1)$$

where:
LNA_GAIN and BBAMP_GAIN can take the values 0 or 1 according to the register settings. This gives a range of RSSI levels from 0 to 13 with a step size of approximately 6dB/step.

4.3.5 RF_R16 to R19 AGC Configuration Registers

Table 20. Register RF_R16 Settings Addr: C7h

Bit	Name	Description	R/W	Hardware Reset
0	AGC_MODE<0>	AGC Mode 0	RW	0
1	AGC_MODE<1>	AGC Mode 1	RW	0
2	AGC_ST_TIME<0>	AGC Settle Time 0	RW	0
3	AGC_ST_TIME<1>	AGC Settle Time 1	RW	0
4	AGC_LST_TIME<0>	AGC Listen Time 0	RW	0
5	AGC_LST_TIME<1>	AGC Listen Time 1	RW	0
6	AGC_PERSIST<0>	AGC Persist 0	RW	0

Table 20. Register RF_R16 Settings Addr: C7h (continued)

Bit	Name	Description	R/W	Hardware Reset
7	AGC_PERSIST<1>	AGC Persist 1	RW	0

Table 21. Register RF_R17 Settings Addr: C8h

Bit	Name	Description	R/W	Hardware Reset
0	AGC_FLG_TIME<0>	AGC Flag Time 0	RW	0
1	AGC_FLG_TIME<1>	AGC Flag Time 1	RW	0
2	SPARE	SPARE	RW	0
3	SPARE	SPARE	RW	0
4	BBDET_GD_TRIM<0>	AGC BBDET Gain Down Trim 0	RW	0
5	BBDET_GD_TRIM<1>	AGC BBDET Gain Down Trim 1	RW	0
6	BBDET_GU_TRIM<0>	AGC BBDET Gain Up Trim 01	RW	0
7	BBDET_GU_TRIM<1>	AGC BBDET Gain Up Trim	RW	0

Table 22. Register RF_R18 Settings Addr: C9h

Bit	Name	Description	R/W	Hardware Reset
0	RSSI_GD_TRIM<0>	AGC RSSI Gain Down Trim 0	RW	0
1	RSSI_GD_TRIM<1>	AGC RSSI Gain Down Trim 1	RW	0
2	RSSI_GU_TRIM<0>	AGC RSSI Gain Up Trim 0	RW	0
3	RSSI_GU_TRIM<1>	AGC RSSI Gain Up Trim 1	RW	0
4	VSS	Ground	RW	0
5	VSS	Ground	RW	0
6	VSS	Ground	RW	0
7	VSS	Ground	RW	0

Table 23. Register RF_R19 Settings: CAh

Bit	Name	Description	R/W	Hardware Reset
0	SPARE	SPARE	RW	0
1	SPARE	SPARE	RW	0
2	SPARE	SPARE	RW	0
3	SPARE	SPARE	RW	0
4	SPARE	SPARE	RW	0
5	SPARE	SPARE	RW	0
6	SPARE	SPARE	RW	0
7	SPARE	SPARE	RW	0

4.3.6 RF_R20 Read-back Register

Table 24. Register RF_R20 Status Readout Addr: CBh

Bit	Name	Description	R/W
0	AGC_RB_LNA_GAIN	Readback LNA_GAIN	R
1	AGC_RB_BBAMP_GAIN	Readback BBAMP_GAIN	R
2	AGC_RB_GD_FLG	Readback AGC Gain Down Flag	R

Table 24. Register RF_R20 Status Readout Addr: CBh (continued)

Bit	Name	Description	R/W
3	AGC_RB_GU_FLG	Readback AGC Gain Up Flag	R
4	VCOTUNE_LO	VCO tune voltage < 450mV	R
5	VCOTUNE_HI	VCO tune voltage > 650mV	R
6	VSS	Ground	R
7	VSS	Ground	R

4.4 MAC SFR Registers

The following MAC registers are described in detail: MAC_R0 to MAC_R22.

MAC_R0

Address: CCh

FIELD	NAME	MODE	RESET	DESCRIPTION
3:0	MSG_TYPE1	R/W	0	Message type 1 : here are the different type of messages: • 'd0: NO-MSG • 'd1: BSEEK • 'd2: NO-MSG • 'd3: BACK • 'd4: TACK • 'd5: BREQDATA • 'd6: BREQSTAT • 'd7: BSENDCFG • 'd8: BSENDDATA • 'd9: NO-MSG • 'd10: B2BSENDDATA • 'd11: B2BREQDATA • 'd12: T2BREQDATA • Others: NO-MSG
7:4	OPCODE (MSG_TYPE2)	R/W	0	Message type 2: similar to message type 1: BSEEK prohibited • 'd0: NO-MSG • 'd5: BREQDATA • 'd7: BSENDCFG • 'd8: BSENDDATA • Others: NO-MSG

MAC_R1

Address: CDh

FIELD	NAME	MODE	RESET	DESCRIPTION
7:0	CULSTER_ADDR	R/W	0	Each cluster is an star Network made up of up to 8 Targets and one Base station, which communicate via the same RF channel. During the link establishment each target assigned to a single cluster. This address must be NON-ZERO.

MAC_R2

Address: CEh

FIELD	NAME	MODE	RESET	DESCRIPTION
2:0	TARGET ADDRESS	R/W	0	This is an identifier unique to the Target device. It is first used in BSEEK transactions when the Base station is establishing a link with a Target. It is always present during each of the BREQ and TACK phases of a normal transaction. It isn't present during a BACK message.
7:3	Reserved			

MAC_R3

Address: CFh

FIELD	NAME	MODE	RESET	DESCRIPTION
7:0	CLUSTER MASK	R/W	0	This is a word exchanged during Link establishment which is then used to mask data (XOR) exchanged between the Base station and Target thereafter. It provides data whitening as well as a basic level of data security. This field is optional i.e. a zero here means no data whitening.

MAC_R4

Address: D2h

FIELD	NAME	MODE	RESET	DESCRIPTION
2:0	CLUSTER MASK	R/W	0	Same as above for MAC_R3
6:3	CHANNEL_SET		0	Index to the lookup table in order to select the RF channel frequency band. Only used if RSSI_BYPASS is high
7	Reserved		0	

MAC_R5

Address: D3h

FIELD	NAME	MODE	RESET	DESCRIPTION
0	RESET_MAC	R/W	0	0] = RESET_MAC_BIT Set to RESET MAC control engine. On Base station, the Target pointed to by Target Address also has its Target Record registers cleared
1	ENABLE ADVANCED NETWORKING MODE	R/W	0	In this mode, addressing is based on a Global Network ID set in TARGET_REC_IN. For Base station: SET to enable LISTEN MODE, where the Base station can receive alarm messages from Target's on it's network or otherwise. It would also communicate with other Base stations. For Target: Set to enable INITIATE MODE, where the Target can send an alarm message to a Base station. This mode is also used for ROAMING.
4:2	OUTPUT SELECT	R/W	0	These bits are used to select which of the MAC Status bits are selected for output. There are 8 selection modes and the STATUS SELECT OUTPUT bus is 16-bits wide, making it able to access up to 128 MAC status bits.

5	CHIP ID/ TARGET DATA SELECT	R/W	0	For Base stations : CHIP ID SELECT This bit is cleared and transmits the GLOBAL NETWORK ID – note this is the default. If this bit is set then SENSIUM™ CHIP ID is selected for transmission with SENSIUM_CFG_DATA. For Targets: TARGET DATA SELECT This bit is cleared to select TARGET REC OUT for transmission of SENSIUM_CFG_DATA. Otherwise it transmits TARGET REC IN. This is an alternative means for a fixed amount of data (16 bytes) to be transferred without DMA intervention.
6	ACCEPT_JOIN / ROAMING MODE	R/W	0	For Base station : ACCEPT_JOIN Set this bit when the Base station is accepting ROAMING Targets. For Targets : ROAMING Set this bit together with the Advanced Networking Mode bit to enable ROAMING. A FORCECOMMS still needs to be asserted to kick off the process.
7	DELETE_TARGET /RX_START_ADDR	R/W	0	For Base station : DELETE TARGET Set this bit after the Target Number for the target to be deleted to erase and free up its slot. It is edge triggered, so to assert, it needs to be cleared and then set. For Target : RX_START_ADDR Set to Load the start address for a BSENDDATA message. This makes it possible for BREQDATA and BSENDDATA to access different memory sections.

MAC_R6

Address: D4h

FIELD	NAME	MODE	RESET	DESCRIPTION
0	FLUSH_MAC	R/W	0	Set this bit to clear all the internal MAC control variables. For a Target that already has a Link established and Base station, it sends the MAC to sleep afterwards. This provides a tidy method to recover from Link Errors.
1	DISABLE AUTO SYNC	R/W	0	Target Only Set to disable the AUTO-SYNC feature which synchronizes the Target's timers to that of the Base station.
2	DEBUG MODE	R/W	0	Set this bit to enable the generation of a DEBUG interrupt anytime the MAC changes state. This provides a very powerful tool for debugging the MAC.
3	MACEnable	R/W	0	Enable the MAC (if this signal is low, key MAC signals are reset and nothing happens). Must be high if MAC operation is desired.
4	CRCEnable	R/W	0	Enable CRC checking (recommended)
5	START_COMMS	R/W	0	When this signal is high, the Base station starts a new communication. When a WAKE_UP_ENA interrupt is received by the micro, this signal must be toggled so that the Base station can start communication with the scheduled Target.
6	HIBERNATE	R/W	0	Hibernate control enable bit. Set to freeze chip. Can resume by asserting the RESUME I/O pin
7	Reserved	R/W	0	Unused

MAC_R7

Address: D5h

FIELD	NAME	MODE	RESET	DESCRIPTION
5:0	SLEEP_TIME	R/W	0	Sleep time value.
7:6	SLEEP_TYPE	R/W	0	The granularity of sleep time: • ‘d0: seconds • 'd1: minutes • 'd2: hours • ‘‘d3: days

MAC_R8

This is the RF configuration register. It sets the timing between the SynthEnable, TxEnable, RxEnable and FSBEnable signals. This timing is done by the RF_ENABLES_GEN module which takes this register as input.

Address: D6h

FIELD	NAME	MODE	RESET	DESCRIPTION
1:0	SYNTH_SETTLE	R/W	0	Synthesizer settles time. • ‘d0: 0.5 ms. • ‘d1: 1.0 ms • ‘d2: 2.0 ms • 'd3: 4.0 ms
3:2	TX_SETTLE	R/W	0	• ‘d0: 0.125 ms • 'd1: 0.25 ms • 'd2: 0.50 ms • ‘d3: 1.0 ms
5:4	RX_SETTLE	R/W	0	• ‘d0: 0.125 ms • 'd1: 0.25 ms • 'd2: 0.50 ms • ‘d3: 1.0 ms
7:6	RXTX_TURNARND	R/W	0	• ‘d0: 0.125 ms • 'd1: 0.25 ms • 'd2: 0.50 ms • ‘d3: 1.0 ms

MAC_R9

Some link control parameter settings.

Address: DCh

FIELD	NAME	MODE	RESET	DESCRIPTION
1:0	Reserved			Unused
3:2	CHANNEL_DWELL_TIME	R/W	0	This parameter determines how long (in number of milliseconds) the Base station or Target dwells on a channel waiting for preamble before moving to another channel or retrying depending on LinkEstablishment Status. • ‘d0: 5 ms • 'd1: 10 ms • 'd2: 20 ms • ‘‘d3: 40 ms

5:4	TRANS_RETRY	R/W	0	This parameter determines how many times a Base station or Target device retries a failed communication transaction before quitting with a Link Error Interrupts. • ‘d0: 2 • 'd1: 8 • 'd2: 16 • ‘'d3: 63
7:6	WAKE_FALL_BACK	R/W	0	This parameter the number of seconds a Target/Base station goes to sleep for when it doesn’t find the Base station/Target on wake-up. • ‘d0: 4 s • 'd1: 8 s • 'd2: 16 s • ‘'d3: 32 s

MAC_R10

Input signals for MAC_BYPASS mode and MAX symbols setting.

Address: DDh

FIELD	NAME	MODE	RESET	DESCRIPTION
0	MAC_BYPASS_EN	R?W	0	Bypass the MAC.
1	MAC_BP_FSBEN	R/W	0	FSBEnable BYPASS input
2	MAC_BP_RXEN	R/W	0	RxEnable BYPASS input
3	MAC_BP_SYNTHEN	R/W	0	SynthEnable BYPASS input
4	MAC_BP_TXEN	R/W		TxEnable BYPASS input
7:5	MAX_TRX_SYMBOLS	R/W	0	MAXIMUM number of MAC_WORDs transmitted or received in one PAYLOAD frame. This setting must be the same for all targets and Base stations in the same network. • ‘d0: 24 words • 'd1: 48 words • 'd2: 80 words • ‘'d3: 160 words • ‘'d4: 320 words • ‘'d5: 640 words • ‘'d6: 1280 words • ‘'d7: 2560 words The lower settings are better suited to a noisy RF channel but would mean that the throughput would be much lower due to higher overhead ratio.

MAC_R11

More link control settings.

Address: DEh

FIELD	NAME	MODE	RESET	DESCRIPTION
1:0	RETRY_LMT_SLCT	R/W	0	How many cycles to wait for a condition before giving up.
3:2	NUM_OF_RETRIES_SLCT	R/W	0	How many times to retry a PREAMBLE or SYNC_WORD search (incremented after RETRY_LIMIT_SLCT or DWELL_TIME miliseconds)
4	RSSI_BYPASS	R/W	0	Bypass the use of RSSI for channel selection. Not advisable in practice because error handling isn’t well defined. • ‘b0: RSSI Enabled • ‘b1: RSSI Disabled/Bypassed

5	ENA_EARLY_TIME	R/W	0	Auto correction of sleep time due to the oscillator drift.
6	BITSTREAM_SEL	R/W	0	Set to enable DSM bitstream acquisition on the DSM data ready interrupt.
7	Reserved	R/W	0	

MAC_R12

Address: DFh

FIELD	NAME	MODE	RESET	DESCRIPTION		
3:0	CHANNEL_SET	R/W	0	RF Channel selection input used in override mode (when RSSI_BYPASS is set) as RF Channel LUT input.		
5:4	SRAM_SPLIT	R/W	00	Code and XData Memory Split in 64kB.		
				SRAM	CODE	XDATA
				00	32kB	32kB
				01	16kB	48kB
				10	48kB	16kB
				11	32kB	32kB
7:6	Reserved					

MAC_R18

Address: ECh

FIELD	NAME	MODE	RESET	DESCRIPTION
1:0	Preamble	R/W	0	• ‘d0 Pre-amble size is 40-bit • ‘d1: Pre-amble size is 80-bit • ‘d2: Pre-amble size 120-bit • ‘d3: Pre-amble size 160-bit
3:2	FCEnable	R/W	0	The length of FC enable control signal. • ‘d0: 0 symbols • 'd1: 10 symbols • ‘d2: 20 symbols • ‘d3: un-limited.
5:4	FCMode	R/W	0	The length of FC mode. • ‘d0: 0 symbols • ‘d1: 10 symbols • ‘d2: 20 symbols • ‘d3: un-limited
6:7	DREnable	R/W	0	Data ready retime signal delay • ‘d0: 0 symbols • ‘d1: 10 symbols • ‘d2: 20 symbols • ‘d3: 40 symbols

MAC_R19

Address: EDh

FIELD	NAME	MODE	RESET	DESCRIPTION
1:0	DRELength	R/W	0	Data ready length period. • ‘d0: 1 update periods • ‘d1: 2 update periods • ‘d2: 4 update periods • ‘d3: un-limited.

3:2	DREUpdatePeriod	R/W	0	• 'd0: 10 symbols • 'd1: 20 symbols • 'd2: 40 symbols • 'd3: 80 symbols
7:4	Reserved		0	

MAC_R20

Address: EEh

FIELD	NAME	MODE	RESET	DESCRIPTION
7:0	NUMBER_OF_MEM_WORDS	R/W	0	Number of MAC_WORDs that the MAC will exchange with the memory controller. Actual number of bytes can be calculated using the following : Num of Bytes = (NUN_OF_MEM_WORDS × 11)/8

MAC_R21

Address: EFh

FIELD	NAME	MODE	RESET	DESCRIPTION
5:0	NUMBER_OF_MEM_WORD	R/W	0	Number of words that the MAC will exchange with the memory controller continued.
7:6	Reseerved		0	

MAC_R22

Address: F1h

FIELD	NAME	MODE	RESET	DESCRIPTION
7:0	MAC_MODE	R/W	0	MAC Mode tuning control word . Each bit controls some function; to either enable or disable it. An enable signal requires a high to assert it as does a disable signal. [0] : FULL_LBT_DISABLE (set high to disable LBT functionality which could sometimes interfere with operation when data transfer exceeds 4 seconds). [1] : DISABLE AUTO GENERATION OF MAC WAKEUP ADDRESS (assert to disable the automatic selection of the Target wake-up address to be used by Base station. If asserted, address to be used has to be set manually using BS_TARGET address input. [2] : TRX TIMEOUT DISABLE (disable the generation of a timeout error when data Tx or Rx time exceeds 1 second as specified under LBT specs). [3] : Enable link Error generation in the event of a BUSY Channel timeout during LBT. When not set, an AUTO FLUSH of the MAC is automatically performed. [4]: Disable hamming error checking! (set to disable Hamming error checking of Message and Address words). [5]: Set to use WAKEUP FALLBACK TIME on WAKEUP, else current SLEEPTIME is used. [6] : ENABLE FREEZE and CONTINUE LBT mode (set to cause a freeze of MAC when 4sec LBT timeout occurs). [7] : DISABLE WAKEUP TIMEOUT (set to stop MAC from going back to sleep following a predefined time of 512/256 ms after wakeup ; 512 for BS, 256 for TS).

4.5 TARGET RECORD INPUT REGISTERS

The TARGET REC IN registers comprise a set of 26 registers each 8-bits wide (=208bits). This set of input registers is only used by CC981H Sensium™ Base stations. The information in these registers is sent from the Base station to a target using the BSENDCFG message and is stored in the TARGET REC OUT registers on the target. These are level 3 registers, because they don't affect the behavior of the MAC but are for higher level configuration.

CC981H Sensium™ configuration and data block is now 16 MAC WORDS which is 176 bits. This is broken down as follows:

- 48 bits for Sensor Interface setup
- 80 bits for application specific data
- 48 bits for a unique chip ID or Global Network ID

SENSIUM™ CONFIGURATION and DATA BLOCK		
SENSOR INTERFACE CONFIGURATION	APPLICATION DATA	SENSIUM™ CHIP ID or GNID
---------- 48 bits ----------	---------- 80 bits ----------	---------- 48 bits ----------

These 176 (22 bytes) of CC981H Sensium™ Configuration and data block is assigned to:

TARGET_REC_IN_R2 -> TARGET_REC_IN_R23

With the following breakdown:

SENSIUM_CHIP_ID => { TARGET_REC_IN_R7 , TARGET_REC_IN_R6 , TARGET_REC_IN_R5 , TARGET_REC_IN_R4 , TARGET_REC_IN_R3 , TARGET_REC_IN_R2 }

For the Base station the CC981H Sensium™, bit 5 CHIP_ID_SEL of register MAC_R5 determines if the GNID (Global network ID) or the Base station chip ID is included in the BSENDCFG message. Note the default is CHIP_ID_SEL = 0 and the GNID is sent from the Base station to the target. If the GNID is selected, the Base station sends the GNID in the lower 32-bits of the 48-bits. The other 2 bytes are the rest of the CHIP ID. When CHIP_ID_SEL = 1, the whole CHIP ID is sent.

For the Target station the CC981H Sensium™ chip ID is always included in the status data field of the BREQSTATUS (TACK) message from the target to the Base station. The first 16bytes of data included in a status message can be selected from either the TARGET REC IN or TARGET REC OUT registers according to the setting of bit 5 in MAC_R5 on the target.

APPLICATION_DATA => { TARGET_REC_IN_R17 , TARGET_REC_IN_R16 , TARGET_REC_IN_R15 , TARGET_REC_IN_R14 , TARGET_REC_IN_R13 , TARGET_REC_IN_R12 , TARGET_REC_IN_R11 , TARGET_REC_IN_R10 , TARGET_REC_IN_R9 , TARGET_REC_IN_R8 }

Application data in the BSENDCFG message enables a Base station to send any additional data or parameters to a target when configuring the target.

SI_CONFIG_DATA [47:0] => {TARGET_REC_IN_R23, TARGET_REC_IN_R22, TARGET_REC_IN_R21, TARGET_REC_IN_R20, TARGET_REC_IN_R19, TARGET_REC_IN_R18 }

The remaining 32 bits (4 bytes) of the 208 bits total are assigned to the GLOBAL NETWORD ID (GNID).

GLOBAL_NETWORK_ID [31:0] => { TARGET_REC_IN_R25, TARGET_REC_IN_R24, TARGET_REC_IN_R1, TARGET_REC_IN_R0 }

TARGET_REC_IN_R0

Address: 88h

FIELD	NAME	MODE	RESET	DESCRIPTION
7:0	GNID[7:0]	R/W	0	GLOBAL NETWORK ID BYTE 0

TARGET_REC_IN_R1

Address: 89h

FIELD	NAME	MODE	RESET	DESCRIPTION
7:0	GNID[15:8]	R/W	0	GLOBAL NETWORK ID BYTE 1

TARGET_REC_IN_R2

Address: 8Ah

FIELD	NAME	MODE	RESET	DESCRIPTION
7:0	CHIP_ID[7:0]	R	0	SENSIUM™ CHIP ID BYTE 0

The unique Sensium™ chip ID is 48 bits long and is contained 6 registers:

TARGET_REC_IN_R2, TARGET_REC_IN_R3, TARGET_REC_IN_R4, TARGET_REC_IN_R5 , TARGET_REC_IN_R6 and TARGET_REC_IN_R7.

The unique ID is blown into fuses at wafer probe and cannot be altered. It is only accessible via the 8051 processor or JTAG.

TARGET_REC_IN_R3

Address: 8Bh

FIELD	NAME	MODE	RESET	DESCRIPTION
7:0	CHIP_ID[15:8]	R	0	SENSIUM™ CHIP ID BYTE 1

TARGET_REC_IN_R4

Address: 8Ch

FIELD	NAME	MODE	RESET	DESCRIPTION
7:0	CHIP_ID[23:16]	R	0	SENSIUM™ CHIP ID BYTE 2

TARGET_REC_IN_R5

Address: 8Dh

FIELD	NAME	MODE	RESET	DESCRIPTION
7:0	CHIP_ID[31:24]	R	0	SENSIUM™ CHIP ID BYTE 3

TARGET_REC_IN_R6

Address: 8Eh

FIELD	NAME	MODE	RESET	DESCRIPTION
7:0	CHIP_ID[39:32]	R	0	SENSIUM™ CHIP ID BYTE 4

TARGET_REC_IN_R7

Address: 91h

FIELD	NAME	MODE	RESET	DESCRIPTION
7:0	CHIP_ID[47:40]	R	0	SENSIUM™ CHIP ID BYTE 5

TARGET_REC_IN_R8

Address: 92h

FIELD	NAME	MODE	RESET	DESCRIPTION
7:0	APP_DATA[7:0]	R/W	0	APPLICATION DATA BYTE 0

TARGET_REC_IN_R9

Address: 93h

FIELD	NAME	MODE	RESET	DESCRIPTION
7:0	APP_DATA[15:8]	R/W	0	APPLICATION DATA BYTE 1

TARGET_REC_IN_R10

Address: 94h

FIELD	NAME	MODE	RESET	DESCRIPTION
7:0	APP_DATA[23:16]	R/W	0	APPLICATION DATA BYTE 2

TARGET_REC_IN_R11

Address: 95h

FIELD	NAME	MODE	RESET	DESCRIPTION
7:0	APP_DATA[31:24]	R/W	0	APPLICATION DATA BYTE 3

TARGET_REC_IN_R12

Address: 96h

FIELD	NAME	MODE	RESET	DESCRIPTION
7:0	APP_DATA[39:32]	R/W	0	APPLICATION DATA BYTE 4

TARGET_REC_IN_R13

Address: 97h

FIELD	NAME	MODE	RESET	DESCRIPTION
7:0	APP_DATA[47:40]	R/W	0	APPLICATION DATA BYTE 5

TARGET_REC_IN_R14

Address: 98h

FIELD	NAME	MODE	RESET	DESCRIPTION
7:0	APP_DATA[55:48]	R/W	0	APPLICATION DATA BYTE 6

TARGET_REC_IN_R15

Address: 99h

FIELD	NAME	MODE	RESET	DESCRIPTION
7:0	APP_DATA[63:56]	R/W	0	APPLICATION DATA BYTE 7

TARGET_REC_IN_R16

Address: 9Ah

FIELD	NAME	MODE	RESET	DESCRIPTION
7:0	APP_DATA[71:64]	R/W	0	APPLICATION DATA BYTE 8

TARGET_REC_IN_R17

Address: 9Bh

FIELD	NAME	MODE	RESET	DESCRIPTION
7:0	APP_DATA[79:72]	R/W	0	APPLICATION DATA BYTE 9

TARGET_REC_IN_R18

Address: 9Ch

FIELD	NAME	MODE	RESET	DESCRIPTION
1:0	SI_CONFIG_DATA[1:0]	R/W	0	RESERVED
3:2	SI_CONFIG_DATA[3:2] = FILTER_DLY	R/W	0	Delay in term of 1Khz clock before switching over to another Sensor. • ‘d0 : 60 ms • ‘d1 : 80 ms • ‘d2 : 160 ms • ‘d3 : 120 ms
4	SI_CONFIG_DATA[4] = CONT_CONVERSION_EN	R/W	0	Continuous conversion enable; This causes the Conversion Enable output from the Sensor Interface controller to remain high and continuously take samples from one sensor (e.g ECG monitoring).
5	SI_CONFIG_DATA[5] = SI_POWERUP_EN	R/W	0	Power Up the Sensor Interface.
6	SI_CONFIG_DATA[6] = SI_ENABLE	R/W	0	Enable the Sensor Interface Controller.
7	SI_CONFIG_DATA[7] = FREQUENCY_S3[0]	R/W	0	SAMPLING frequency of DSM FILTER for Sensor 3 continued

TARGET_REC_IN_R19

Address: 9Dh

FIELD	NAME	MODE	RESET	DESCRIPTION
0	SI_CONFIG_DATA[8] = FREQUENCY_S3[1]	R/W	0	SAMPLING frequency of DSM FILTER for Sensor 3
2-1	SI_CONFIG_DATA[10:9] = FREQUENCY_S2	R/W	0	SAMPLING frequency of DSM FILTER for Sensor 2
4-3	SI_CONFIG_DATA[12:11] = FREQUENCY_S1	R/W	0	SAMPLING frequency of DSM FILTER for Sensor 1 • 'd0 : 250 Hz • ‘d1 : 100 Hz • ‘d2 : 50 Hz • ‘d3 : 25 Hz
6-5	SI_CONFIG_DATA[14:13] = COUNT_SAMPLE3[1:0]	R/W	0	Number of sample that will be taken from SENSOR3.
7	SI_CONFIG_DATA[15] = COUNT_SAMPLE2[0]	R/W	0	Number of samples that will be taken from SENSOR2 continued.

TARGET_REC_IN_R20

Address: 9Eh

FIELD	NAME	MODE	RESET	DESCRIPTION
0	SI_CONFIG_DATA[16] = COUNT_SAMPLE2[1]	R/W	0	Number of samples that will be taken from SENSOR2.
2-1	SI_CONFIG_DATA[18:17] = COUNT_SAMPLE1[1:0]	R/W	0	Number of sample that will be taken from SENSOR1.
7-3	SI_CONFIG_DATA[23:19] = INTERVAL_S3[7:3]	R/W	0	Time interval between sampling from SENSOR3 continued.

TARGET_REC_IN_R21

Address: A1h

FIELD	NAME	MODE	RESET	DESCRIPTION
7-5	SI_CONFIG_DATA[26:24] = INTERVAL_S3[2:0]	R/W	0	Time interval between sampling from SENSOR3.
4-0	SI_CONFIG_DATA[31:27] = INTERVAL_S2[4:0]	R/W	0	Time interval between sampling from SENSOR2 continued.

TARGET_REC_IN_R22

Address: A3h

FIELD	NAME	MODE	RESET	DESCRIPTION
2-0	SI_CONFIG_DATA[34:32] = INTERVAL_S2[7:5]	R/W	0	Time interval between sampling from SENSOR2 continued.
7-3	SI_CONFIG_DATA[39:35] = INTERVAL_S1[4:0]	R/W	0	Time interval between sampling from SENSOR1 continued.

TARGET_REC_IN_R23

Address: A4h

FIELD	NAME	MODE	RESET	DESCRIPTION
2-0	SI_CONFIG_DATA[42:40] = INTERVAL_S1[7:5]	R/W	0	Time interval between sampling from SENSOR1.
7-3	SI_CONFIG_DATA[47:43] = SCMODE[4:0]	R/W	0	Different modes for the sensor interface: • 'h0: MODE0 • 'h1: MODE1 • …. • …. • 'hE: MODE18

TARGET_REC_IN_R24

Address: A5h

FIELD	NAME	MODE	RESET	DESCRIPTION
7:0	GNID[23:16]	R/W	0	GLOBAL NETWORK ID BYTE 2

TARGET_REC_IN_R25

Address: A6h

FIELD	NAME	MODE	RESET	DESCRIPTION
7:0	GNID[31:24]	R/W	0	GLOBAL NETWORK ID BYTE 3

4.6 TARGET RECORD OUTPUT REGISTERS

This is a 208 bit output word organized as 26 registers (each 8-bit wide). The SI_CONFIG_DATA, APPLICATION DATA and SENSIUM™ CHIP ID parts are the read back data of TARGET_REC_IN_R23-R2 above and have the same structure. The remaining 4 bytes are MAC status information.

After a Base station has sent a BREQSTATUS command to a target, this set of Base station TARGET REC OUT registers stores the data received back from the addressed target's TARGET REC OUT registers. On a target, after receiving a BSENDCFG message from a Base station, this field holds the data received from the Base station TARGET_REC_IN registers.

SENSIUM™ CONFIGURATION and DATA BLOCK		
SENSOR INTERFACE CONFIGURATION	APPLICATION DATA	SENSIUM™ CHIP ID or GNID
---------- 48 bits ----------	---------- 80 bits ----------	---------- 48 bits ----------

These 176 (22 bytes) of CC981H Sensium™ Configuration and data block is assigned to:

TARGET_REC_OUT_R2 -> TARGET_REC_OUT_R23

With the following breakdown:

SENSIUM_CHIP_ID => { TARGET_REC_OUT_R7 , TARGET_REC_OUT_R6 , TARGET_REC_OUT_R5 , TARGET_REC_OUT_R4 , TARGET_REC_OUT_R3 , TARGET_REC_OUT_R2 }

APPLICATION_DATA => { TARGET_REC_OUT_R17, TARGET_REC_OUT_R16, TARGET_REC_OUT_R15, TARGET_REC_OUT_R14, TARGET_REC_OUT_R13, TARGET_REC_OUT_R12, TARGET_REC_OUT_R11, TARGET_REC_OUT_R10, TARGET_REC_OUT_R9, TARGET_REC_OUT_R8}

SI_CONFIG_DATA[47:0] => { TARGET_REC_OUT_R23, TARGET_REC_OUT_R22, TARGET_REC_OUT_R21, TARGET_REC_OUT_R20, TARGET_REC_OUT_R19, TARGET_REC_OUT_R18}

The remaining 32 bits (4 bytes) of the 208 bits total are assigned to internal MAC status information.

TARGET_REC_OUT_R25 => {Timer MSBs , Link Status and Address MSBs}

TARGET_REC_OUT_R24 => {Address LS Byte}

TARGET_REC_OUT_R1 => {SLEEP TIME}

TARGET_REC_OUT_R0 => {Timer Lower Byte}

TARGET_REC_OUT_R0

Address: E2h

FIELD	NAME	MODE	RESET	DESCRIPTION
7:0	SleepTimerMsecs[7:0]	R	0	Milliseconds output (8 LSBs) of Sleep Timer. Can be used to decide direction of 32kHz crystal drift.

TARGET_REC_OUT_R1

Address: E3h

FIELD	NAME	MODE	RESET	DESCRIPTION
7-6	SleepTimeType	R	0	• ‘d0: The sleep time granularity is second. • ‘d1: The sleep time granularity is minutes. • ‘d2: The sleep time granularity is hours • ‘d3: The sleep time granularity is days
5-0	SleepTime	R	0	0 to 63 time units as specified by SleepTimeType. **This field must be non-zero for it to be functional in any application.**

TARGET_REC_OUT_R2

Address: E4h

FIELD	NAME	MODE	RESET	DESCRIPTION
7:0	CHIP_ID[7:0]	R	0	SENSIUM™ CONFIG ID BYTE 0

TARGET_REC_OUT_R3

Address: E5h

FIELD	NAME	MODE	RESET	DESCRIPTION
7:0	CHIP_ID[15:8]	R	0	SENSIUM™ CONFIG ID BYTE 1

TARGET_REC_OUT_R4

Address: E6h

FIELD	NAME	MODE	RESET	DESCRIPTION
7:0	CHIP_ID[23:16]	R	0	SENSIUM™ CONFIG ID BYTE 2

TARGET_REC_OUT_R5

Address: E7h

FIELD	NAME	MODE	RESET	DESCRIPTION
7:0	CHIP_ID[31:24]	R	0	SENSIUM™ CONFIG ID BYTE 3

TARGET_REC_OUT_R6

Address: E9h

FIELD	NAME	MODE	RESET	DESCRIPTION
7:0	CHIP_ID[39:32]	R	0	SENSIUM™ CONFIG ID BYTE 4

TARGET_REC_OUT_R7

Address: EAh

FIELD	NAME	MODE	RESET	DESCRIPTION
7:0	CHIP_ID[47:40]	R	0	SENSIUM™ CONFIG ID BYTE 5

TARGET_REC_OUT_R8

Address: EBh

FIELD	NAME	MODE	RESET	DESCRIPTION
7:0	APP_DATA[7:0]	R	0	APPLICATION DATA BYTE 0

TARGET_REC_OUT_R9

Address: ECh

FIELD	NAME	MODE	RESET	DESCRIPTION
7:0	APP_DATA[15:8]	R	0	APPLICATION DATA BYTE 1

TARGET_REC_OUT_R10

Address: EDh

FIELD	NAME	MODE	RESET	DESCRIPTION
7:0	APP_DATA[23:16]	R	0	APPLICATION DATA BYTE 2

TARGET_REC_OUT_R11

Address: EEh

FIELD	NAME	MODE	RESET	DESCRIPTION
7:0	APP_DATA[31:24]	R	0	APPLICATION DATA BYTE 3

TARGET_REC_OUT_R12

Address: EFh

FIELD	NAME	MODE	RESET	DESCRIPTION
7:0	APP_DATA[39:32]	R	0	APPLICATION DATA BYTE 4

TARGET_REC_OUT_R13

Address: F1h

FIELD	NAME	MODE	RESET	DESCRIPTION
7:0	APP_DATA[47:40]	R	0	APPLICATION DATA BYTE 5

TARGET_REC_OUT_R14

Address:F2h

FIELD	NAME	MODE	RESET	DESCRIPTION
7:0	APP_DATA[55:48]	R	0	APPLICATION DATA BYTE 6

TARGET_REC_OUT_R15

Address: F3h

FIELD	NAME	MODE	RESET	DESCRIPTION
7:0	APP_DATA[63:56]	R	0	APPLICATION DATA BYTE 7

TARGET_REC_OUT_R16

Address: F4h

FIELD	NAME	MODE	RESET	DESCRIPTION
7:0	APP_DATA[71:64]	R	0	APPLICATION DATA BYTE 8

TARGET_REC_OUT_R17

Address: F5h

FIELD	NAME	MODE	RESET	DESCRIPTION
7:0	APP_DATA[79:72]	R	0	APPLICATION DATA BYTE 9

TARGET_REC_OUT_R18

Address: F6h

FIELD	NAME	MODE	RESET	DESCRIPTION
7:0	SI_CONFIG_DATA [7:0]	R	0	See TARGET_REC_IN_R18 for breakdown.

TARGET_REC_OUT_R19

Address: F7h

FIELD	NAME	MODE	DEFAULT	DESCRIPTION
7:0	SI_CONFIG_DATA [15:18]	R	0	See TARGET_REC_IN_R19 for breakdown.

TARGET_REC_OUT_R20

Address: FAh

FIELD	NAME	MODE	DEFAULT	DESCRIPTION
7:0	SI_CONFIG_DATA [23:16]	R	0	See TARGET_REC_IN_R20 for breakdown.

TARGET_REC_OUT_R21

Address: FBh

FIELD	NAME	MODE	DEFAULT	DESCRIPTION
7:0	SI_CONFIG_DATA [31:24]	R	0	See TARGET_REC_IN_R21 for breakdown.

TARGET_REC_OUT_R22

Address: FCh

FIELD	NAME	MODE	DEFAULT	DESCRIPTION
7:0	SI_CONFIG_DATA [39:32]	R	0	See TARGET_REC_IN_R22 for breakdown.

TARGET_REC_OUT_R23

Address: FDh

FIELD	NAME	MODE	DEFAULT	DESCRIPTION
7:0	SI_CONFIG_DATA [47:40]	R	0	See TARGET_REC_IN_R23 for breakdown.

TARGET_REC_OUT_R24

Address: FEh

FIELD	NAME	MODE	DEFAULT	DESCRIPTION
7:0	CTAdress [7:0]	R	0	8 LSBs Target Address

TARGET_REC_OUT_R25

Address: FFh

FIELD	NAME	MODE	DEFAULT	DESCRIPTION
7:6	SleepTimerMSecs[9:8]	R	0	2 MSBs of sleep timer.
5	FSBEnable	R	0	Internal FSB Enable of MAC
4	Enable	R	0	This bit shows that the instance is enabled. It is used to enable the sleep counter when asserted or disable and reset it when de-asserted.
3	LinkEstablishment	R	0	A flag indicating that the link has been established.
2:0	CTAddress [10:8]	R	0	3 MSBs of Target Address

4.7 UART Special Functions Registers

UART control register 0 **SCON0** **Read/Write**

Addr.	Bit7							Bit0	Reg.	R/W
D8h	MOE	MFE	MPE	SM1	SMO	LBE	REN	ENA	SCON0	R

MOE	1	Overwrite Error enabled
	0	Masking overwrite error
MFE	1	Framing Error enabled
	0	Masking framing error
MPE	1	Parity Error enabled
	0	Masking parity error
SM0/SM1	0/0	Mode1
	0/1	Mode2
	1/0	Mode3
	1/1	Mode4
LBE	1	Loop back enable of UART data
REN	1	Receiver enable
ENA	1	Enable Uart-module

UART control register 0 **SCON0** **Read/Write**

Addr.	Bit7							Bit0	Reg.	R/W
D8h	MOE	MFE	MPE	SM1	SMO	LBE	REN	ENA	SCON0	R

MOE	1	Overwrite Error enabled
	0	Masking overwrite error
MFE	1	Framing Error enabled
	0	Masking framing error
MPE	1	Parity Error enabled
	0	Masking parity error
SM0/SM1	0/0	Mode1
	0/1	Mode2
	1/0	Mode3
	1/1	Mode4
LBE	1	Loop back enable of UART data
REN	1	Receiver enable
ENA	1	Enable Uart-module

UART control register 1 **SCON1** **Read/Write**

Addr.	Bit7							Bit0	Reg.	R/W
D9h	OE	FE	PE	–	TB8	–	T1	R1	SCON1	R

OE	1	Overwrite error (reset by a read of SACON1)
FE	1	Framing error (reset by a read of SACON1)
PE	1	Parity error (reset by a read of SACON1)
TB8		9th transmit data bit (only modes 2-4
		This is a status bit indicating that the 9th bit is currently transmitted
TI	1	Transmitter interrupt (reset by a read of SACON1)
RI	1	Receiver interrupt (reset by a read of SACON1

Note that every read-access to any bit of this register is recognized as a read-access to all bits thus even a bit-addressed read to one bit will reset all status bits. Thus, a byte read command should be used.

UART control register 2 **SCON2** **Read/Write**

Addr.	Bit7							Bit0	Reg.	R/W
DAh	–	–	–	–	IRDA	RTS	TXF	RXNE	SCON2	RW

This register is a control and status register.
RTS is used to select if receive data flow should be enabled.
IRDA selects between IrDA and “standard” UART data bit representation.
RXNE and TXF are status bits that are updated continuously (each clock cycle). Writing to these bits has no effect.

IRDA	1	IrDA data pulse modulation used. (TXD/RXD according to IrDA v1.0)
	0	UART mode
RTS	1	Inactive - receive data flow disabled
	0	Active - enables data flow (unless HW RTS stops the flow)
TXF	1	TX buffer is full (do not write more data to TX buffer)
RXNE	1	RX buffer is not empty (data could be read)

UART data register **SABUF** **Read/Write**

Addr.	Bit7							Bit0	Reg.	R/W
DBh	D7	D6	D5	D4	D3	D2	D0	RXNE	SBUF	RW

This register contains the 8 bit data word to be transmitted or received by the UART module.
On a write access to this register address, the internal transmit data buffer.
TXBUF is written by a read access the internal receive buffer RXBUF is read

UART data rate and RI/TI mask **SASCAL** **Read/Write**

Addr.	Bit7							Bit0	Reg.	R/W
DCh	DTI	DRI	–	–	SCL	SCL	SCL	SCL	SASCA	RW

DTI	1	Masking of transmit interrupt
DRI	1	Masking of receive interrupt

SASCAL register bits SCL3-SCL0 are used for selection of the baud rate of the UART module. The Baud rate is given by following relationship:

Baudrate =	10.368 x 16 MHz
SASCAL[3:0] = 0 to 5	45 x 2(SASCAL[3:0]+1)
Baudrate =	10.368 x 64 MHz
SASCAL[3:0] = 6 to A	135 x 2(SASCAL[3:0]+1)

After reset, this register is initialized to 08h. This gives a baud rate of 9600 Baud.

SASCAL[3:0] (hex)	Baudrate
0000 = 0	1843200
1	921600
2	460800
3	230400
4	115200
5	57600
6	38400
7	19200
8	9600
9	4800
A	2400
B, C, D, E and F	2400

UART Baud Rate Tune register **SATUNE** **Read/Write**

Addr.	Bit7						Bit0	Reg.	R/W
D1h	D7	D6	D5	D4	D3	D2	D0	SATUNE	RW

The coefficient for Baud rate generation

4.8 Register Description SSC Interface

Addr.	Name	Bits	Byte	R/W	Description	Res. value
E1h	SSCTB	8	1	W	SSC Transmit buffer	00h
E2h	SSCRB	8	1	R	SSC Receive buffer	00h
E3h	SSCCON	8	1	R/W	SSC Program/Operating reg.	00h
E4h	SSCBRI	8	1	R/W	SSC Interrupt Enable register	00h
E5h	SSCSTC	8	1	R/W	SSC Status and Control register	00h

Normally the SSC interface is used interrupt driven.

SSC Buffer for Transmit Direction **SSCTB** **WRITE**

Addr.	Bit7							Bit0	Reg.	R/W
E1h									SSCTB	W

The SSCTB register contains the transmit data value. The data to transmit has to be right aligned in the register.

SSC Buffer for Receive Direction **SSCRB** **WRITE**

Addr.	Bit7							Bit0	Reg.	R/W
E1h									SSCRB	R

The SSCRB register contains the receive data value. The receive data is always right aligned in the register.

Programming Mode (SSCCON.EN = 0)

The SSCCON register has two modes. A programming mode and an operating mode. The meaning of this register changes with the selected mode. A mode selection is done via the SSCCON.EN bit. This selection is instant, meaning that the values of the corresponding register bits in a write access are relevant.

SSC Control Register				SSCCON				Read/Write
Addr.	Bit7					Bit0	Reg.	R/W
E3h	EN	MS	PO	PH	HB	BM(2..0)	SSCCON	R/W

EN This bit switches between the programming mode and the operating mode.
- 1 Operating mode is active
- 0 Programming mode is active

MS Master/Slave select bit
- 1 Master Mode. The master SSC generates the shift clock and output it via SCLK
- 0 Slave Mode. The slave SSC operates on the shift clock received via SCLK

PO Clock Polarity Control bit
- 1 Idle clock line is high, leading clock edge is high-to-low transition
- 0 Idle clock line is low, leading clock edge is low-to-high transition

PH Clock Phase Control bit
- 1 Shift transmit data on leading clock edge, latch on trailing edge
- 0 Latch receive data on leading clock edge, shift on trailing edge

HB Heading Control bit
- 1 Transmit/Receive MSB First (required for SPI compatible setting)
- 0 Transmit/Receive LSB First

BM(2.0) Data Width Selection
- 0 Reserved. Do not use this combination
- 1..7 Transfer Data Width is 2..8 bit

Operating Mode (SSCCON.EN = 1):

SSC Control Register				SSCCON						Read/Write
Addr.	Bit7							Bit0	Reg.	R/W
E3h	EN	MS	BSY	LB	RE	TE	TI	RI	SSCCON	R/W

EN This bit switches between the programming mode and the operating mode.
- 1 Operating mode is active
- 0 Programming mode is active

MS Master/Slave select bit (read only in operating mode)
- 1 Master Mode. The master SSC generates the shift clock and output it via SCLK
- 0 Slave Mode. The slave SSC operates on the shift clock received via SCLK

BSY Busy Flag, bit must not be set by software.
- 1 Transfer is in progress
- 0 No transfer is in progress

LB Loop Back bit
- 1 Receive input is connected with transmit output
- 0 Normal outputs

RE Receive Error Flag (reset by read access / can not be written)
- 1 Reception completed before the receive buffer was read.
- 0 No receive error occurred

TE Transmit Error Flag (reset by read access / can not be written)
- 0 Transfer starts with the slave's transmit buffer not being updated
- 1 No transmit error occurred

TI Transmit Interrupt (reset by read access / can not be written
- 0 A transmit interrupt occurred
- 1 No transmit interrupt occurred

RI Receive Interrupt (reset by read access / can not be written)
- 1 A receive interrupt occurred
- 0 No receive interrupt occurred

SSC Baud Rate and Interrupt Enable

Register Description				SSCBRI					Read/Write
Addr.	Bit7						Bit0	Reg.	R/W
E4h	BR(3..0)	REEN	TEEN	TIEN	RIEN	SSCBRI	R/W		

BR(3..0) Using this register the Baud rate of the device is configured.
The Baud rate is Baud rate (BR) = 15.552Mhz / (2^{BR})
Reading the register BR returns the programmed value

REEN Receive Error Enable
- 1 Receive error interrupts are enabled
- 0 Receive error interrupts are disabled

TEEN Transmit Error Enable
- 1 Transmit error interrupts are enabled
- 0 Transmit error interrupts are disabled

TIEN Transmit Interrupt Enable
- 1 Transmit interrupts are enabled
- 0 Transmit interrupts are disabled

RIEN Receive Interrupt Enable
- 1 Receive interrupts are enabled
- 0 Receive interrupts are disabled

SSC Status and Control register					SSCSTC				Read/Write
Addr.	Bit7							Bit0	Reg.	R/W
A5h	I	I	–	SSCPD	I	I	–		SSCSTC	R/W

SSCPD Power control of SSC module
1 SSC is deactivated (internal clocks off)
0 SSC is activated (internal clocks on)

Timer Registers

There are 3 programmable timers A, B and C on the Sensium. The timers are controlled using the SensiumTimerApiLibrary. The timers are driven from a 10kHz clock derived from the 16MHz crystal (see Figure 4 Clock Generation Unit). This means the 16MHz crystal must be on if any of the 3 on chip timers are used. This has power consumption implications.

Timer A	TA/TAWRAP/TACMP	Read/Write
Timer B	TB/TBWRAP/TBCMP	Read/Write
Timer C	TC/TCWRAP/TCCMP	Read/Write

Addr.	Bit7			Bit0	Register	R/W
96h					TxL	R/W
97h					TxH	R/W

TimeA address: TAL/TAH 96H/97H

TimeB address: TBL/TBH 99H/9AH

TimeC address: TCL/TCH 9CH/9DH

These three timers follow exactly the same behavior. In this specification, no further distinction is made between them. When describing register setting the symbol x is used instead of the explicit declaration A, B or C. Note the 3 timers are clocked from a clock signal derived from the 16MHz crystal – see Figure 4 Clock Generation Unit CGU.

An interrupt is generated when the counter in the timer module reaches the value stored in registers TxWRAP, or if the TxCMP value is reached.

Access-Modes

TxCON:TxACCESS	Read/Write Access	Action
00	Read	Read actual timer value is read
	Write	Write value is written to TxWRAP
01	Read	Read actual timer value is read
	Write	Write value is written to TxCMP
10	Read	Read value from TxWRAP is read
	Write	Write value is written to TxWRAP
11	read	Read value from TxCMP is read
	Write	Write value is written to TxCMP

After counter has been started, no write access to TxWRAP/TxCMP is allowed. Note that no value of 0 or 1 has to be written to TxWRAP.

Timer A Configuration register	TACON		Read/Write
Timer B Configuration register	TCCON		Read/Write
Timer C Configuration register	TBCON		Read/Write

Addr.	Bit7			Bit0	Reg.	R/W			
95h	NEWTx MODE	DITx			DIAR	TxACCESS	TM	TxON	TxCONR/W

TimeA address: TACON 95H

TimeB address: TBCON 98H

TimeC address: TCCON 9BH

These three timers follow exactly the same behavior. In this specification, no further distinction is made between them. When describing register setting the symbol x is used instead of the explicit declaration A, B or C.

NEWTxMODE	1	A timer x-interrupt is generated if the timer-counter reaches the value stored in register TxCMP
	0	A timer x-interrupt is generated when the TxWRAP value is reached and the timer x is started again.
DIAR		Disable auto-reload-mode (only for testing)
TxACCESS		Access-mode to special function registers location Tx. Please refer to the description of register Tx
TM		Test-Bit, must not be set by the application SW
TxON	1	Start Timer x
	0	Stop Timer x

Note: Used bits must be set 0. Bit 7 in register ECON (addr 8Bh) enables the clock to the Timers.

4.9 Other SFR Registers

ECON

Address: 8Bh

FIELD	NAME	MODE	DEFAULT	DESCRIPTION
7	wdtimer clock enable	R/W	0	When set the watch dog timer's clock is enabled
6:0	Reserved	R/W	0	

SRAM_CNTRL_R17

Address: DAh

FIELD	NAME	MODE	DEFAULT	DESCRIPTION
7:0	MAC_START_ADDR[7:0]	R/W	0	Lower byte of MAC Memory start address

SRAM_CNTRL_R18

Address: DBh

FIELD	NAME	MODE	DEFAULT	DESCRIPTION
7:0	MAC_START_ADDR[15:8]	R/W	0	Upper byte of MAC Memory start address

WDTCON

Watchdog Control Registers **WDTCON** **Read/Write**

Addr.	Bit7							Bit0	Reg.	R/W
8Dh	–	–	WD2	WD1	–	–	WCAR	WDIS	WDTCON	R/W

WD2, WD1		Watchdog control bits. Both bits can be changed simultaneously (within one instruction)
	01	Reset of watchdog
	10	Initialization of reset
WCAR		Watchdog timer overflow has occurred
	0	No watchdog timer overflow
WDIS	1	Disable watchdog timer and clean watchdog timer.
	0	Watchdog timer enable

WDTOVL

Watchdog Register **WDTOVL** **Read/Write**

Addr.	Bit7			Bit0	Reg.	R/W
8Eh					WDTOVL	R/W

Watchdog timer overflow value corresponds to the high byte of 16 bits watchdog counter.

Registers for GPIO Ports

P2 Port 2 **Read/Write**

Addr.	Bit7							Bit0	Reg.	R/W
A0h	–	–	–	–	P2.3	P2.2	P2.1	P2.0	P2	R/W

P2.0, P2.1, P2.2 and P2.3 are used for the 4 general purpose IOs: GPIO0 to GPIO3 respectively. The other bits do not have any functions. On reset, it is set to the value FFh, which is input mode. Note the GPIO have weak pull ups.

Port0, Port1 and Port3 are not used. They should be reserved.

Registers of the Interrupt Module

Interrupt Request Register **IREQ** **Read/Write**

Addr.	Bit7							Bit0	Reg.	R/W
9Fh	–	–	INT5	INT4	INT3	INT2	INT1	INT0	IREQ0	R/W
A9h	INT13	INT12	INT11	INT10	INT9	INT8	INT7	INT6	IREQ1	R/W

Read operation		
INTx	1	An interrupt is currently requested on the interrupt line
	0	No interrupt is currently requested on the interrupt line
Write operation		
INTx	1	Generates interrupt request No. X
	0	Clear interrupt request for No. X

Bits INTx correspond to the respective interrupt-line x. If an interrupt is detected at interrupt-line x, the bit INTx is set and the respective interrupt (if not masked by IENA) is generated. After the interrupt is processed by the µC, the interrupt-bit is cleared by the interrupt-module. After the interrupt is acknowledged by the µC, the interrupt-bit is reset by the interrupt-module. After reset, the bits are also reset to 0.

Note: Not every interrupt-line is in use, it depends on the implemented peripherals. Bit not used must be set to 0.

The clear interrupt signal is only applicable on an IRQ generated by a write of 1 to the IREQ register. If a request is pending from a connected source, it is active after the clear operation.

Interrupt Enable Register **IE** **Read/Write**

Addr.	xFh	xEh	xDh	xCh	xBh	xAh	x9h	x8h	Reg.	R/W
A8h	INDIS	–	EINT5	EINT4	EINT3	EINT2	EINT1	EINT0	IE0	R/W
E8h	EINT13	EINT12	EINT11	EINT10	EINT9	EINT8	EINT7	EINT6	IE1	R/W

INDIS		Disable all interrupts
	1	Interrupts can be separately masked using register IENA
	0	All interrupts are disabled.
EINTx		Bits EINTx correspond to the respective interrupt-line x. An interrupt x can only be generated if bit EINTx is set 1. Notice that a 0 at EINTx does not prevent an interrupt from setting the request bit in IREQ. Only the generation of the interrupt is disabled.
	1	Enable interrupt No. x
	0	Disable interrupt No. x

Bit not used must be set to 0.

IP0 Interrupt Priority Register **Read/Write**

Addr.	Bit7							Bit0	Reg.	R/W
B8h	–	–	INT5	INT4	INT3	INT2	INT1	INT0	IPL0	R/W
B9h	–	–	INTH5	INTH4	INTH3	INTH2	INTH1	INTH0	IPH0	R/W

2 bits in register IP0 determine the priority of the interrupt No. x. The priority is defined as follows:

INTPRIH0.x	INTPRIL0.x	Priority
0	0	Priority 0 (lowest)
0	1	Priority 1
1	0	Priority 2
1	1	Priority 3 (highest)

A four-level interrupt priority scheme is supported. Each maskable interrupt is individually assigned to one of four priority levels by writing to parallel IPLx (IP0 or IP1) and IPHx Interrupt Priority Register. Note an interrupt of higher priority immediately interrupts an interrupt of lower priority. But a new interrupt with the same priority level as an ongoing interrupt must wait until the existing interrupt is completed.

Note: IPL0 and IPL1 are bit-addressable. IPH0 and IPH1 are not bit-addressable.

No priority level is assigned to the NMI. It takes precedence over all other interrupts.

IP1 Interrupt Priority Register **Read/Write**

Addr.	Bit7							Bit0	Reg.	R/W
F8h	INT13	INT12	INT11	INT10	INT9	INT8	INT7	INT6	IPL1	R/W
F9h	INTH13	INTH12	INTH11	INTH10	INTH9	INTH8	INTH7	INTH6	IPH1	R/W

2 bits in register IP1 determine the priority of the interrupt No. x. The priority is defined as follows:

INTPRIH1.x	INTPRIL1.x	Priority
0	0	Priority 0 (lowest)
0	1	Priority 1
1	0	Priority 2
1	1	Priority 3 (highest)

Register for Bank Switching

Bank Select Register **BSEL** **Read/Write**

Addr.	Bit7							Bit0	Reg.	R/W
8Fh	EFSR	BTMD	BMDSTA	–	–	–	–	–	BSEL	R/W

ESFR	1	Special Function Register bank 1 is active
	0	Special Function Register bank 0 is active
BTMD		Boot Mode, bit to specify the program source after reset. This bit is reset only by hardware reset.
	1	Boot from program RAM
	0	Boot from ROM loader
BMDSTA		Current Boot Mode state. This bit is read only and be set only. when hardware reset and software reset
	1	Booted from program RAM
	0	Booted from ROM loader

Power Control Register

POWCON Power Control Register **Read/Write**

Addr.	Bit7							Bit0	Reg.	R/W
8Fh	–	–	–	–	GF1	GF0	PD	IDLE	PCON	R/W

GF1	1	General purpose flag bit
GF0	0	General purpose flag bit
PD		Power Down. Stops all clocks to both peripherals and the core. Only a RESET can wake up the system.
	1	Power-Down mode is entered
	0	Power Down mode is not entered
IDLE	1	Idle mode is entered
	0	Idle mode is not entered

Note: The IDLE signal is specified according to the conditional text in the documentation from MENTOR/INVENTRA. This signal is however not implemented in this device. For the PD bit, all uP internal SFRs are turned off, but that information is omitted to avoid confusion.

EOR Extended Operation Register **Read/Write**

Addr.	Bit7							Bit0	Reg.	R/W
A2h	–	–	–	TRAPEN	0	DPSEL2	DPSEL1	DPSEL0	EOR	R/W

TRAPEN		This setting of this bit decides the action to be performed when the machine code A5h is executed.
	0	Selects the TRAP instruction. This mode is used during debug mode as a software break point.
	1	Selects the MOVC ((DP++), A) instruction.
DPSEL		Different data pointers can be selected by this bit. The contents of a selected data pointer will be preserved while another one is used
DPSEL(2:0)	000	Data pointer 0 selected
	001	Data pointer 1 selected
	010	Data pointer 2 selected
	011	Data pointer 3 selected
	100	Data pointer 4 selected
	101	Data pointer 5 selected
	110	Data pointer 6 selected
	111	Data pointer 7 selected

Special Function Registers of the Microprocessor Core

SP Stack pointer **Read/Write**

Addr.	Bit7			Bit0	Reg.	R/W
81h					SP	R/W

The content of the SP-register is an address pointer to the internal 256 byte RAM. The content of the SP-register is incremented before data is stored in the RAM during a PUSH and CALL-operation. It is decremented after a data fetch to the RAM during a POP- and RET (RETI) operation. The SP-register is initialized to 00h after a reset that means the stack-data begin at address 01h in the RAM, above register bank 0. The stack pointer-value should be initialized directly after reset. The stack pointer can be read and written by software.

DPL Data Pointer Low byte **Read/Write**

Addr.	Bit7			Bit0	Reg.	R/W
82h					DPL	R/W

DPH Data Pointer High byte **Read/Write**

Addr.	Bit7			Bit0	Reg.	R/W
83h					DPH	R/W

The data pointer is a 16 bit register which can be addressed using 2 special function register addresses. The data pointer will be used for indirect register addressing of the data RAM or the program ROM and for program jumps in the program ROM address space.

PSW Program Status Word Register **Read/Write**

Addr.	D7h	D6h	D5h	D4h	D3h	D2h	D1h	D0h	Reg.	R/W
D0h	CY	AC	F0	RS1	RS0	0V	F1	P	PSW	R/W

Cy		Carry flag
AC	0	Auxiliary carry flag
F0	1	Free user bit 0
RS1/RS0		Register bank select control
	00	Bank 0 00h-07h
	01	Bank 1 08h-0Fh
	10	Bank 2 10h-17h
	11	Bank 3 18h-1Fh
0V	100	Overflow flag
F1	101	Free user bit
P		Parity bit, will be set or reset only by hardware
	1	Odd number of “1” in the accumulator
	0	Even number of “1” in the accumulator

The PSW-register is bit and byte programmable and contains information about the state of the program.

A Accumulator Register **Read/Write**

Addr.	Bit7			Bit0	Reg.	R/W
E0h					ACCU	R/W

This register is bit and byte programmable. Many command operations use this register as an auxiliary memory location for results and operands.

B B-Register **Read/Write**

Addr.	Bit7			Bit0	Reg.	R/W
F0h					B	R/W

This register is bit and byte programmable. It is used during a multiply or division operation as an auxiliary memory location for operands and results.

I/O Configuration

SIGMUX Signal Multiplexing Register **Read/Write**

Addr.	Bit7							Bit0	Reg.	R/W
88h	–	–	–	–	–	–	–	SEL_UART	SIGMUX	R/W

SEL_UART		GPIO0 and TX(UART) pins are multiplexed. GPIO1 and RX(UART) pins are multiplexed.
	0	Use pins as GPIO0 and GPIO1
	1	Use pins as TX and RX of UART

4.10 Sensor Interface Registers

Register Signal Name	Address	Bit Number	Register Name	Type	Description
SI_R0	85h	Bit 0 bits(2:1) bits (5:3)	PD_SCLPFDSM TSTMUX_SEL<2:0>	R/W	Power down SCLPF/DSM Change common mode voltage for thermal Output Test mux select
SI_R1	86h	bit 0 bit 1 bit 2 bit 3 bit 4 bit 5 bit 6 bit 7	EN_MAMP RUN_AMP TEST_AMP SI_AMPIX SEL_RPD RPDX SEL_RDISCK RDISCK	R/W	Enable amperometric measurement Run amperometric Test amperometric Enable Internal amperometric settings select register power down for SI register power for SI select register disable CK register disable CK
SI_R2	89h	Bits(4:0) bit 5 bit 6	CRT(12:8) SEL_RIPD RIPDX	R/W	Isfet bias current settings select register Isfet power down for SI register Isfet power for SI
SI_R3	8Ah	Bit 0 Bit(5:1) Bit(7:6)	SEL_RSCMODE RSCMODE<4:0> VCMSEL<2:1>	R/W	select register SCMODE register SCMODE<4:0> VCM select for ECG
SI_R4	91h	bits(2:0) bit 3 bit 4 bit 5 bit 6 bit 7	CRT(7:5) SEL_RMSL RMSL<0> RMSL<1> SEL_RPD_ADCI RPDX_ADCI	R/W	Ampero (P and N) Measuring range settings select register MSL settings register MSL<0> value register MSL<1> value Select register ADC input power down for SI register ADC input power down for SI
SI_R5	92h	bit 0 bit 1 bit 2 bit 3 bit 4 bit 5 bit 6 bit 7	SEL_RPD_AMPP RPDX_AMPP SEL_RPD_AMPN RPDX_AMPN SEL_RPD_THERI RPDX_THERI SEL_RPD_THERE RPDX_THERE	R/W	select register AMPP power down for SI register AMPP power for SI select register AMPN power down for SI register AMPN power for SI select register THERI power down for SI register THERI power for SI select register THERE power down for SI register THERE power for SI
SI_R6	93h	bits(4:0) bit5	CRT(4:0) HCMX	R/W	Ampero (P&N) Measuring capacitor settings High common-mode rejection (active low) Do not change bit 5!
SI_R7	94h	Bit(7:0)	CRT(22:15)	R/W	ISFET and AMPEROP Control voltage settings
SI_R8	A3h	bit(0) bit(1) bit(5:2) bit(7:6)	CRT(23) CRT(24) CRT(14:13)	R/W	ISFET and AMPEROP Control voltage settings ISFET and AMPEROP Control voltage settings SPARE Isfet ref voltage settings
SI_R9	A4h	bit(3:0) bit(7:4)	PICON(4:1) PICON(8:5)	R/W	Gain setting for constant current ref. Gain setting for SCLPF bias current opamp2 Do not change this register!
SI_R10	A5h	bit(3:0) bit (7:4)	PICON(12:9) PICON(16:13)	R/W	Gain setting for SCLPF bias current opamp1 Gain setting for DSM bias current opamp2/3 Do not change this register!
Si_R11	A6h	bit (7:0)	TIPG<8:1>	R/W	Gain Setting for thermal

Register Signal Name	Address	Bit Number	Register Name	Type	Description
SI_R12	A7h	Bit(0) Bits(3:1) Bits(7:4)	TIPG<9> PIDCOMP<3:1> PIDSMOP1	R/W	Gain Setting for thermal Programmable current for DSM COMPARATOR Gain setting for DSM bias current opamp1 Do not change bits <7:3>!
SI_R13	AAh	bit0 bit1 bit2 bit3 bit4 bit(7:5)	EN_RLD SEL_RPPD RPPDX SEL_REPD REPDX EPG<2:0>	R/W	Enable right leg driver Select register PRESSURE power down for SI register PRESSURE power for SI select register ECG power down for SI register ECG power for SI Gain Setting for ECG Preamplifier
SI_R14	ABh	bit(1:0) Bit(6:2) bit7	PPG<1:0> CKHPM	R/W	Gain Setting for pressure amplifier Setting for VREG voltage clock high power mode Do not change bits <7:2>
SI_R15	ACh	bit(2:0) bit(4:3) bit 5 bit 6	GPG(4:2) GPG(1:0) SEL_GP1RPD Gp1RPDX	R/W	General Purpose (GP) Amp#1 Vbias GP Amp#1 Gain select GP Amp #1 register power down for SI GP Amp #1 register power for SI
SI_R16	ADh	bit(2:0) bit(4:3) bit 5 bit 6	GPPG(9:7) GPPG(6:5) SEL_GP2RPD GP2RPDX	R/W	GP Amp #2 Vbias GP Amp #2 Gain select GP Amp #2 register power down for SI GP Amp #2 register power for SI
SI_R17	AEh	bit(2:0) bit(4:3) bit 5 bit 6	GPPG(14:12) GPPG(11:10) SEL_GP3RPD GP3RPDX	R/W	GP Amp #3 Vbias GP Amp #3 Gain select GP Amp #3 register power down for SI GP Amp #3 register power for SI
SI_R18	Afh	bits(7:0)	AlmHI	R/W	Alarm hi
SI_R19	B1h	bits(1:0) bits(7:1)	AlmHI AlmLo	R/W	Alarm hi Alarm lo
SI_R20	B2h	bits(3:0)	AlmLo	R/W	Alarm lo
SI_R21	B3h	bits(7:0)	ADC_OUT(7:0)	R	[7:0] : lower 8-bits ADC digital filter output
SI_R22	B4h	bits(3:0) bits(5:4) bits(7:6)	ADC_OUT(11:8) MSL(1:0) ALARM STATUS	R R R	[11:8] : upper nibble ADC dig. filter output SENSOR INPUT read back Alarm interrupt source read back bits

SI_R0<2:1> - common mode voltage setting for thermal block

2	1	VCM THERMAL(V)
0	0	0.4
0	1	0.5
1	0	0.6

SI_R0<5:3> = TSTMUX_SEL<2:0>

2	1	0	TO_P	TO_N	Notes
0	0	0	NONE	NONE	Default
0	0	1	CKO	DATAO	
0	1	0	VBG		
0	1	1	IOUTT		
1	0	0	VAMPHLD		
1	0	1	VOUT1	VOUT1X	(SI_FE)
1	1	0	VOUT2	VOUT2X	(SI_FE)
1	1	1	VOUT3	VOUT3X	(SI_FE)

SI_R2<4:0> = CRT<12:8> - sets ISFET bias current

12	11	10	9	8	Ibias(uA)
0	0	0	0	0	Off
0	0	0	0	1	5µA
0	0	0	1	0	10µA
…..	…..	…..	….	….	
1	1	1	1	1	155µA

SI_R3<5:1> = RSCMODE<4:0> - Register configuration mode setting.

- Mode 0 – ISFET (S1), thermal (ext) (S3)
- Mode 1 – ISFET (S1), thermal (int) (S3)
- Mode 2 – ISFET (S1)
- Mode 3 - AMPERO_N (S1), AMPERO_P (S2), thermal (ext) (S3)
- Mode 4 - AMPERO_N (S1), AMPERO_P (S2), thermal (int) (S3)
- Mode 5 - AMPERO_N (S1), thermal (ext) (S3)
- Mode 6 – AMPERO_N (S1), thermal (int) (S3)
- Mode 7 – AMPERO_N (S1)
- Mode 8 – Not used
- Mode 9 - ECG (S1), temperature (ext) (S3)
- Mode 10 - ECG (S1), temperature (int) (S3)
- Mode 11 - ECG (S1)
- Mode 12 – thermal (ext) (S3)
- Mode 13 – thermal (int) (S3)
- Mode 14 – pressure (S1)
- Mode 15 - AMPERO_P (S2), thermal (ext) (S3)
- Mode 16 - AMPERO_P (S2), thermal (int) (S3)
- Mode 17 - AMPERO_P (S2)
- Mode 18 – ADC (S1)

SI_R3<7:6> = VCMSEL<2:1> - common mode voltage (VCM) setting for ECG

2	1	VCM(V)
0	0	0.5
0	1	0.4
1	0	0.6

SI_R4<2:0> = CRT<7:5> - AMPERO P and N current measurement range

7	6	5	Range(nA)
0	0	0	200
0	0	1	100
0	1	0	50
0	1	1	20
1	0	0	10
1	0	1	5
1	1	0	2
1	1	1	1

SI_R4<5:4> = RMSL<1:0> (register mux select for sensor input)

1	0	Select
0	0	Sensor 1(S1)
0	1	Sensor 2(S2)
1	0	Sensor 3(S3)
1	1	Test Input(1)

(1) The user must set RF MUX = 0 for the test input in the Sensor Interface.

SI_R6<4:0> = CRT<4:0> - AMPERO P and N measurement capacitor size

4	3	2	1	0	CAP(pF)	Note
0	0	0	0	0	103.6	
0	0	0	0	1	105	LSB=1.4pF
0	0	0	1	0	106.4	
0	0	0	1	1	107.8	
0	0	1	0	0	109.2	
...	…	…	…	…	…	
1	0	0	0	0	126	
1	0	0	0	1	127.4	
1	0	0	1	0	128.8	
1	0	0	1	1	130.2	
1	0	1	0	0	131.6	
1	0	1	0	1	133	
1	0	1	1	0	134.4	
1	0	1	1	1	135.8	
1	1	0	0	0	137.2	
1	1	0	0	1	138.6	
1	1	0	1	0	140	
1	1	0	1	1	141.4	
1	1	1	0	0	142.8	
1	1	1	0	1	144.2	
1	1	1	1	0	145.6	
1	1	1	1	1	147	

SI_R8<1:0>,SI_R7<7:0> = CRT<24:15> - AMPERO P and N, ISFET control voltage setting

24	23	22	21	20	19	18	17	16	15	Vctrl(V)	Note
0	0	0	0	0	0	0	0	0	0	0.19	
0	0	0	0	0	0	0	0	0	1	0.192392	LSB
0	0	0	0	0	0	0	0	1	0	0.194784	0.002392
…..	…..	…..	…..	…..	…..	…..	…..	…..	…..		
0	0	1	1	1	1	1	1	1	1	0.8	
0	1	0	0	0	0	0	0	0	0	0.106	LSB
0	1	0	0	0	0	0	0	0	1	0.107741	0.001741
0	1	0	0	0	0	0	0	1	0	0.109482	
…..	…..	…..	…..	…..	…..	…..	…..	…..	…..		
0	1	1	1	1	1	1	1	1	1	0.55	
24	23	22	21	20	19	18	17	16	15	Vctrl(V)	
1	0	0	0	0	0	0	0	0	0	0.264	
1	0	0	0	0	0	0	0	0	1	0.266635	LSB
1	0	0	0	0	0	0	0	1	0	0.269271	0.002635
…..	…..	…..	…..	…..	…..	…..	…..	…..	…..		
1	0	1	1	1	1	1	1	1	1	0.936	
1	1	0	0	0	0	0	0	0	0	0.01	LSB
1	1	0	0	0	0	0	0	0	1	0.01191	0.00191
1	1	0	0	0	0	0	0	1	0	0.01382	
…..	…..	…..	…..	…..	…..	…..	…..	…..	…..		
1	1	1	1	1	1	1	1	1	1	0.497	

SI_R8<7:6> = CRT<14:13> - ISFET reference voltage setting (gate voltage)

14	13	Vref(V)	Note
0	0	2	
0	1	2.4	nom
1	1	2.8	

SI_R9<3:0> = PICON<4:1> - Gain factor for master bias current (ICON)

4	3	2	1	Multiply by
0	0	0	0	1
0	0	0	1	X
0	0	1	0	X
0	0	1	1	X
0	1	0	0	1.33
1	0	0	0	1.33
1	1	0	0	1.66
When Rext = 620K, ICON = 1µA				

SI_R9<7:4> = PICON<8:5> - Gain factor for SCLPF opamp2 bias current

4	3	2	1	Add
0	0	0	0	0
0	0	0	1	(0.3 × ICON)
0	0	1	0	2 × (0.3 × ICON)
…	…	…	…	…
1	1	0	1	13 × (0.3 × ICON)
1	1	1	0	14 × (0.3 × ICON)
1	1	1	1	15 × (0.3 × ICON)

SI_R10<3:0> = PICON<12:9> - Gain factor for SCLPF opamp1 bias current

4	3	2	1	Add
0	0	0	0	0
0	0	0	1	(0.3 × ICON)
0	0	1	0	2 × (0.3 × ICON)
…	…	…	…	…
1	1	0	1	13 × (0.3 × ICON)
1	1	1	0	14 × (0.3 × ICON)
1	1	1	1	15 × (0.3 × ICON)

SI_R10<7:4> = PICON<16:13> - Gain factor for DSM opamp2/3 bias current

4	3	2	1	Add
0	0	0	0	0
0	0	0	1	(0.3 × ICON)
0	0	1	0	2 × (0.3 × ICON)
…	…	…	…	…
1	1	0	1	13 × (0.3 × ICON)
1	1	1	0	14 × (0.3 × ICON)
1	1	1	1	15 × (0.3 × ICON)

SI_R12<0>,SI_R11<7:0> = TIPG<9:1> - Thermal current programmable gain If external bias resistor = 620kΩ then Icon = 1μA Total thermal current = ICON + Curr1 + Curr2 + Curr3. See following tables for Curr1, Curr2, and Curr3.

SI_R11<3>	SI_R11<2>	SI_R11<1>	SI_R11<0>	Curr1
0	0	0	0	0
0	0	0	1	1 × (ICON/12)
0	0	1	0	2 × (ICON/12)
…	…	…	…	…
1	1	0	1	13 × (ICON/12)
1	1	1	0	14 × (ICON/12)
1	1	1	1	15 × (ICON/12)
When Rext = 620K, ICON = 1μA				

SI_R11<5>	SI_R11<4>	Curr1
0	0	0
0	1	1 × ICON
1	0	2 × ICON
1	1	3 × ICON
When Rext = 620K, ICON = 1µA		

SI_R12<0>	SI_R11<7>	SI_R11<6>	Curr1
0	0	0	0
0	0	1	1 ×ICON
0	1	0	2 ×ICON
0	1	1	3 × ICON
1	0	0	4 × ICON
1	0	1	5 × ICON
1	1	0	6 × ICON
1	1	1	7 × ICON
When Rext = 620K, ICON = 1µA			

SI_R12<3:1> = PIDCOMP<3:1> - programmable current for DSM comparator

3	2	1	Ibias
0	0	0	(0.4 × ICON) + (ICON/40)
0	0	1	(0.4 × ICON) + 2 × (ICON/40)
0	1	0	(0.4 × ICON) + 3 × (ICON/40)
…	…	…	…
1	0	1	(0.4 × ICON) + 6 × (ICON/40)
1	1	0	(0.4 × ICON) + 7 × (ICON/40)
1	1	1	(0.4 × ICON) + 8 × (ICON/40)
When Rext = 620K, ICON = 1µA			

SI_R12<7:4> = Gain factor for DSM opamp1 bias current

4	3	2	1	Add
0	0	0	0	8µ
0	0	0	1	8µ + (0.3 × ICON)
0	0	1	0	8µ + 2 × (0.3 × ICON)
…	…	…	…	…
1	1	0	1	8µ + 13 × (0.3 × ICON)
1	1	1	0	8µ + 14 × (0.3 × ICON)
1	1	1	1	8µ + 15 × (0.3 × ICON)

SI_R13<7:5> = EPG<2:0> - ECG programmable gain

2	1	0	ECG Pre-amp gain
0	0	0	250(default) (x50,x5)
0	0	1	500 (x100,x5)
0	1	0	50 (x10,x5)
0	1	1	125 (x25,x5)
1	0	0	500 (x50,x10)
1	0	1	1000 (x100,x10)
1	1	0	100 (x10,x10)
1	1	1	250 (x25,x10)

SI_R14<1:0> = PPG<1:0>

1	0	Gain
0	0	1/0.1
0	1	1/0.2
1	0	1/0.3
1	1	1/0.4

SI_R14<6:2> - sets VREG voltage

6	5	4	3	2	VREGI(V)	VREG(V)
0	0	0	0	0	1.004	1.015
0	0	0	0	1	1.019	1.03
0	0	0	1	0	1.036	1.047
0	0	0	1	1	1.054	1.065
0	0	1	0	0	1.074	1.085
0	0	1	0	1	1.12	1.131
0	0	1	1	0	1.169	1.18
0	1	0	0	0	0.991	1.002
0	1	0	0	1	1.006	1.016
0	1	0	1	0	1.022	1.032
0	1	0	1	1	1.039	1.05
0	1	1	0	0	1.059	1.069
0	1	1	0	1	1.103	1.114
0	1	1	1	0	1.156	1.167
1	0	0	0	0	0.9775	0.9882
1	0	0	0	1	0.9916	1.002
1	0	0	1	0	1.007	1.018
1	0	0	1	1	1.024	1.035
1	0	1	0	0	1.042	1.053
1	0	1	0	1	1.085	1.096
1	0	1	1	0	1.138	1.149

SI_R15,SI_R16,SI_R17<2:0> = Vbias setting for general purpose AMP

2	1	0	Vbias
0	0	0	700mV (default)
0	0	1	600mV
0	1	0	900mV
0	1	1	800mV
1	0	0	300mV
1	0	1	200mV
1	1	0	500mV
1	1	1	400mV

SI_R15,SI_R16,SI_R17<4:3> = gain setting for general purpose AMP

1	0	Gain
0	0	0.1 (default)
0	1	0.2
1	0	0.3
1	1	0.4

The equation for the GP amp circuit is shown in Equation 2

$$V_{OUT} = Gain \times (Vbias - Vin) + Vbias \quad (2)$$

The user should try to limit the output voltage (V_{OUT}) between 0 and 1V. As an example, the equivalent input voltage to achieve a output voltage range from 0.25V to 0.7V is:

IF V_{IN} = 0.7 to 2.2V, THEN V_{OUT} = 0.7 to 0.25V.

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