User's Guide

SN6507DGQEVM Low-Emissions 500 mA Push-Pull Transformer Driver for Isolated Power Supplies Evaluation Module

ABSTRACT

This user's guide describes the evaluation module (EVM) for TI's SN6507 push-pull isolation transformer driver. This EVM helps designers analyze and evaluate performance of the SN6507 device for quick development of isolated power supplies.

In addition to the SN6507 device, this EVM contains a small form-factor transformer, simple rectifier circuit, voltage regulator, and various adjustable options. These combinations simulate a complete isolated power supply system suitable for many applications.

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Trademarks

1 Introduction

This user's guide presents a typical laboratory setup used with this EVM.

CAUTION

Do not use this EVM for isolation voltage tests even though the isolated power transformer has galvanic isolation protection of up to 2500 V. This EVM is designed for the evaluation of device operating parameters only. If a high voltage (greater than 36 V) or a high load current (greater than 500 mA) is applied anywhere in the circuit, the EVM could be damaged.

Exceeding the specified input voltage range and applying loads outside the specified output range may cause unexpected operation and irreversible damage to the EVM. If there is uncertainty as to the input voltage range, power specifications, or about using a configuration that is or is not described in this user guide, please contact a TI field representative or create a post on e2e.ti.com prior to connecting power.

2 Overview

The SN6507 evaluation module allows users to evaluate the performance and features of the SN6507 push-pull isolation transformer driver in an isolated power supply application. This includes a transformer, rectifier circuit, and an optional low-dropout (LDO) voltage regulator. The power supply input and isolated output is separated by the isolation transformer which can be de-soldered and replaced with other push-pull transformers in 6-pin and 8-pin packages that fit on the PCB's T1 footprint.

Isolated power supplies help block high voltages and prevent noise currents from entering isolated grounds and interfering with or damaging sensitive circuitry. They are required to preserve an isolation barrier in systems using isolated devices requiring discrete power supplies.

The complementary output signals (SW1 and SW2) from the SN6507 are ground-referenced, N-channel, power switches that drive the primary side of the center-tapped transformer. The secondary side of the transformer has its center-tap referenced to an isolated ground plane, and the complementary outputs are rectified through a two-diode bridge. The break-before-make feature of the two driver outputs from the SN6507 ensures that only one of the primary-side transformer windings is driven at a time. After being rectified, the DC voltage is smoothed and routed to an unregulated output to power external loads up to 500 mA, or the LM317A voltage regulator can be enabled using jumper J4. Once enabled, the regulator outputs a stable, regulated +12-VDC output by default that can also be used to drive up to 500 mA load circuits. As configured by default, the SN6507DGQEVM complies with the CISPR 32 Class B radiated emissions standard, as shown by the measurement in Figure 2-1.

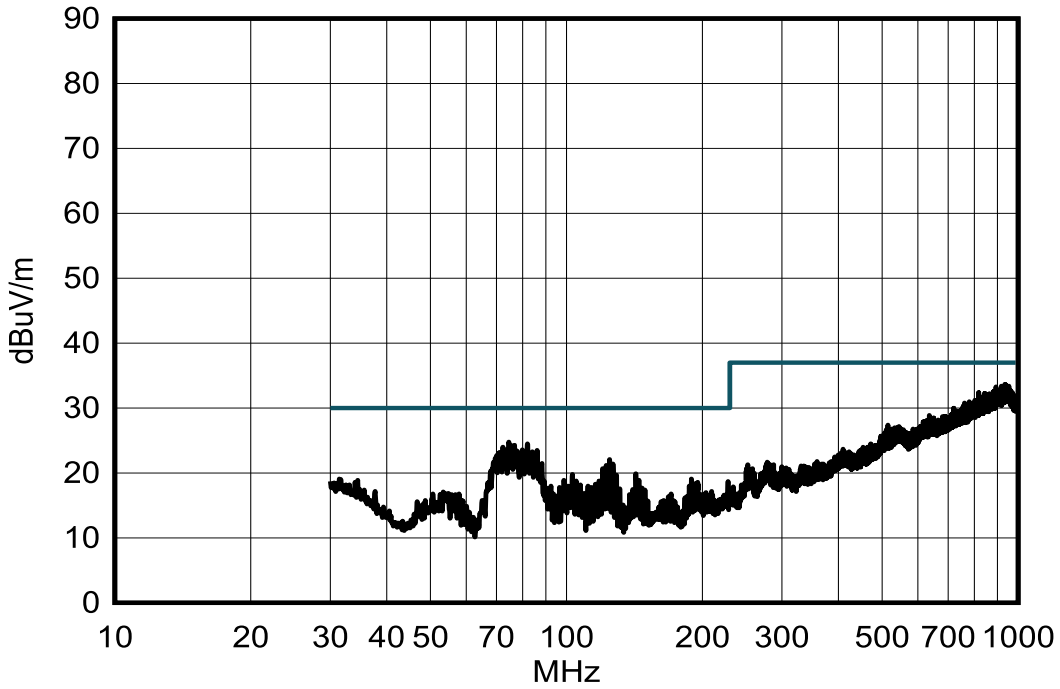

Figure 2-1. SN6507DGQEVM Radiated Emissions Sweep at Full Load per CISPR 32 Class B

Use this EVM to evaluate electrical and timing parameters of the SN6507 device in different configurations. Apply power to evaluate performance characteristics such as enable delay, rise and fall times, soft-start duration, and power consumption for different load conditions. This EVM offers provisions for a wide range of configurations, as detailed in Section 4.

3 EVM Setup and Operation

CAUTION

Note that this EVM is for operating-parameter evaluation only and not designed for isolation voltage testing. Any voltage applied above the 36-V maximum recommended operating voltage or load current applied above the 500-mA maximum recommended switching current of SN6507 may damage the EVM.

SN6507DGQ is designed to sink a maximum amount of current up to 500 mA through its SW1 and SW2 pins and connect to up to 36 V inputs. Care must be taken to ensure transformer power parameters are not exceeded if they are lower than SN6507 limits.

This section describes the setup and operation of the EVM for parameter-performance evaluation. The EVM is configured for a 24 V input and an unregulated 15 V output. It comes with an SN6507DGQ unit installed in place of U2 and a 24 V IN to 15 V, 500 mA OUT transformer in place of T1. This EVM can also be configured for evaluation of various transformers and voltage input and output combinations by replacing the included push-pull transformer device in place of T1. A list of recommended commercially available transformers is listed in the SN6507 datasheet.

Figure 3-1 shows the basic setup of the EVM with an input power supply needed to evaluate device performance. Power this Evaluation Module by connecting a voltage to VIN that is within the Recommended Operating Range in the SN6507 device datasheet. Typical voltage levels for the VIN are 24 V and 12 V, respectively. Both grounds of the EVM may be shorted together for evaluation. In practice, shorting the non-isolated and isolated grounds would bypass the isolation barrier and is not recommended.

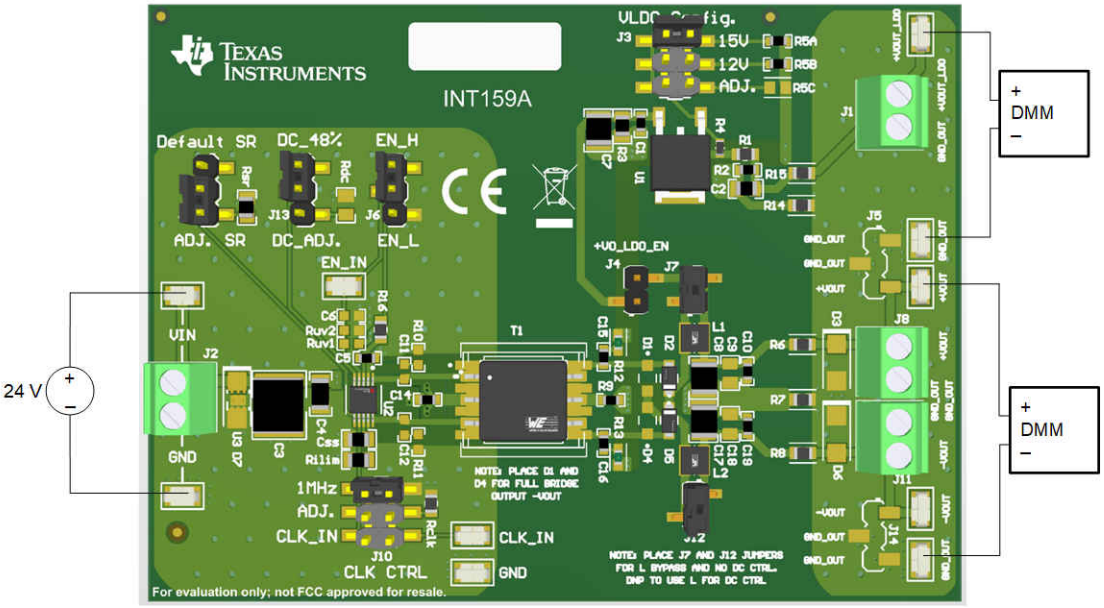

Figure 3-1. Basic SN6507DGQEVM Operation

4 EVM Configuration Options

The pin diagram of SN6507 in the DGQ package is shown in Figure 4-1.

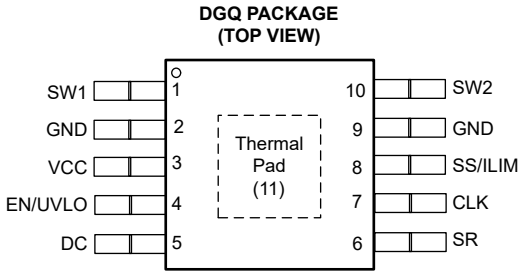

Figure 4-1. SN6507 Pinout

The SN6507DGQEVM is designed for flexibility in evaluation of the SN6507 device by providing placeholder options for several external components. The SN6507 pin-configurable options, snubber circuit components, full-bridge output configurations, LDO output, and the isolation transformer itself may all be adjusted using component-footprint and jumper provisions on this EVM. The transformer footprint, T1, is compatible with many commercially-available push-pull isolation transformers. The EVM PCB is shown in Figure 4-2.

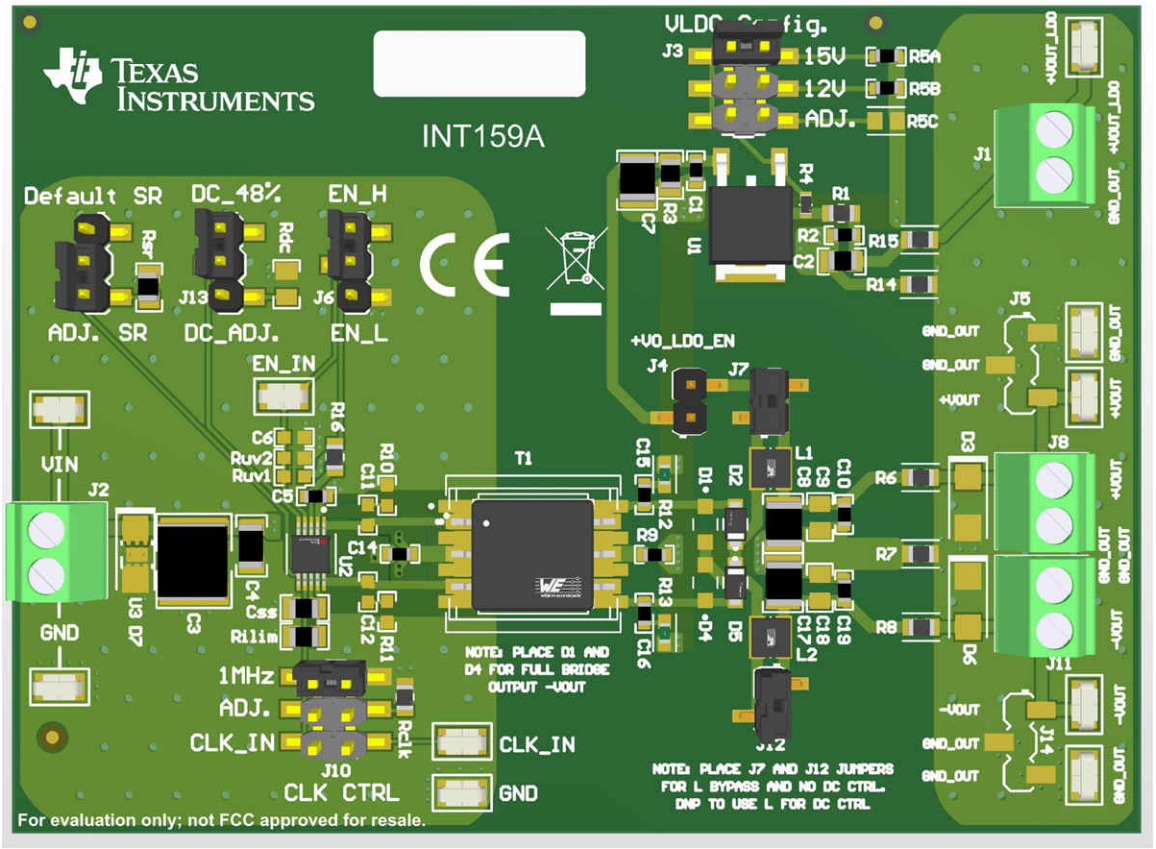

Figure 4-2. SN6507DGQEVM Top View

Details for the various configuration options of the SN6507 EVM are listed below.

Pin-configurations using RCs: Configuration options for pin-adjustable features of SN6507, including Enable, UVLO, SW1/SW2 switching frequency (CLK), duty cycle control, slew rate adjustment, soft-start time, and over-current protection limit can be found in the SN6507 data sheet. Corresponding component footprints on this EVM are as follows:

- Ruv1 and Ruv2 correspond to RENT and RENB for UVLO and EN programming

- RDC is used for duty cycle control programming and is active when pins 2-3 of J13 are connected. If duty cycle control is used, ensure a compatible transformer is placed in footprint T1 and output inductors with sufficient inductance are populated in place of L1 (and L2 as needed)
- RCLK can be used to program the internal CLK and is active when pins 3-4 of J10 are connected
- RSR is used to adjust the slew rate of the switching pins, SW1 and SW2, and is active when pins 2-3 of J9 are connected
- Rilim is used to adjust the over-current protection limit of SN6507
- Css is used to adjust the soft start time of SN6507 during power-up

Transformer replacement: A 24 V IN to 15 V OUT transformer is included by default in place of T1. To evaluate different transformers, de-solder this transformer and replace it with a 6-pin or 8-pin push-pull transformer that is compatible with the T1 footprint.

Secondary-side snubber circuit: An RC snubber circuit of 100 Ω, 62pF is populated on R12, C15 and R13, C16 by default to help minimize electromagnetic emissions. These components are optional, so they may be replaced with other components or removed from the EVM and excluded from designs using the SN6507 device.

Primary-side snubber circuits: Primary-side snubber circuits can be placed using footprints for R10, C11 and R11, C12 to further reduce emissions. Primary-side snubber circuit values can be calculated using the steps in How to Reduce Emissions in Push-Pull Isolated Power Supplies (SLLA566).

Output rectifier: Diode placeholders D1, D2, D4, D5, and resistor R9 are included to allow system designers to experiment with the different output topologies push-pull power supplies can support. D2 and D5 are populated by default as this is the typical application topology, and some example output designs found in the SN6507 data sheet can be configured on this EVM to achieve bi-polar or voltage-doubling outputs using the “-Vout” net by populating D1 and D4 on the EVM. Make sure the output LDO, U1, is bypassed by disconnecting pins 1-2 of J4 if R9 is removed since the ISO_GND potential will be floating.

Ferrite bead options: To reduce emissions when power supply outputs are connected to long cables or have high ringing, ferrites can be soldered in place of R15, R14, R6, R7, and R8. A ferrite with 1 kΩ impedance or greater at 100 MHz like the Würth Elektroniks 742792662 is recommended.

Input-side transient protection: Provisions for a flat-clamp diode like TVS3300, U3, or a TVS diode like SMAJ36A, D7, are included to protect the power supply input from external transients above the desired power supply level.

Output-side transient protections: TVS diode placeholders D3 and D6 are included to protect the SN6507 output from external transients above the desired output power supply level.

LDO output: The included LM317A can be configured to change the regulated output voltage level by connecting either of the R5x resistors using jumper J3. When configuring the LDO, ensure the LDO input voltage is within the LDO’s recommended limits and high enough to support the desired output voltage level and the dropout voltage of the LM317A. A regulated 15 V output can be configured by connecting pins 1-2 of J3, a regulated 12 V output can be configured by connecting pins 2-3 of J3, or a custom output voltage value can be configured by connecting pins 5-6 of J3 and changing R5C to a value which meets the desired output voltage using Equation 1.

$$V_{OUT} = 1.25\ V \times (1+R5C/R4) + (50\ uA \times R5C) \quad (1)$$

A table of calculated resistor values for R5C to achieve common voltage outputs is shown Table 4-1:

Table 4-1. LM317A (U1) Resistor Values for Common Regulated Output Voltages

Desired V_{OUT} (V)	R4 value (Ω)	R5C value (Ω)
3.3	240	390
5	240	713
12	240	2044
15	240	2615
24	240	4326

Table 4-1. LM317A (U1) Resistor Values for Common Regulated Output Voltages (continued)

Desired V_{OUT} (V)	R4 value (Ω)	R5C value (Ω)
36	240	6609

Jumper configurations: Table 4-2 details the jumper configuration information of the SN6507DGQEVM.

Table 4-2. SN6507DGQEVM Jumper Configurations

Connection	Label	Function
J3	15 V, 12 V, ADJ.	Connect pins 1-2, 2-3, or 5-6 of J3 to select the desired regulated output voltage of either 15 V, 12 V, or a custom value respectively between +VOUT_LDO and GND_OUT
J4	+VO_LDO_EN	Connect this jumper to enable the regulated output LDO, U1
J5	+VOUT, GND_OUT	A surface-mount 3x1 terminal block can be soldered onto this footprint for additional measurement points of each labelled pad
J6	EN_H, EN_L	Connect pins 1-2 of J6 to enable or pins 2-3 of J6 to disable SN6507 respectively. Do not connect any pins of J6 if enable signals are controlling SN6507 using TP6 or if UVLO is configured using Ruv1 and Ruv2
J7	NOTE	Connect pins 1-2 of J7 to bypass output inductor L1 if duty cycle control is not used. Disconnect these pins to use output inductor L1 for duty cycle control
J9	Default SR, ADJ. SR	Connect pins 1-2 of J9 to use the default switching slew rate of SN6507 or connect pins 2-3 to adjust the slew rate using RSR. If J9 is completely disconnected, SN6507 will use its default slew rate
J10	1 MHz, ADJ., CLK_IN	Connect pins 5-6 of J10 for SN6507 to use the internal 1 MHz clock for switching SW1 and SW2. Connect pins 3-4 of J10 to use an adjustable clock value based on the resistance of RCLK. Connect pins 1-2 of J10 to use an external clock input connected to the test point CLK_IN, described as SYNC Mode in Section 7.4.4 of the SN6507 datasheet.
J12	NOTE	Connect pins 1-2 of J12 to bypass output inductor L2 if duty cycle control is not used. Disconnect these pins to use output inductor L2 for duty cycle control
J13	DC_48%, DC_ADJ.	Connect pins 1-2 of J13 to use the default switching duty cycle of SN6507 or connect pins 2-3 to adjust the slew rate using RDC. If J13 is completely disconnected, SN6507 will use its default switching duty cycle
J14	-VOUT, GND_OUT	A surface-mount 3x1 terminal block can be soldered onto this footprint for additional measurement points of each labelled pad

5 Bill of Materials

Table 5-1 lists the bill of materials (BOM) for SN6507DGQEVM.

Table 5-1. SN6507DGQEVM Bill of Materials

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
C1, C5, C14	3	0.1 uF	CAP, CERM, 0.1 uF, 100 V,+/- 10%, X7R, AEC-Q200 Grade 1, 0603	603	GCJ188R72A104KA01D	MuRata
C2	1	10 uF	CAP, CERM, 10 uF, 35 V, +/- 10%, X5R, 0805	805	C2012X5R1V106K085AC	TDK
C3, C13	2	10 uF	CAP, CERM, 10 uF, 100 V, +/- 10%, X7S,	2220	C5750X7S2A106K230KB	TDK
C4	1	1 uF	CAP, CERM, 1 µF, 100 V,+/- 10%, X7R, 1206	1206	12061C105KAT2A	AVX
C7, C8, C17	3	10 uF	CAP, CERM, 10 uF, 50 V, +/- 10%, X7R, AEC-Q200 Grade 1, 1210	1210	UMJ325KB7106KMHT	Taiyo Yuden
C10, C19	2	0.1uF	CAP, CERM, 0.1 uF, 50 V, +/- 10%, X7R, 0603	603	C1608X7R1H104K080AA	TDK
C15, C16	2	62 pF	Ceramic Capacitor for Automotive 62 pF ±1% 100VDC X8G 0603 Paper T/R	603	GCM1885G2A620FA16D	Murata
Css	1	2.2 uF	CAP, CERM, 2.2 uF, 10 V, +/- 10%, X7R, 0805	805	GRM21BR71A225KA01L	MuRata
D2, D5	2		200 V, 2 A Silicon Germanium (SiGe) rectifier CFP3 Package 2.8 A 200 V 58 pF	CFP3	PMEG200G20ELRX	Nexperia
H1, H2, H3, H4	4		Bumpon, Hemisphere, 0.44 X 0.20, Clear	Transparent Bumpon	SJ-5303 (CLEAR)	3M
J1, J2, J8, J11	4		Conn Term Block, 2POS, 3.5 mm, TH	11x8.5x7.3 mm	1751248	Phoenix Contact
J3, J10	2		Header, 2.54 mm, 3x2, Gold, SMT	Header, 2.54 mm, 3x2, SMT	TSM-103-01-L-DV	Samtec
J4, J7, J12	3		Header, 2.54 mm, 2x1, Gold, SMT	Header, 2.54 mm, 2x1, SMT	61000218321	Wurth Elektronik
J6, J9, J13	3		Header, 2.54 mm, 3x1, Gold, SMT	Header, 2.54 mm, 3x1, SMT	M20-8770342	Harwin
L1, L2	2	33 µH	33 µH Shielded Molded Inductor 500 mA 1.33Ohm Max 1212 (3030 Metric)	SMT2_3MM0_3MM0	74438335330	Wurth
LBL1	1		Thermal Transfer Printable Labels, 0.650" W x 0.200" H - 10,000 per roll	PCB Label 0.650 x 0.200 inch	THT-14-423-10	Brady
R1, R6, R7, R8, R14, R15, R16, Rclk	8		0 Ohms Jumper 0.125 W, 1/8 W Chip Resistor 0805 (2012 Metric) Automotive AEC-Q200 Thick Film	805	RMCF0805ZT0R00	Stackpole Electronics
R2	1	10k	RES, 10 k, 5%, 0.1 W, 0603	603	RC0603JR-0710KL	Yageo

Table 5-1. SN6507DGQEVM Bill of Materials (continued)

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
R3	1	10k	RES, 10 k, 5%, 0.125 W, AEC-Q200 Grade 0, 0805	805	ERJ-6GEYJ103V	Panasonic
R4	1	240	240 Ohms ±0.1% 0.2W, 1/5W Chip Resistor 0603 (1608 Metric) Automotive AEC-Q200, Pulse Withstanding Thick Film	603	ERJ-PB3B2400V	Panasonic
R5A	1	2.61k	RES, 2.61 k, 1%, 0.1 W, 0603	603	RC0603FR-072K61L	Yageo
R5B	1	2.05k	RES, 2.05 k, 1%, 0.1 W, 0603	603	RC0603FR-072K05L	Yageo
R9	1	0	RES, 0, 5%, 0.1 W, 0603	603	RC0603JR-070RL	Yageo
R12, R13	2	100	100 Ohms ±5% 0.2W, 1/5W Chip Resistor 0603 (1608 Metric) Automotive AEC-Q200, Moisture Resistant, Pulse Withstanding Thick Film	603	SG73S1JTTD101J	KOA Speer
Rilim	1	18.2k	RES, 18.2 k, 1%, 0.125 W, AEC-Q200 Grade 0, 0805	805	ERJ-6ENF1822V	Panasonic
Rsr	1	20.5k	RES, 20.5 k, 1%, 0.125 W, AEC-Q200 Grade 0, 0805	805	ERJ-6ENF2052V	Panasonic
SH-J1, SH-J2, SH-J3, SH-J4, SH-J5, SH-J6, SH-J7	7		Shunt, 100 mil, Gold plated, Black	Shunt 2 pos. 100 mil	881545-2	TE Connectivity
T1	1		24 V: 15 V TRANSFORMER	SMT_XFRMR_9MM45_8MM50	750319696	Wurth
T1	0		Push-Pull Transformer ER9.5 SMD8 24Vin 1 MHz Output 15 V/0.5 A	SMT_XFRMR_12MM07_10MM3	TX1-ZB1459-BE	Coilcraft
T1	0		XFMR, PUSH-PULL, 10 W, 120 V-USEC, EP7, SMT	SMT_XFRMR_10MM3_13MM2	PAG6356.086NLT	Pulse Electronics
T1	0		Transformer, Turns Ratio 0.733, 430uH, 2.5kVAC, 13.2x11.8x11.1mm	SMT_XFRMR_13MM2_11MM8	SM91207L	Bourns
T1	0		Push Pull Transformer, 10:7, 550uH, 2.5kV, 8.6x9.4x9.1mm	SMT_XFRMR_8MM6_9MM4	B1807127	Bourns
TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9, TP10	10		Test Point, Miniature, SMT	Test Point, Miniature, SMT	5019	Keystone
U1	1		1% Accurate, 1.5 A Adjustable Linear Regulator with Short Circuit Protection, NDP0003B (TO-252-3)	NDP0003B	LM317AMDT/NOPB	Texas Instruments
U2	1		Low-Noise 36 V Push-Pull Transformer Driver with Duty Cycle Control for Isolated Power Supplies	PowerPAD10	SN6507DGQ	Texas Instruments

6 EVM Schematic and PCB

Figure 6-1 shows the schematic diagram for this EVM, and Figure 6-2 and Figure 6-3 show the printed circuit board (PCB) layout.

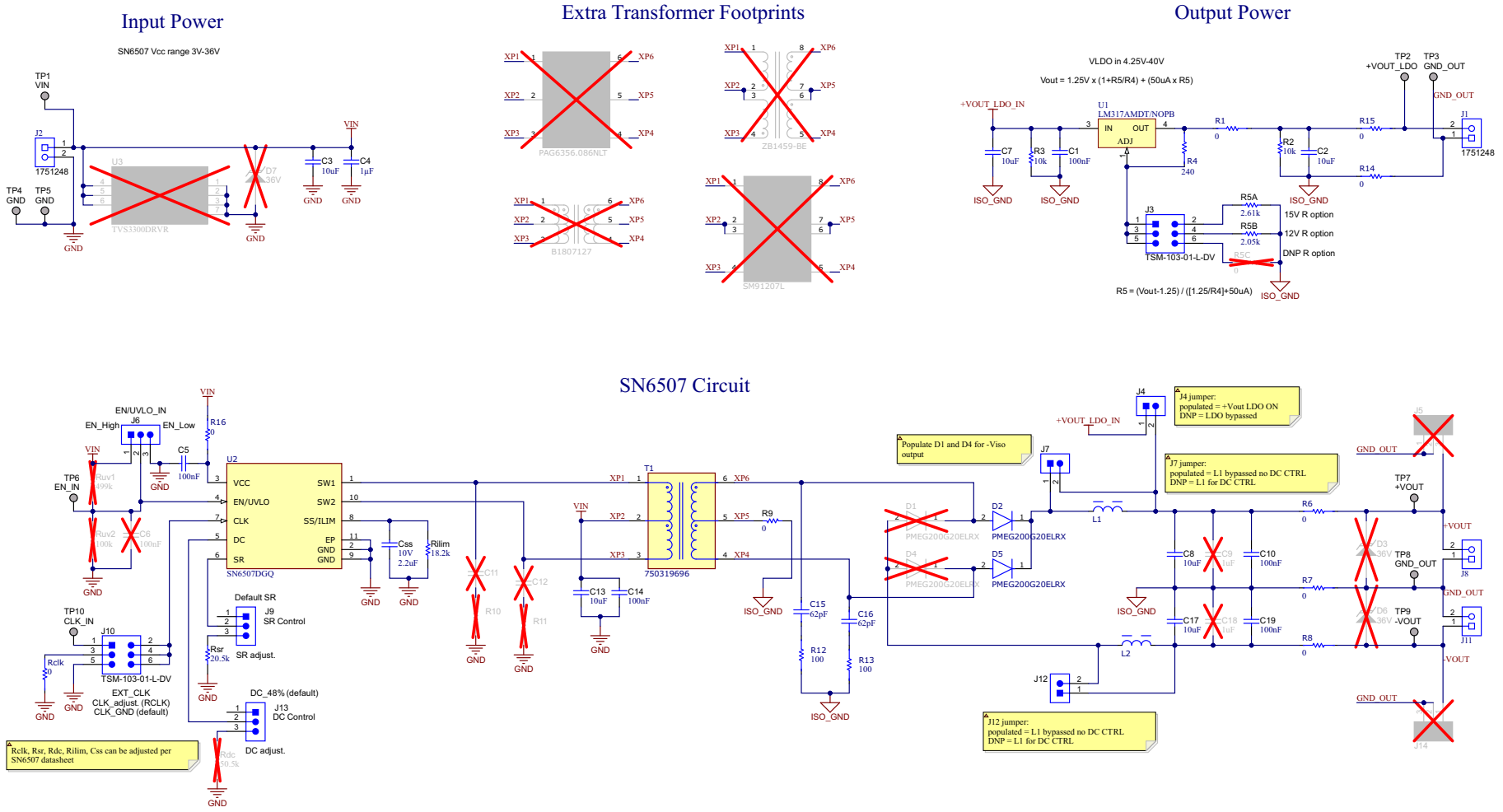

Figure 6-1. SN6507DGQEVM Schematic

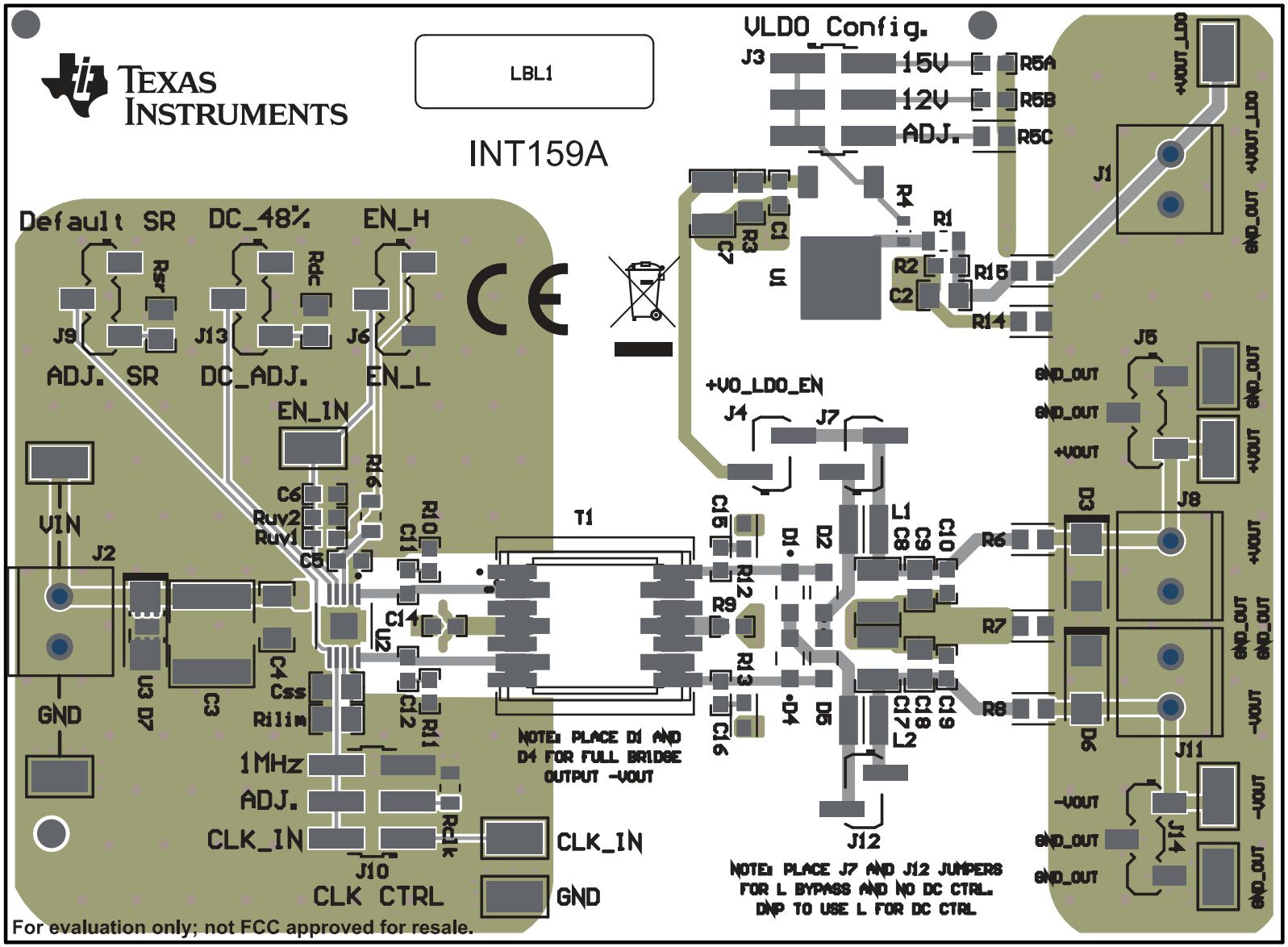

Figure 6-2. SN6507DGQEVM Top PCB Layout

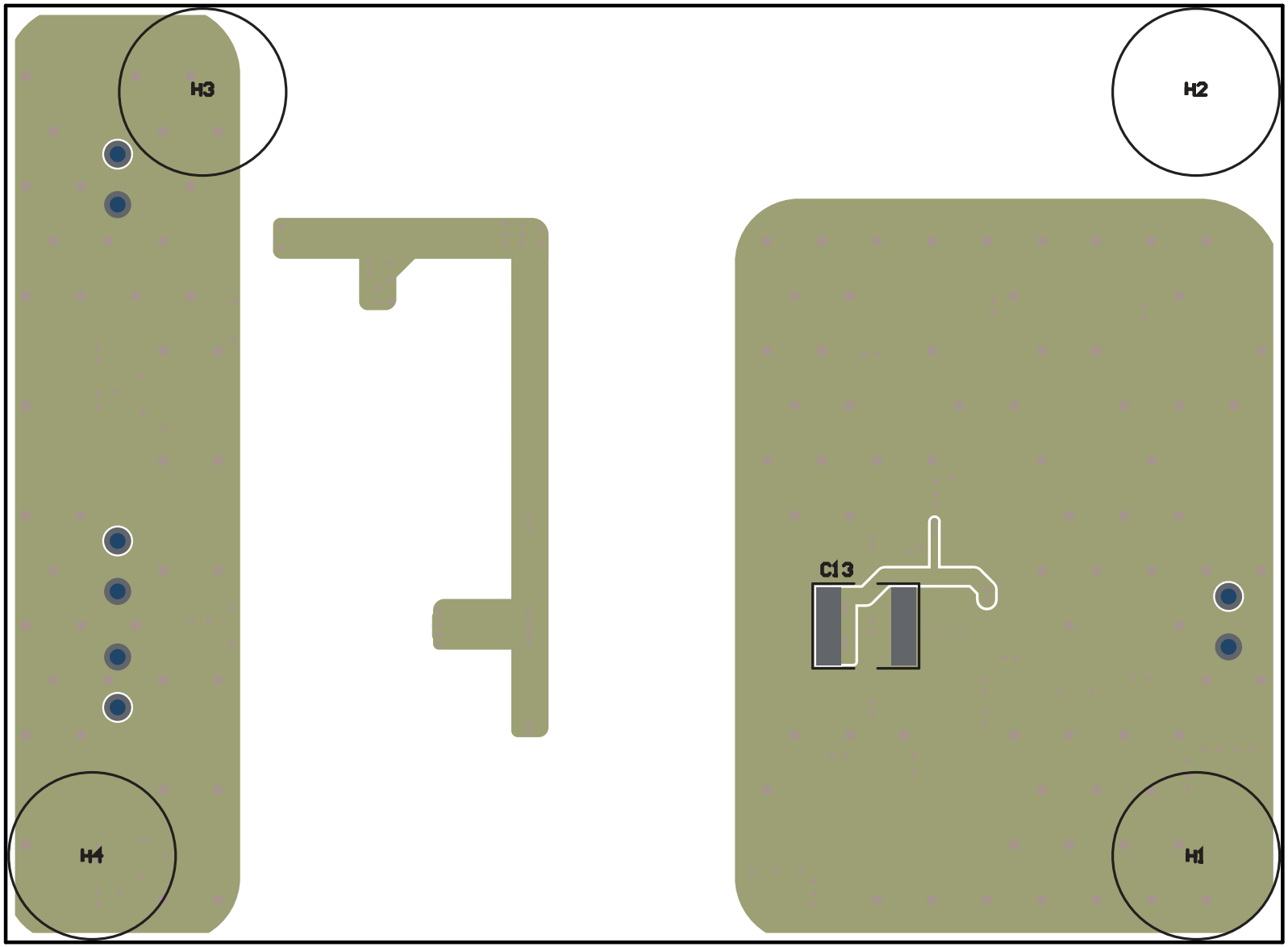

Figure 6-3. SN6507DGQEVM Bottom PCB Layout

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