Errata to TFP501, Datasheet Literature Number SLDS127B

1. **I2C drive strength**.

ISSUE

The DC digital I/O specification values for the I^2C lines on the TFP501 to support the EEPROM and Data Display Channel (DDC) are not specified in the datasheet. Also, the I2C requirement of V_{OL} 0.4V max with 3mA sink on these lines is marginal. The I2C related signals are not 5V tolerant, which is specified in the datasheet. The pin definition table has a statement about 10K pullup tolerance which is not clear.

BACKGROUND & RECOMMENDATIONS

The HDCP specification 1.0 requires an HDCP port (section 2.6, page 20) to exchange values "over the I^2C serial interface of the DVI interface". This specification references version 2.0 of the Philips Semiconductor I^2C bus specification.

The DVI specification version 1.0 specifies that the interface will contain a DDC lines. Section 1.3.1 on page 8 requires DDC2B from DDC specification version 3.

DDC version 3 defines DDC2B as I2C protocol. Refer to sections 2.3.2, 2.4.2 and 3.1.2.1. Section 6.1.6, electrical specifications indicate graphic controller (host) termination resistances of 1.5K ohms minimum to 5V, or 3mA current source. Additional 47K ohm pullup resistance is defined for the clock line at the display end. Since the protocols related to the HDCP port are I2C and since DDC2AB is not required for DVI and HDCP, the TFP501 targets I^2C specified levels. Threshold voltages are not found in the DDC specification.

E-DDC version 1 defines various DDC protocols referring to I^2C. Electrical definition remains the same as DDC version 3 with pullup resistors of $\geq$1.5K and $\leq$2.2K ohm in the host except for 47K ohm pullup resistance on the clock line in the display.

The I^2C specification version 2.1 lists electrical specifications in table 4 on page 31 for standard and fast mode devices. For devices with Vdd > 2V, V_{OL1} is 0.4V max. with 3mA sink current. Based on characterization of limited samples of the TFP501, this specification is met under typical conditions.

In section 18, the I^2C specification recognized the system need for level translation in bus systems. This section describes a level shifter using a MOSFET. The use of "DDC" in the pin names on the TFP501 is to indicate their function, not to specify they connect directly to the DDC lines of a system. While it was desired to have these pins 5V tolerant, this was not achieved in the TFP501. Level shifters as described in the I^2C bus specification or other level translators will be needed for a system implementation. Level shifters of the type in the I2C specification are one shown in the latest TFP403/501 reference design document.

I^2C low level input voltages depend on the supply voltage level, 0.3Vdd or 1.5V max for a 5V system. The TFP501 will meet this level with good margin at the 3mA drive level. Losses through the level shifter, an additional level shifter at the transmitting system end, heavier loads and longer cables may all reduce the margin in the system.

System designers should consider the external circuits needed to support compliance to the various versions of DDC in their system design.

CHANGES TO DOCUMENT TEXT:

In the "Terminal Functions" table, sheet 4, for the entries "DDC_SCL" and "DDC_SDA", change the last sentence of the "Description" column
FROM:
External pullup resistors = 10Kohm and 3.3 V tolerant.
TO:
This pin is 3.3V tolerant and will typically sink 3 mA. External pullup resistors are required. A level translator must be used to interface to 5V DDC lines.

In the "Terminal Functions" table, sheet 5, for the entries "PROM_SCL" and "PROM_SDA", change the last sentence of the "Description" column
FROM:
External pullup resistors = 10Kohm and 3.3 V tolerant.
TO:
This pin is 3.3V tolerant and will typically sink 3 mA. External pullup resistors are required.

2. **Power pad dimension**.
ISSUE

The size of the exposed metal on the PowerPad package figure is shown as larger than on production devices. When providing a thermal land, it may be smaller than assumed from the package drawing. If routing traces under the power pad, some method of protection from shorts between the traces or vias and the PowerPad should be used.

Changes to document:

Sheet 22, change the package figure as described:
a) Re-size the thermal pad dashed box from its present size to 5.05mm, centered in the package.
b) Note the dimensions and change note D:

Add dimensions to re-sized pad showing: 5.05 SQ
3.95

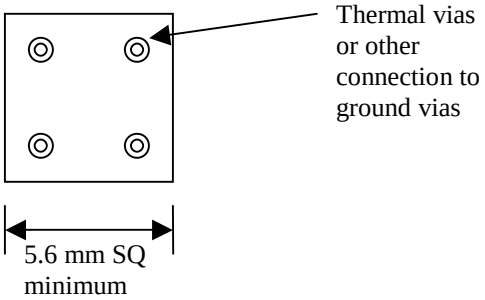
and
Change note D to read:
The package thermal performance may be enhanced by bonding the thermal pad to an external thermal plane. This pad is centered on the package and is electrically and thermally connected to the backside of the die.

Sheet 21, in the "PowerPAD…" section, add a sentence to paragraph 1, reword paragraph 2 and add figure and paragraphs between existing paragraphs 2 &3 to read:

… soldering the back side of the TFP501 to the application board is not required thermally as the device power dissipation is well within the package capability when not soldered. If traces or vias are located under the back side pad, they should be protected by suitable solder mask or other assembly technique to prevent inadvertent shorting to the exposed back side pad.

Soldering the backside of the device to a thermal land connected to the PCB ground plane is recommended for electrical and EMI considerations. The thermal land may be soldered to the exposed PowerPAD using standard reflow soldering techniques.

The recommended pad size for the grounded thermal land is 5.6mm minimum, centered in the device land pattern. When vias are required to ground the land, multiple vias are recommended for a low impedance connection to the ground plane. Vias in the exposed pad should be small enough or filled to prevent wicking the solder away from the interface between the package body and the thermal land on the surface of the board during solder reflow.



More information on this package and other requirements for using thermal lands and thermal vias are detailed in the TI application note *PowerPAD Thermally Enhanced Package Application*

Report, TI literature number SLMA002, available via the TI Web pages beginning at URL: http://www.ti.com

The following table outlines the thermal properties…

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