

# Features of TAS2770 high efficiency Class-D amplifier with I/V sense

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# ABSTRACT

The TAS2770 is a digital input Class-D amplifier ideal for small loudspeakers in applications such as portable Bluetooth speakers, personal computers, and IOT devices. While the amplifier is a mono channel device, it can be paired with other devices in order to support up to eight channels of audio. The Class-D amplifier is specified up to 15.4 W of peak power and at 11.6 W continuous power into a 4- $\Omega$  load. The device is available in both WCSP and QFN packages.

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#### Introduction

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# 1 Introduction

In addition to excellent audio performance, the TAS2770 also incorporates many additional features that improve and simplify the design process. Features of the TAS2770 include:

- Integrated voltage and current sensing
- Battery tracking limiter
- Brown out prevention
- Inter chip limiter alignment
- Highly customizable TDM/I2S input
- Configurable Interrupt
- Configurable high-pass filter (HPF)
- Adjustable volume ramp for pop and click suppression.

For ease of implementation, an app within the Pure Path Console 3 software has been developed to assist with device characterization using the TAS2770 EVM. In this document we will discuss device performance as well as explore each of the feature sets and how to use them.

# 2 Device Overview

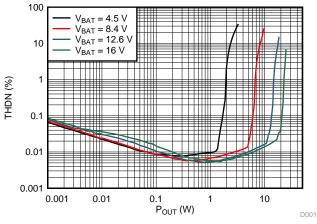
The recommended operation conditions for the device are listed below.

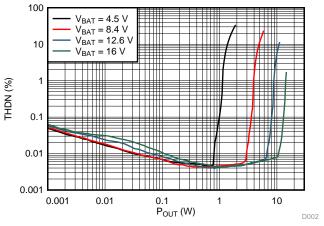
| Parameter         | MIN  | NOM                     | MAX               | Unit |
|-------------------|------|-------------------------|-------------------|------|
| AV <sub>DD</sub>  | 1.65 | 1.8                     | 1.95              | V    |
| IOV <sub>DD</sub> | 1.65 | 1.8                     | 1.95              | V    |
| VBAT              | 4.5  |                         | 16                | V    |
| V <sub>IH</sub>   |      | 0.7 x IOV <sub>DD</sub> | IOV <sub>DD</sub> | V    |
| V <sub>IL</sub>   | 0    | 0.5 * IOV <sub>DD</sub> |                   | V    |
| R <sub>spk</sub>  | 3.2  |                         |                   | Ω    |
| L <sub>spk</sub>  | 10   |                         |                   | μH   |

For the characterization data shown in this section, VBAT = 12.6 V,  $AV_{DD} = IOV_{DD} = 1.8$  V,  $f_{in} = 1$  KHz,  $F_s = 48$  kHz, Gain = 21 dBV, and  $T_A = 25^{\circ}C$  unless otherwise noted.

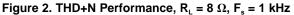


The TAS2770 shows excellent THD+N performance across the VBAT supply range for both an 8- $\Omega$  and 4- $\Omega$  load as shown in Figure 1 and Figure 2.

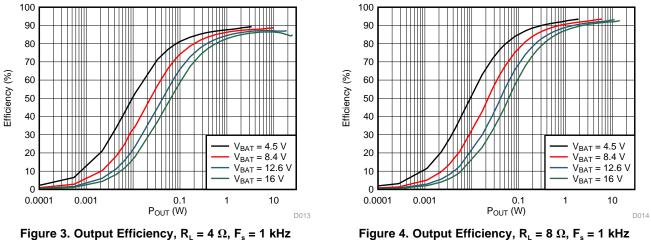








Output Efficiency for the TAS2770 is excellent as well.



=  $1 \text{ km}^2$  Tigure 4. Output Enciency,  $R_L = 0.22$ , T

For more complete performance data, refer to the TAS2770 data sheet.



# 3 Pure Path Console 3 - User Interface

Pure Path Console 3 (PPC3) is a versatile software platform that aids the user when evaluating and configuring the TAS2770. Access to this software can be requested at the device page. From the TAS2770 product webpage, follow the link as pictured below to request access to the software.

# Figure 5. Pure Path Console 3 (PPC3) Access Request

After installing the PPC3 software and launching the executable, you will be required to sign in using a my.ti.com account. This will allow you to download the TAS2770 specific app within the software package.

To get started click the panel for the TAS2770 EVM.

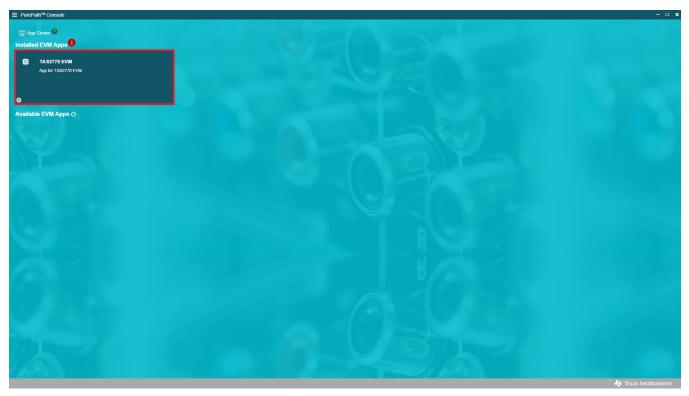


Figure 6. TAS2770 EVM Selection



# 3.1 Connect to the EVM

If no EVM is connected, the user may continue to use the App in emulation mode. This can be useful for quickly modifying device settings to export over I2C. Once a powered up EVM is connected over USB the connect button will appear in the lower left corner of the screen.

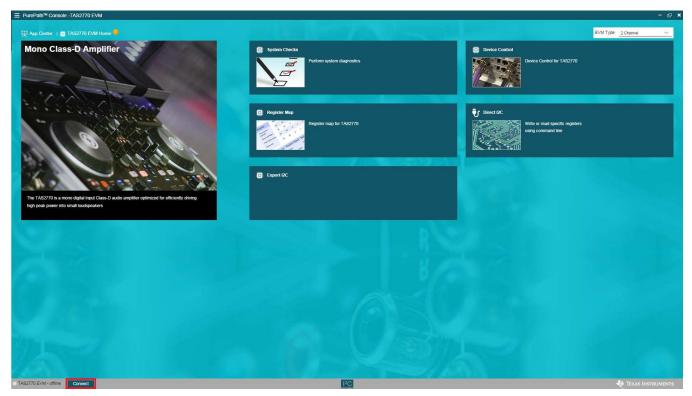


Figure 7. Connect Screen

After connecting to the TAS2770 EVM several options are available to the user to assist with device evaluation. For assistance with configuring the EVM hardware, please refer to the EVM User's Guide.



# 3.2 System Checks

A brief set of system checks are available to debug communication issues with the EVM. These can be accessed in the pane shown below.

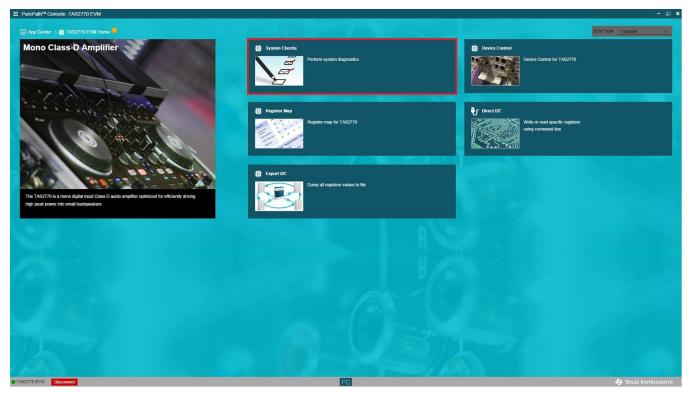


Figure 8. System Checks Pane



# 3.3 Direct I2C

Direct I2C access is available by clicking in either of the following areas within the PPC3 interface.

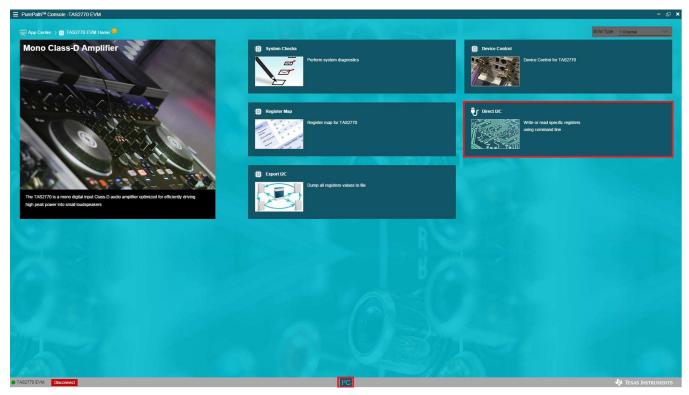


Figure 9. Direct I2C Access

This terminal allows the user to generate scripts and debug specific device settings manually. The syntax for this input is shown in the below.

Register Write Syntax:

w [i2c address] [register] [datal] [data2] ... [data k] > [data k+1] ... [data m] > [data m+1]
... [data n]

Where 'i2c address', 'register' and 'data x' are in hexadecimal format and n is less than or
equal to 32.

Register Read Syntax:

r [i2c address] [register] [read amount]

Where 'i2c address', 'register' and 'read amount' are in hexadecimal format and read amount is
less than or equal to 32 (0x20).
Interface Syntax:



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i [interface] Where 'interface' is i2cstd, i2cfast, spi8, spi16, or gpio. \_\_\_\_\_ Breakpoint Syntax: b ["string"] Where "string" can be any string of characters to be displayed at a pop-up message. \_\_\_\_\_ Delay Syntax: d [milliseconds] Where "milliseconds" is the delay time in decimal format. Wait for Flag Syntax: f [i2c address] [register] [D7][D6][D5][D4][D3][D2][D1][D0] Where 'i2c address' and 'register' are in hexadecimal format and 'D7' through 'D0' are in binary format with values of 0, 1, or X for don't care.

-----



# 3.4 Register Map

The Register Map panel provides an informative alternative to the Direct I2C terminal. By using this feature the user is able to navigate through the various registers.

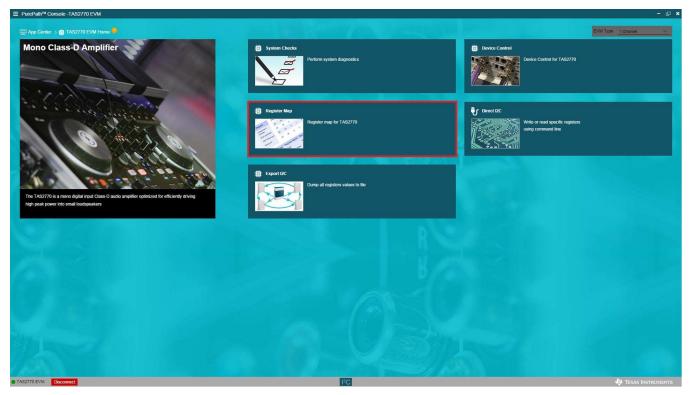


Figure 10. Register Map Access

A brief summary for each control is available and the user is able to manually toggle bits. In both Direct I2C terminal and in Register Map the user has the freedom to control any register at any time. Care should be taken to ensure the device is in shutdown mode before changing critical settings.



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|                             |   |              |       |   |            |   |   |      | Read A | dl Registers | Page Q ▼ | Fields                   |           |  |
|-----------------------------|---|--------------|-------|---|------------|---|---|------|--------|--------------|----------|--------------------------|-----------|--|
| egister Name 41             | Q | Address #1 Q | Value | 7 |            |   | E | lits | 2001   | 2020         | 1.46     | Power Control            |           |  |
| Book0_Page0                 |   |              |       | 1 | ь          | ь | 4 | 3    | 4      |              | 0        | Field                    | Value     |  |
| Page                        |   | 0×00         | 0x00  | 0 | 0          | 0 | 0 | 0    | 0      | 0            | 0        | Reserved [7:5]           |           |  |
| Software Reset              |   | 0x01         | 0x01  |   |            |   |   |      |        |              | - 9 I    | Reserved                 |           |  |
| Power Control               |   | 0x02         | 0x02  |   |            |   |   | 0    | 0      | 1            | 0        | ISNS Power Down          | 0         |  |
| Playback Configuration Rep0 |   | 0x03         | 0x10  |   | 0          | 0 |   | 0    | 0      | 0            | 0        | VSNS Power Down          | 0<br>0×02 |  |
| Playback Configuration Reg1 |   | 0x04         | 0x00  |   |            |   | 2 | 2    | 0      | 0            | 0        | Operational Mode [1:0]   | 0x02      |  |
| Playback Configuration Reg2 |   | 0x04         | 9x00  | 0 |            | 0 |   | 0    | 0      | 0            | 0        | Description              |           |  |
|                             |   |              |       | 0 | 0          |   |   | 0    | 0      | 0            | 0        | Reserved                 |           |  |
| Playback Configuration Reg3 |   | 0×06         | 0x00  | 0 | 0          | 0 | 0 |      | 0      |              |          | Reserved                 |           |  |
| Misc Configuration Reg0     |   | 0×07         | Oxc6  | 1 | <u>(†)</u> | 0 | 0 | 0    | 1      |              | 共        | Current sense power down |           |  |
| PDM Input Reg0              |   | 0×08         | 0×00  |   | 0          | 0 | 0 | 0    | 0      |              | 0        | Voltage sense power down |           |  |
| PDM Configuration Reg1      |   | 0×09         | 0x08  | 0 | 101        | 0 |   | 1    | 00     | 0            | 10       | Device operational mode  |           |  |
| TDM Configuration Reg0      |   | 0x0A         | 0x07  |   |            | 0 | 0 | 0    | 1      | 1            | 1        |                          |           |  |
| TDM Configuration Reg1      |   | 0x08         | 0x02  |   | 0          | 0 | 0 | 0    | 0      | 1            | 0        |                          |           |  |
| TDM Configuration Reg2      |   | 0x0C         | 0x0a  | 8 | 0          | 0 | 0 | 1    | 0      | 1            | 0        |                          |           |  |
| TDM Configuration Reg3      |   | 0x0D         | Dx1D  | 0 | 0          | 0 | 3 | 0    | 0      | 0            | 0        |                          |           |  |
| TDM Configuration Reg4      |   | 0×0E         | 0x/3  | 1 | 1          | 1 | 5 | 0    | 0      | 1            | 4        |                          |           |  |



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# 3.5 Export I2C

Once all settings have been configured as desired, the user can use this feature to generate a .h file or a .cfg file (in the same format as I2C terminal) to assist with end system integration.

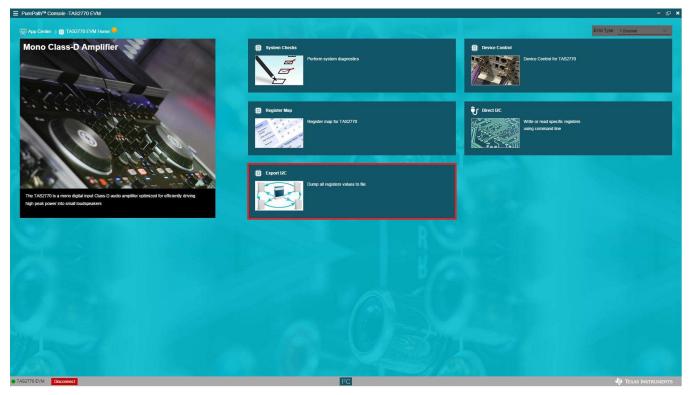


Figure 12. Export I2C Pane



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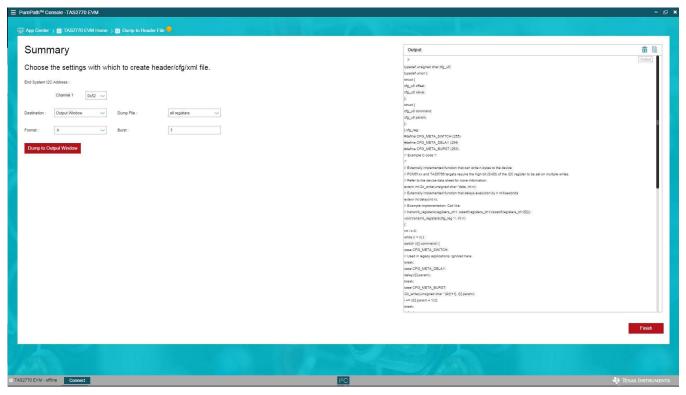


Figure 13. Summary Screen

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# 3.6 Device Control

To access Device Control click the panel shown below on the home screen.

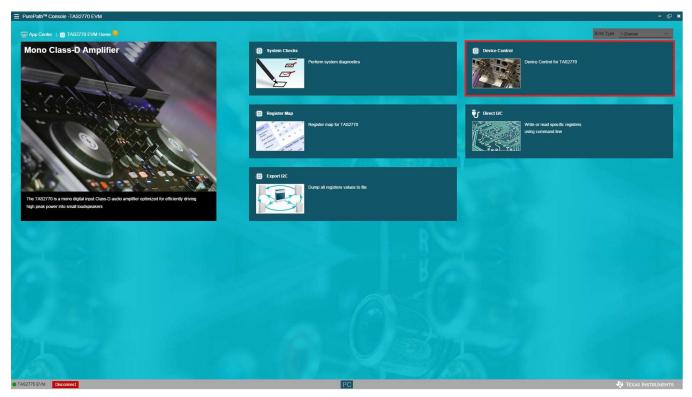


Figure 14. Device Control

Some advanced controls are automatically set in the standard view, but advanced control can be activated by clicking the icon indicated below. This GUI view groups related settings and features to provide quick setup without needing to refer to the register map. It is recommended to setup features like the Brown Out Prevention and Battery Tracking Limiter in this view.



|   |  |  | - e ,                                      |
|---|--|--|--|
| 强 App Center 🔉 👩 TAS2770 EVM Home 🖇 🗃 Device Control 🧧  | Basic Advanced                               | States and the states of the s | Data Read IRQ 🕑 Power Up                   |
| Limiter and Brown-Out Protection  | wn Brown-Out Battery Guard Volume Control    | Volume Ramp Rate<br>0.5 dB per 1 sample  | Amplifier Level                            |
| Paris Cur C S   | 0 dB<br>✔ Sample Rate Auto Detect            | Sample Rate<br>44.1/48.1/12  | - 19.0 dBV<br>Sample Ramp Rate<br>40 KHz ~ |
| 4<br>0<br>0<br>0<br>0<br>4<br>2<br>8<br>0<br>120<br>120<br>120  | Playback Source<br>PCM                       | PDM SBCLK / FS Auto Detect   | SBCLK / FS Ratio 0<br>256 ~                |
| VDA((V)   | PCM  |  |  |
| Infection Point Threahold Max Atten<br>10.8 V 5 V 13 V<br>Hold Time Abask Rate Release R  | 9 dB 2                                       | <u> </u>   |  |
| Stope         Attack Stop Stop         Reference         1000 mail           1         -         0.5 cm         0.5 cm         0.6 cm |  |  |  |
| Brown-Out Protection     On   |  |  |  |
|   |  |  |  |
| Miscellaneous   | три  | Receiver Transmitter   |  |
| Class D Synchronization mode  Univ EM Spread Spectrum   | Edge polarity<br>Rising edge of SBCLK        | Justification  |  |
| Over Temperature Retry         Over Current Retry           Do Not Retry         Do Not Retry   | <u> </u>                                     |  |  |
| Enable V-Sense Enable I-Sense   | Frame Start Polarity<br>High to Low on FSYNC | Vord Length  | Slot Length<br>32 bits                     |
|   | Receiver Offset                              | Left Channel Time Slot<br>0  | Right Channel Time Slot                    |
| TAS2770 EVM Deconnect   | Slot Select Confin                           |  | TEXAS INSTRUMENTS                          |

Figure 15. Advanced Control

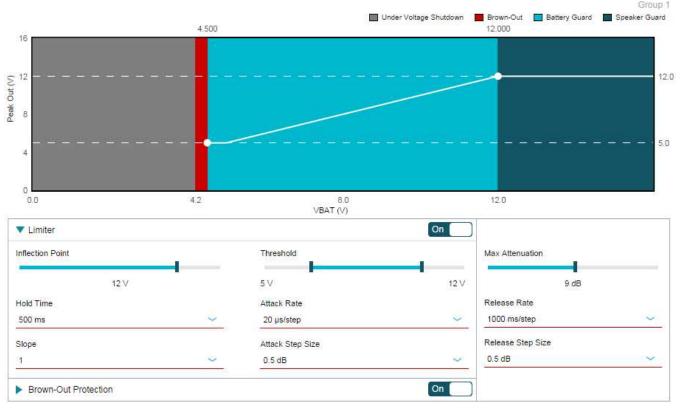
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# 3.6.1 Battery Tracking Limiter

The TAS2770 also incorporates a battery tracking limiter with automatic gain control (AGC). VBAT is continuously monitored and compared against the limiter settings. The intent of this feature is to limit power consumption at lower voltages as well as to prevent distortion and clipping that may result from the intended output signal exceeding the output range for a given VBAT voltage. A sample configuration is shown in the figure below.

#### Limiter and Brown-Out Protection



# Figure 16. Sample Configuration

In the above example, the maximum output level for all valid VBAT voltages will be 12 V. However, once VBAT drops below the 12-V inflection point the AGC will take control to further limit the output. Once VBAT reaches 5 V, AGC will stop adjusting the gain maintaining a lowest maximum of 5 V. The slope setting will dictate how rapidly the AGC limits output voltage relative to VBAT level.

Additional settings for the limiter include attack rate & step size, release rate & step size, and hold time. When the limiter is activated or released, the rate and step size will dictate how aggressively the adjustment is made. Too rapid of an adjustment up or down may be detectable by the listener. The hold time also helps to prevent pumping effect that can be caused by the limiter constantly activating and releasing when VBAT experiences ripple or droop.



#### 3.6.2 Brown Out Prevention

A related feature to the limiter is brown out prevention (BOP). When this function is activated, the amplifier will either enter shutdown mode or limit the gain based on the Max Attenuation setting. The threshold can be set so that the device will enter the selected state to help prevent too much current draw from the supply. Similar to the voltage limiter, the attack rate, step size, and hold time settings can be independently set. If desired, the amplifier can be set to enter an infinite hold state where BOP will not be released until the setting is reset. An example configuration is shown in the figure below.

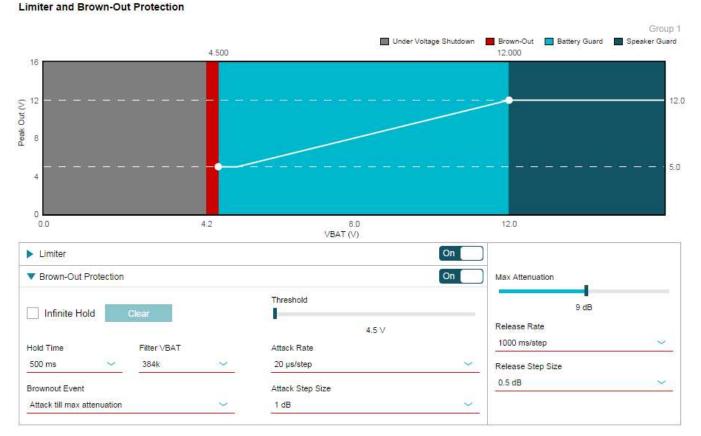


Figure 17. Brown Out Prevention



# 3.6.3 Customizable TDM/I2S Interface

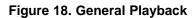
General playback, transmitter, and receiver settings of the TAS2770 can be customized to match the host configuration. The TAS2770 is capable of supporting up to eight independent channels on a single TDM interface.

# 3.6.3.1 General Playback

There are several features in the general playback settings. The user is given control over digital volume control as well as amplifier gain and volume ramp rate. Also, the device may be configured for specific bit clock and frame clock frequencies. To simplify configuration and prevent possible audio artifacts from mismatched clocking, the device has both sample rate and bit clock to frame ratio auto detect functions. The device may also be configured to use the standard I2S/TDM interface (PCM) or use PDM input to control audio playback.

#### Playback

| Volume Control          | Volume Ramp Rate<br>Volume ramping disabled | ~ | Amplifier Level  |   |  |
|-------------------------|---|---|------------------|---|--|
| 0 dB                    |   | 2 | 19.0 dBV         |   |  |
|                         | Sample Rate                                 |   | Sample Ramp Rate |   |  |
| Sample Rate Auto Detect | 44 <mark>.1/4</mark> 8 kHz                  | ~ | 48 KHz           | ~ |  |
| Playback Source         |   |   | SBCLK / FS Ratio |   |  |
| PCM PDM                 | SBCLK / FS Auto Detect                      |   | 256              | ~ |  |





#### 3.6.3.2 Receiver Settings

The receiver settings allow the user to adjust the bit edge polarity, frame edge polarity, justification, word length, slot length, offset, and channel settings. The supported word lengths are 16, 20, 24, and 32 bits and the supported slot lengths are 16, 24, and 32 bits. The slot length defines the number of bits allocated per channel, while word length specifies the number of valid data bits in the slot.

Another feature of the device is automatic slot assignments based on I2C addressing. When multiple devices are used in a system, they each require separate I2C addressing. The default setting for the device will use the I2C address specified by the mode pin connection to automatically configure itself to use the respective word slot. If desired, this function can be overridden to configure the device to play left, right, or a down-mixed combination of the two. Left and right channels can be assigned to any of the eight TDM word slots.

An example receiver configuration is shown in the figure below.

| ТDМ                                  |        |                | Receiver | Transmitter |                         |   |
|--------------------------------------|--------|----------------|----------|-------------|-------------------------|---|
| Edge polarity                        |        | Justification  |          |             |                         |   |
| Rising edge of SBCLK                 | ~      | Left           |          | ~           |                         |   |
|                                      |        |                |          |             |                         |   |
|                                      |        |                |          |             |                         |   |
| Frame Start Polarity                 |        | Word Length    |          |             | Slot Length             |   |
| High to Low on FSYNC                 | ~      | 24 bits        |          | ~           | 32 bits                 | ~ |
| Receiver Offset                      |        | Left Channel T | ime Slot |             | Right Channel Time Slot |   |
| 1                                    |        | 0              |          |             | 1                       |   |
| Slot Select Config                   |        |                |          |             |                         |   |
| Mono with slot as I2C address offset | $\sim$ |                |          |             |                         |   |

Figure 19. Receiver Configuration



#### 3.6.3.3 Transmitter Settings

The outputs of the TAS2770 include voltage and current sensing data, decimated PDM inputs, VBAT voltage, temperature, and gain as set by the limiter. The location of this data does not necessarily have to be confined to the devices word slot as set in the receiver settings. Care should be taken to not overlap data when using multiple devices in a single system. The unused bit configuration can be set to either Hi-Z or '0' for any device. If multiple devices are connected together, the Hi-Z setting should be used on each to prevent conflicting control of the data line. There is also a bus keeper configuration setting to help manage the state of the output signal. It will maintain the state of the output as last driven by any of the connected devices until any of the devices attempts to transmit data. It is recommended to only enable this function on a single device on any shared output line.

Pure Path Console 3 - User Interface

VBAT voltage, temperature, and sample rate are also available to poll over I2C if constantly updated feedback is not needed. PPC3 will automatically poll I2C for these registers and show live updates in the data read pane.

| Data Read   |   |             |           |        |
|-------------|---|-------------|-----------|--------|
|             |   |             | Channel 1 | $\sim$ |
| Sample Rate | : | 44.1/48 KHz |           |        |
| VBAT        | : | 14.066 Volt |           |        |
| Temperature | : | 27.063 °C   |           |        |

# Figure 20. Data Read Pane

An example transmitter configuration is shown in the figure below.

| Receiver                    | Transmitter   |   |
|-----------------------------|---|---|
|                             |   |   |
|                             |   |   |
| VBAT Time Slot Length       |   | Transmitter Offset  |
| Truncate to 8-bits (1 slot) | <u> </u>  | 1   |
| ✓ Bus Keeper Config         |   | ✓ LSB Config  |
|                             | Enable  | Slot  |
|                             | ✓   | 4   |
|                             | ✓   | 0   |
|                             |   | 8   |
|                             |   | 12  |
|                             |   | 16  |
|                             |   | 20  |
|                             | VBAT Time Slot Length<br>Truncate to 8-bits (1 slot)<br>Use Keeper Config | VBAT Time Slot Length<br>Truncate to 8-bits (1 slot)<br>Bus Keeper Config<br>Enable |

# Figure 21. Example Transmitter Configuration



### 3.6.4 Adjustable Volume Ramp for Pop and Click Suppression

As mentioned in the general playback settings, there is control for the digital volume ramp rate. This setting will adjust how quickly the device ramps to the volume setting at mute and un-mute. This feature helps reduce pop and click as a result of enabling the outputs and comfortably increases volume to user preference.

An example of outputs being enabled without volume ramp rate control is shown in Figure 22 and can be compared to volume ramping slowly in Figure 23.

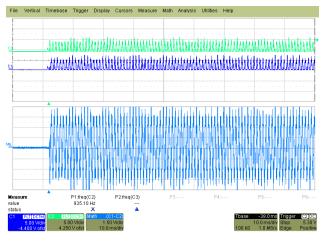


Figure 22. Volume Ramp Rate Control Disabled

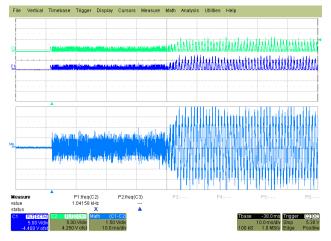


Figure 23. Volume Ramp Rate Control Enabled



### 3.6.5 Integrated Voltage and Current Sensing

The TAS2770 has built in voltage and current sensing that may be beneficial for use in load sensing for advanced audio shaping and control. The measured values from the device may be set to output on SDOUT along with Decimated PDM input, VBAT voltage, Die Temperature, and Limiter Gain.

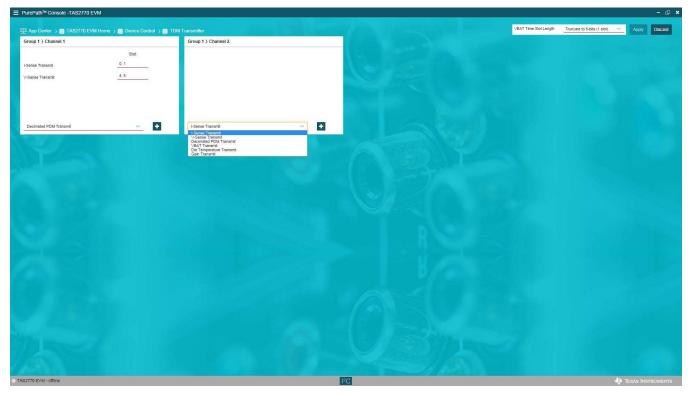


Figure 24. Integrated Voltage and Current Sensing Setting

The voltage and current values each will be output in 16-bit words. Within PPC3, SDOUT is broken into up to 64 separate 8-bit slots. PPC3 will assist the user to ensure no two outputs overlap. If programmed carefully, the host can poll for data in the appropriate region of the TDM word cycle. The USB interface for the TAS2770 EVMs will expect data in 32-bit intervals. To record both I sense and V sense separately using the USB interface on the EVM, the data should be separated by two empty slots as shown in the figures below.

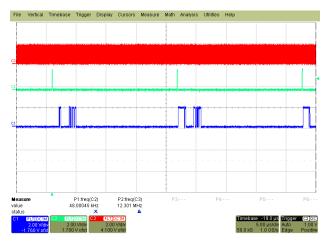


Figure 25. I Sense and V Sense on EVM USB Interface



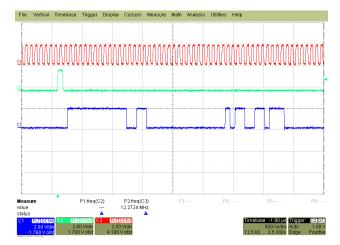


Figure 26. I Sense and V Sense on EVM USB Interface - Zoomed

# 3.6.6 Inter Chip Limiter Alignment (ICLA)

When using multiple devices, it is possible that one channel will have its limiter activate while another device does not require adjustment based on the loudness of the content that each channel is playing. If one limiter is allowed to activate without communicating to the other devices, the result will be an alteration of audio balance. This may result with an undesirable listening experience. To prevent this, multiple channels may be grouped together for limiter alignment. Each device in a group will both broadcast gain as well as track the transmitted gain of the other devices in the same group. Three modes are available to the user to align the limiter gains. The first mode will use the minimum attenuation. In this case if any one device is not limiting output, then none of devices in the same group will. The second mode is to use the minimum non-zero attenuation. In this case, the group will ignore gain data from any device that is not attenuating and will assume the least aggressive limiter output. The last setting will use the gain setting from the device with the maximum attenuation output.

To use this function, each device in a group needs to output gain to consecutive output slots. Each device can then be configured with the location of the first slot in the group and how many consecutive slots to read.

A sample configuration is shown below for eight devices using the maximum attenuation. The first device is expected to transmit gain in slot 0.

| Inter Chip Limiter Alignment |   |                    |             |    |  |  |
|------------------------------|---|--------------------|-------------|----|--|--|
| ICLA Alignment Config        |   | Starting Time Slot | Slot Enable |    |  |  |
| Use maximum                  | ~ | 0                  | 8           | 28 |  |  |
|                              |   |                    |             |    |  |  |

Figure 27. Inter Chip Limiter Alignment



# 3.6.7 Configurable Interrupt

There are several conditions that the TAS2770 will detect as interrupts which may cause the device to enter shutdown. They are shown in the figure below and can be polled by reading back the I2C registers. There are registers for both live conditions and latched conditions. Once set, the latched register will maintain state until it is read back.

These interrupt flags will set the IRQ pin output level to either high or low based on user settings. This can be used for immediate feedback to the host. In addition, each of the interrupt flags can be masked from generating this output signal.

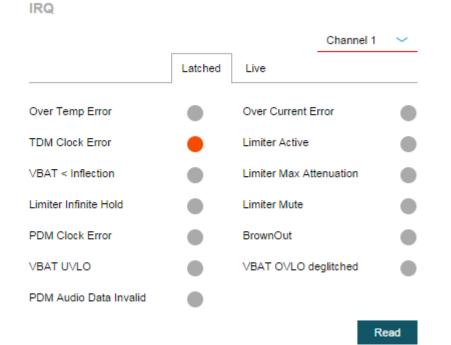


Figure 28. Configurable Interrupts



# 3.6.8 Configurable High-Pass Filter (HPF)

One final feature of the TAS2770 is a configurable high-pass filter (HPF). The HPF allows the user to remove low frequency content from the output. The filter settings are bypass, 2 Hz, 50 Hz, 100 Hz, 200 Hz, 400 Hz, and 800 Hz.

This feature is useful in limiting output power and extending battery life. Some speakers may be unable to efficiently reproduce audio below the set frequency and any signal below a certain threshold results in wasted power. The filter can be set as low as 2 Hz so that in effect the only portion of the signal blocked is DC offset in the signal.

|   | $\sim$ |   |
|---|--------|---|
| - | انا    | V |
|   | -      |   |

| HPF Corner Frequency(Hz)            |   |  |
|-------------------------------------|---|--|
| Bypass                              | ~ |  |
| 2<br>50<br>100<br>200<br>400<br>800 |   |  |
| Bypass                              |   |  |

# Figure 29. High-Pass Filter Configuration

# 4 References

- TAS2770 Data Sheet (SLASEM6)
- TAS2770 EVM User's Guide (SLOU508)

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