"Hot Plug-in" In-rush Current Limiting Circuits for Power Trends' DC-DC Converters

In-rush current is the initial current that flows to the converter's input de-coupling capacitor(s) when the host board assembly is connected to an active input power source. The magnitude of the in-rush current is high and can induce arcing, transients, and erosion of the connector. Limiting the in-rush current allows the host board assembly to be safely plugged into a live system backplane connector, such as those powered from a -48V central office power supply.

An active in-rush limiting circuit powers up prior to the converter and controls the in-rush current by limiting the rate in which the input voltage, V_{in} is applied to the input de-coupling capacitor(s), C_{in}. Under these conditions the input current, I_{in} is determined by the following equation.

$$I_{in} = \frac{C_{in} \cdot dV_{in}}{dt} \qquad \text{Eq. 1}$$

An n-channel MOSFET is commonly used as the controlling element, which is placed in series with the input source negative return. The rate-of-rise of V_{in} is controlled by adding capacitance across the MOSFET drain and gate. This limits the transistor's dV_{ds}/dt when the gate is driven from a low-level current source. Once the input capacitors are fully charged, the control circuit then enables the converter output by releasing its "Inhibit" pin.

Comparator Application Circuit

The circuit of Figure 1 is one of two circuits described (see also Figure 3). It uses a low-cost micro-power comparator (U_1) as an under-voltage lockout. The comparator senses the applied input voltage ($-V_{EE}$) via R_1 and R_2. When a valid input voltage is detected, the comparator provides a signal to slowly turn on the power MOSFET (Q_2). The "On" threshold is set at –38V, and a 3V hysteresis provides a corresponding "Off" threshold of -35V. C_1 is added to provide filtering for contact bounce. The supply current to U_1 is provided by resistors R_3 and R_4, which combined with the zener diode (VR_1) gives U_1 a supply voltage of 10V.

The turn-on rate of Q_2 is controlled by the capacitor C_2. The gate current is limited by R_9, and C_2 adds the required rate feedback to control the dV/dt at Q_2's drain. The 'Inhibit' to the converter (PT3320) is controlled by the p-channel JFET, Q_1. Q_1 remains on until until the end of the in-rush charge period. At this point Q_2 has pulled '$-V_{in}$' below Q_1's gate, turning Q_1 off and allowing the PT3320 to power up. Q_1 is senstive to input voltage transients, which induce a corrsponding current surge through the input capacitor C_{in}. This momentarily raises Q_2's V_{ds}(on), thereby depleting the Vgs of Q_1 below its "pinch-off" voltage. This can turn Q_1 on, which toggles the PT3320's "Inhibit". C_4 solves this problem by ac-coupling the drain and gate of Q_1 to prevent these transients from affecting the converter's "Inhibit". The principal design equations for this circuit are described by equations 3 and 4, herein.

Figure 2 shows the typical start-up waveforms for the circuit of Figure 1 using a PT3323 converter. The waveforms are in response to the application of -50V between GND and $-V_{EE}$.

Figure 2

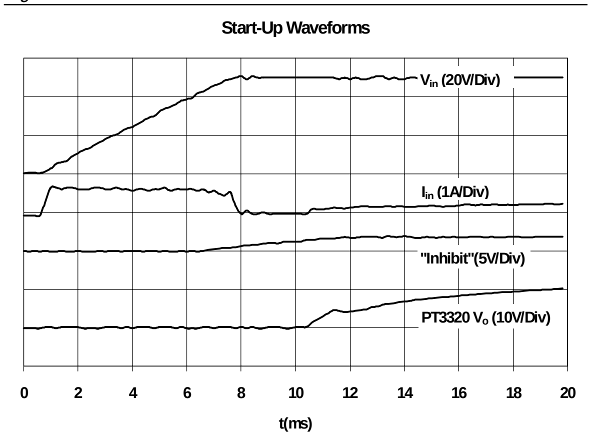
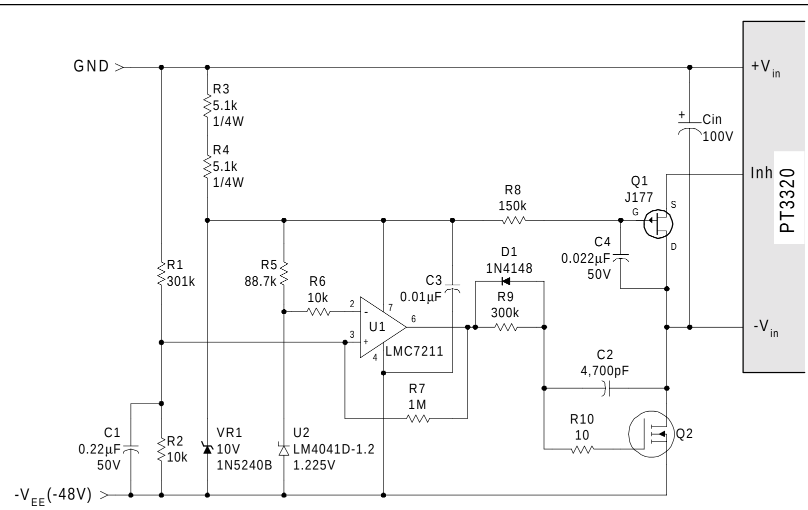


Figure 1



Design Equations

The following design equations apply to Figure 1. The in-rush current magnitude, $I_{d(Q2)}$ is controlled by the ratio C_{in}/ C_2, which in turn determines the charge period t_c. The principal design equations are given as follows.

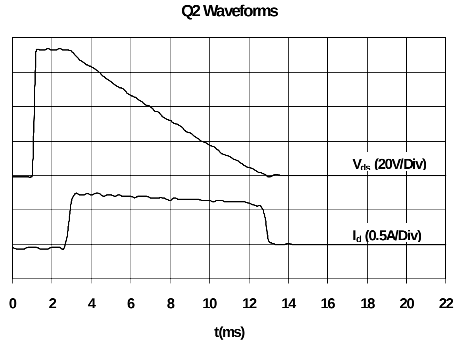
$$C_2 \approx \frac{45.10^{-6} \cdot C_{in}}{I_{d(Q2)}} \qquad \text{Eq. 2}$$

$$t_c = \frac{C_{in} \cdot V_{EE}}{I_{d(Q2)}} \qquad \text{Eq. 3}$$

Q2 Power Dissipation

The magnitude of the in-rush current determines how fast the converter input de-coupling capacitors charge to the input source voltage ($-V_{EE}$). The lower the in-rush current, the longer the charge period before the converter output can be enabled. The in-rush current also determines the power dissipation in Q_2 during the charge period, which can be high. While the charge period may be flexible, the power dissipation in Q_2 is a real limitation. It may be necessary to lengthen the in-rush period to ensure that the maximum junction temperature of Q_2 is not exceeded. For example, with a C_{in} of 100µF, limiting the in-rush current to 0.75A from a 75V maximum input source voltage requires a 10ms charge period. Figure 3 shows the drain-source voltage (V_{ds}) and drain current (I_d) waveforms for Q_2. During the charge period, Q_2 is subjected to a single, sawtooth-shaped power dissipation transient with an initial peak dissipation of 56W. This transient is estimated to momentarily raise the die temperature of a D-Pak transistor by 50°C, and that of a D^2-Pak by 30°C above the ambient case temperature.

Figure 3



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