UCC3912 INTEGRATED ELECTRONIC CIRCUIT BREAKER IC FOR HOT-SWAP AND POWER MANAGEMENT APPLICATIONS

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ABSTRACT

This application note describes the design and performance characteristics of the UCC3912 Electronic Circuit Breaker. The practical aspects of applying the circuit breaker are discussed as well as its performance compared to existing technologies. The UCC3912 integrates a power MOSFET with all of the necessary control and housekeeping functions including current limiting, short circuit protection, and auto recovery capabilities. The performance of the circuit breaker is compared to PolySwitches® and conventional fuses in both hot swap and short circuit applications.

INTRODUCTION

Today's design engineers are faced with a variety of choices when selecting protection devices to meet their circuit or system's design requirements. Fuses, positive temperature coefficient (PTC) resistors, and electromechanical circuit breakers represent only a sampling of the technologies available to meet their needs. Each of these devices provides a different degree of security, ranging from simple short circuit protection to devices which offer active current limiting and remotely resettable operation.

Fuses, while providing an inexpensive solution, fall short of many of the protection requirements imposed on modern electronic equipment. Figure 1 illustrates the protection capability of two general fuse categories; fast-acting and slow-blow. Although both devices provide gross short circuit protection, even the fastest devices react on the order of milliseconds, passing currents up to 500% of their rated value. In addition, fuses, by their very nature, have to be physically replaced following an overload condition. This increases the equipment's down time along with the chance of an incorrect device being installed, thereby reducing overall system reliability.

PTC resistors, on the other hand, eliminate the need for human intervention by providing resettable overcurrent protection. However, because they are actuated by the heating effect of an overcurrent load, their reaction time is limited to several milliseconds. This results in output currents several times their steady state rating. Figure 2 illustrates typical "time to trip" data for polymeric PTC resistors.

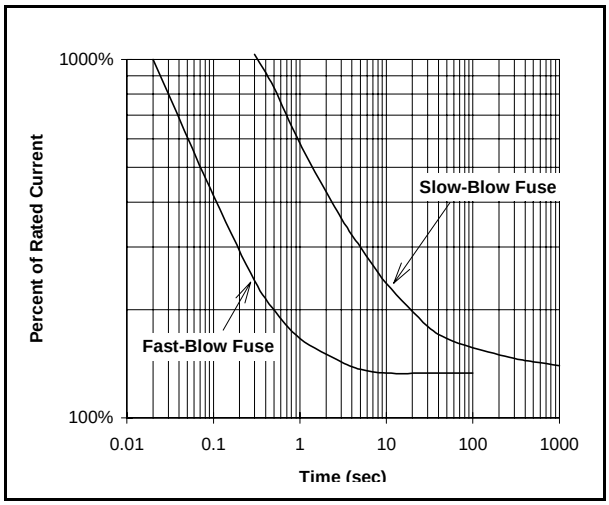

Figure 1. Relation of Percent of Rated Current to Fuse Blowing Time.

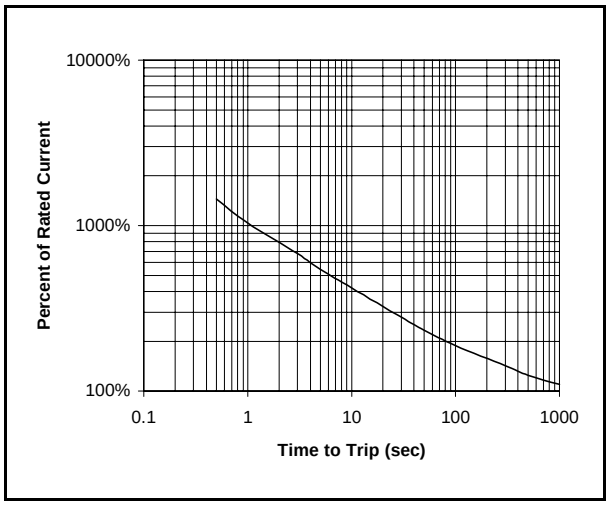

Figure 2. Relation of Percent of Rated Current to Blowing Time.

The UCC3912 Electronic Circuit Breaker offers a new, integrated solution to the problem of circuit protection and power management. Each of the drawbacks associated with existing technologies are addressed in the UCC3912 design. In addition, the UCC3912 provides logic level load control for power management applications. This note describes the features and performance of the UCC3912 as compared to other available protection techniques. In particular, hot swap, power management, and short circuit protection applications are addressed in detail.

HOT SWAPPING

The term hot swap refers to the system requirement that submodules be swapped out upon failure or system modification without removing power to the hardware. Design of modern computer systems, disk arrays, network hubs and communication switches require modules to be hot swapped while maintaining the integrity of the powered and operating system. This requirement allows the hardware to maintain operation, increasing the system's performance and reliability.

Implementing the hot swap requirement imposes several design constraints upon the equipment's power system. In order for the hardware to maintain error free operation during the installation or removal of a submodule, the 5 volt power bus must not drop below a minimum voltage of 4.5V. Voltages below 4.5V can disrupt logic levels, causing an indeterminate number of failures including data corruption and logic lockups. This ultimately reduces system reliability and data integrity.

The potential for glitching the power bus exists whenever an unpowered module is inserted into an operational system. Virtually all modules possess some amount of onboard bus capacitance which serves to filter and maintain power quality once the board becomes operational. However, these very same capacitors require an initial charging current in order to bring their voltage up to the same level as the system's power supply. The only factors limiting the magnitude of this current is the equivalent series resistance (ESR) of the capacitors themselves and the impedance of the interconnect between the module and the rest of the system. Unfortunately, the better the capacitors are at serving their purpose of filtering the bus, the lower their ESR. As a result, the initial inrush current during the hot swap can become excessively high.

Figure 3 illustrates the inrush current and corresponding voltage glitch when a load of 2A and 120µF is switched onto a 5V power bus. The 120µF of load capacitance consisted of a solid tantalum, surface mount style capacitor (Sprague #595D127X9020R2T) with a typical ESR of 0.25Ω at 100kHz. The power bus was bypassed with 240µF of the same style capacitor. As the figure illustrates, the inrush current reaches a maximum value of approximately 27A, resulting in a 1V glitch on the power bus. This exceeds the 4.5V limit by 500mV causing the supply to drop to 4.0V! In addition to causing the voltage glitch, the excessive inrush current can also result in arcing between connector pins and excessive heating of the load capacitance. Each of these effects shortens the life of the component, ultimately reducing system reliability.

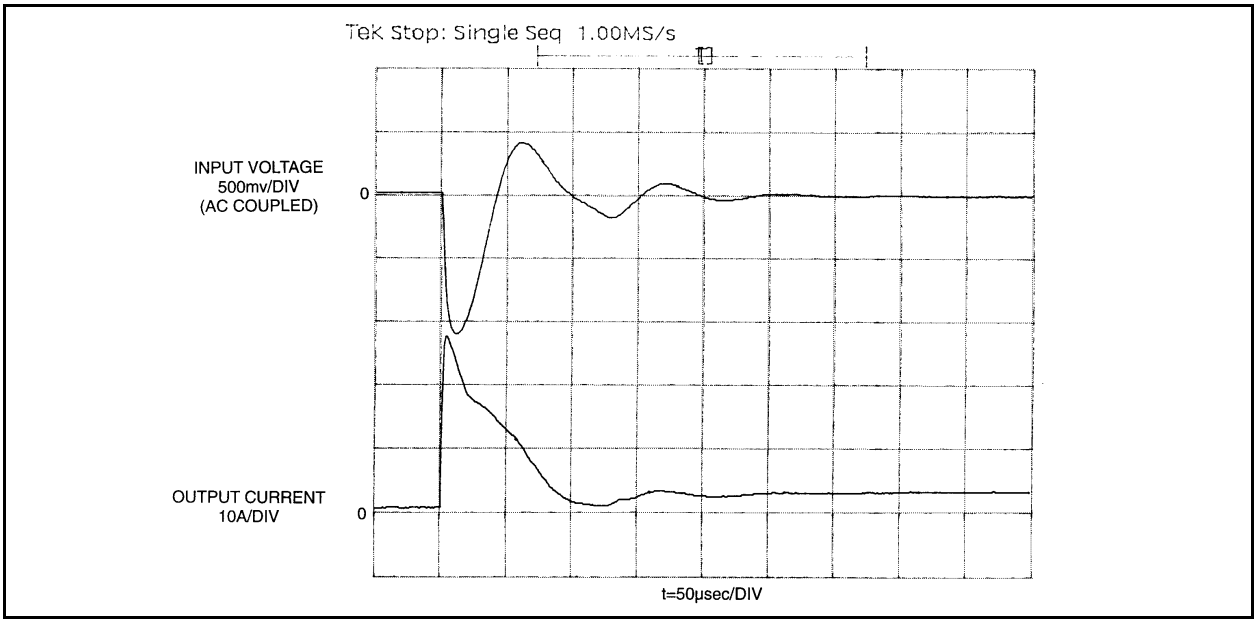

Figure 3. Inrush Current and Corresponding Voltage Glitch for a 2A, 120µF Load.

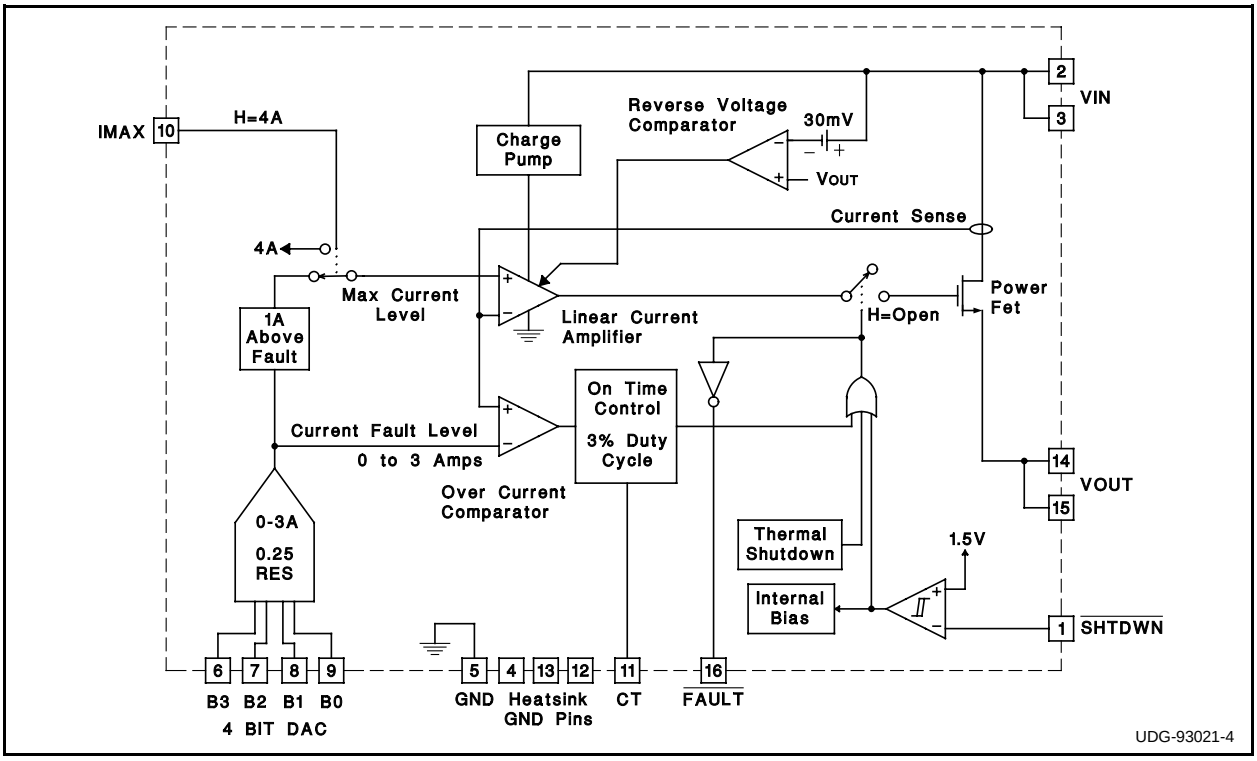

Figure 4. UCC3912 Electronic Circuit Breaker Block Diagram

THE UCC3912 ELECTRONIC CIRCUIT BREAKER

In its most rudimentary form, a circuit breaker, whether electromechanical or electronic, protects a circuit from excessive current flow. Electromechanical devices accomplish this by opening a set of contacts when the current exceeds a specified level. These types of breakers usually latch off during a fault and therefore need to be manually reset once the current falls below a reasonable value. An electronic circuit breaker, on the other hand, provides protection through the use of a power transistor. By monitoring the output current through a current shunt, the transistor can be biased "on" or "off" based upon whether or not a predetermined trip current has been exceeded.

The UCC3912 is an electronic circuit breaker IC designed to provide power management and hot swap capability in addition to its basic circuit breaker function. Performance features of the UCC3912 include:

- Integrated 0.15Ω power MOSFET
- Switchmode short circuit protection
- Automatic short circuit recovery
- Digitally programmable 4-bit maximum current limit
- Unidirectional current flow
- SMT power package
- Fault indicator output
- Low power "sleep" mode
- Thermal shutdown
- Low part count implementation

The block diagram of the UCC3912 is shown in Figure 4. Under normal operating conditions the integrated N-channel MOSFET is biased "on" using the internal charge pump to drive the gate. Output current is sensed using a mirrored MOSFET and is compared to an adjustable trip level set by the 4-bit DAC input. When the output current exceeds the trip level, the fault timer begins to charge the timing capacitor, CT, with a current of 36µA. If the output current does not fall below the trip level by the time the capacitor charges to 1.5V, the output is switched off and the capacitor is discharged with a current of 1.2µA. Once the capacitor's voltage has reached 500mV, the circuit breaker attempts to return power to the load. At this point the timer cycle will repeat as long as the fault is present, resulting in an output duty cycle of 3%.

Figure 5 illustrates the cyclical retry of the UCC3912 under fault conditions. Note that the initial fault time is longer than subsequent cycles due to the fact that the capacitor is completely discharged and must initially charge to the reset threshold of 0.5V. If at any time the output current reaches IMAX, the MOSFET transitions into linear mode, providing constant output current until the fault time expires. The discrete IMAX input is used to set the maximum output current to either a fixed

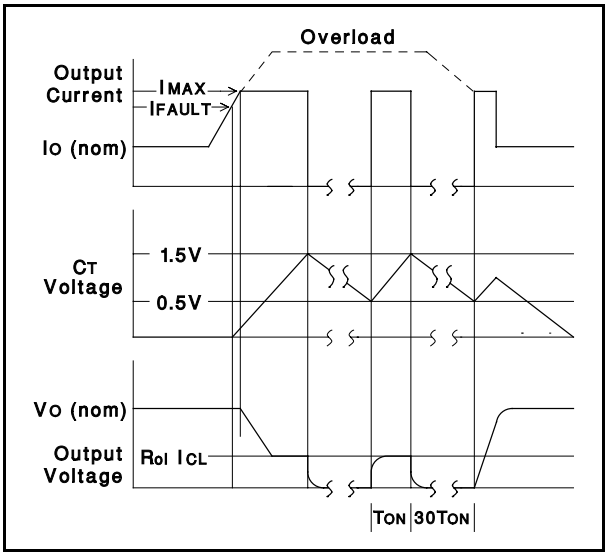

Figure 5. Load Current, Timing Capacitor Voltage and Output Voltage of the UCC3912 under Fault Conditions.

value of 4A, (logic level high), or to a value 1A above the trip current as set by the DAC inputs, (logic level low). The 4 bit DAC allows the fault current level to be programmed from 0 to 3A in 250mA increments.

Fault time duration is controlled by the value of the timing capacitor, CT, according to the following equation:

$$(1)\quad t_{FAULT} = CT \bullet \frac{\delta v}{I} = CT \bullet \frac{1.5 - 0.5}{36E - 6} = 27.8E3 \bullet CT$$

Figure 6 provides a plot of fault time vs timing capacitance. The fault time duration is set based upon the load capacitance, load current, and the maximum output current. *The "on" or fault time must be of sufficient duration to charge the load capacitance during a normal startup sequence or when recovering from a fault.* If not, the charge accumulated on the output capacitance will be depleted by the load during the "off" time. The cycle

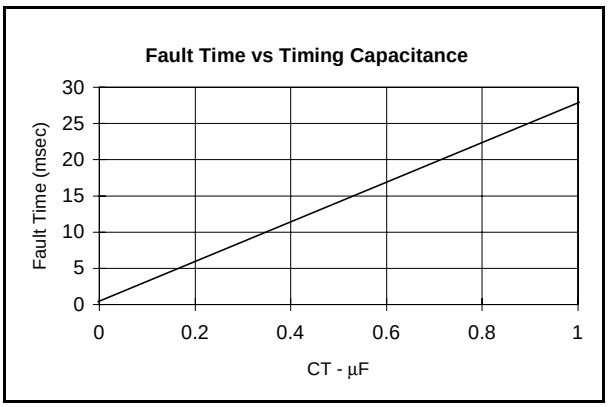

Figure 6. Fault Time vs Timing Capacitance

will then repeat, preventing the output from turning on.

To determine the minimum fault time, assume a maximum load current just less than the trip limit. This leaves the difference between the IMAX and ITRIP values as the current available to charge the output capacitance. The minimum required fault time can then be calculated as follows:

$$(2)\quad t_{FAULTmin} = \frac{C_{OUT} \bullet V_{OUT}}{I_{MAX} - I_{TRIP}}$$

The minimum timing capacitor can be calculated by substituting equation (1) for tFAULT in equation (2) and solving for CT.

$$(3)\quad CT_{min} = \frac{C_{OUT} \bullet V_{OUT}}{27.8E3 \bullet (I_{MAX} - I_{TRIP})}$$

In addition to the IMAX and DAC inputs, the UCC3912 provides a fault indicator output and shutdown command. The $\overline{\text{FAULT}}$ signal is an open drain output which is active low under any condition which turns the output MOSFET "off". These conditions include under voltage lockout (UVLO), over current faults, thermal shutdown, and active shutdown as commanded by the $\overline{\text{SHTDWN}}$ input. Note that $\overline{\text{FAULT}}$ is asserted (low) during power up while the UCC3912 is in a UVLO state.

The $\overline{\text{SHTDWN}}$ command is an active low input which turns the MOSFET "off" and puts the IC into sleep mode, reducing the quiescent current to less than 5µA. The shutdown command can be used to extend the life of battery powered systems by powering down subsystems when not in use.

Unidirectional current flow is another attractive feature of UCC3912. The reverse voltage comparator senses the output voltage and turns the MOSFET "off" whenever the intput voltage is less than 30mV below the output. Under light loads, the UCC3912 regulates the voltage drop until

$$(4)\quad (I_{OUT}) \bullet (R_{DSon}) \geq 30mV,$$

thus preventing false shutdowns. This effectively prevents current flow from output to input, eliminating the need for series diode protection and the associated voltage drop and power losses incurred with its use.

PRACTICAL CONSIDERATIONS

The UCC3912 is supplied in 16-pin power surface mount packages. Four ground leads are provided in order to effectively transfer heat out of the package. These pins should always be terminated to as large an area of copper as possible. Although the 3% duty cycle switchmode protection drastically minimizes power dissipation, thermal analysis

should still be performed in order to insure reliable circuit operation.

When interfacing with larger values of load capacitance, the UCC3912 fault time must be increased accordingly. While the average power remains low due to the 3% duty cycle, the power dissipation during the fault time will result in a junction temperature rise based on the thermal time constant of the system. A simplified thermal model of the system is comprised of the die, leadframe and PC board. However, for fault times less than 30msec, the effect of the leadframe and PC board can be considered negligible as their thermal time constants are on the order of 2 and 300sec respectively. A rough estimate of the transient junction temperature can then be calculated based on the following equation:

$$(5) \quad Tj(t) = P_{DISS}\left[\Theta_{DIE}\left(1 - e^{-t/\tau}\right)\right] + T_L$$

Where P_{DISS} = transient power dissipation
Θ_{DIE} = thermal resistivity between die and leadframe ≈ 4°/W
t = fault time
τ = thermal time constant of the die ≈ 30msec
T_L = steady state lead temperature

As the fault time is increased beyond 30msec, a more thorough transient thermal analysis is required. For additional information regarding thermal analysis and transient response, the reader is directed to reference (1).

In applications requiring minimum voltage losses, it is important to take the effects of PCB trace resistance into account. When passing two to three amps of current, minimum trace widths can result in enough I • R voltage drop to effect system performance. By increasing either the trace width or copper weight, these effects can be made negligible. Table I provides resistance/inch values for various trace widths of 1, 1.5, and 2 oz. copper.

Table I
PCB Trace Resistance (mΩ/inch)

Copper Wt.	Trace Width (inches)					
	0.01	0.02	0.03	0.05	0.07	0.1
1.0 oz.	48.5	24.23	16.2	9.7	6.9	4.9
1.5 oz.	38.8	19.4	12.9	7.8	5.5	3.9
2.0 oz.	24	12	8	4.8	3.4	2.4

A TYPICAL APPLICATION

In order to evaluate the performance of the UCC3912, consider a typical application consisting of a 2A maximum load current in parallel with 120µF of load capacitance. The 2A output current is accommodated by setting the UCC3912 trip current to 2.25A, using the DAC inputs. Bits B0 and B1 are grounded while bits B2 and B3 are tied to VIN. The maximum output current is configured to 1A above the trip current (3.25A) by grounding the IMAX input. The timing capacitor value must then be selected to accommodate the 120µF load capacitance:

$$(6) \quad CT_{min} = \frac{C_{OUT} \bullet V_{OUT}}{27.8E3 \bullet (I_{MAX} - I_{TRIP})}$$

$$= \frac{120E-6 \bullet 5}{27.8E3 \bullet (3.25 - 2.25)} = 21.6nF$$

A 47nF capacitor was chosen in order to provide adequate margin for component and parameter tolerances. Lastly, the $\overline{SHTDWN}$ input to the UCC3912 is connected to VIN since it is not used in this example.

In actual hot swap applications, the circuit breaker function may reside on the system's backplane servicing one or more submodules, or be distributed throughout the individual submodules depending on system requirements. In order to test both of these application scenarios, a MOSFET was used to simulate a hot swap on the input and output of the UCC3912. A test load was constructed using a 120µF low ESR tantalum capacitor in parallel with a carbon power resistor, while 240µF was used to simulate the system's input bus capacitance. Output current was monitored using a noninductive 10mΩ current shunt in series with the load. Figure 7 illustrates the test setup including the UCC3912 circuit configuration.

HOT SWAP PERFORMANCE

Figure 8 illustrates the load current and input voltage waveforms, measured at points A and B in Figure 7, with and without the UCC3912. In Figure 8(a), transistor Q2 was used to perform the hot swap on the output of the UCC3912, simulating an application with the circuit breaker resident on the system backplane. In this situation the UCC3912 limits the load current to approximately 4A as compared to the 24A peak seen without the breaker! Consequently, the voltage glitch seen at the input bus capacitor is reduced from approximately 1V to less than 150mV!

Figure 8(b) illustrates the results when Q2 is used to simulate the hot swap on the input of the UCC3912. Again, the output current is controlled as both the circuit breaker and submodule receive power, providing very similar results to those of Figure 8(a).

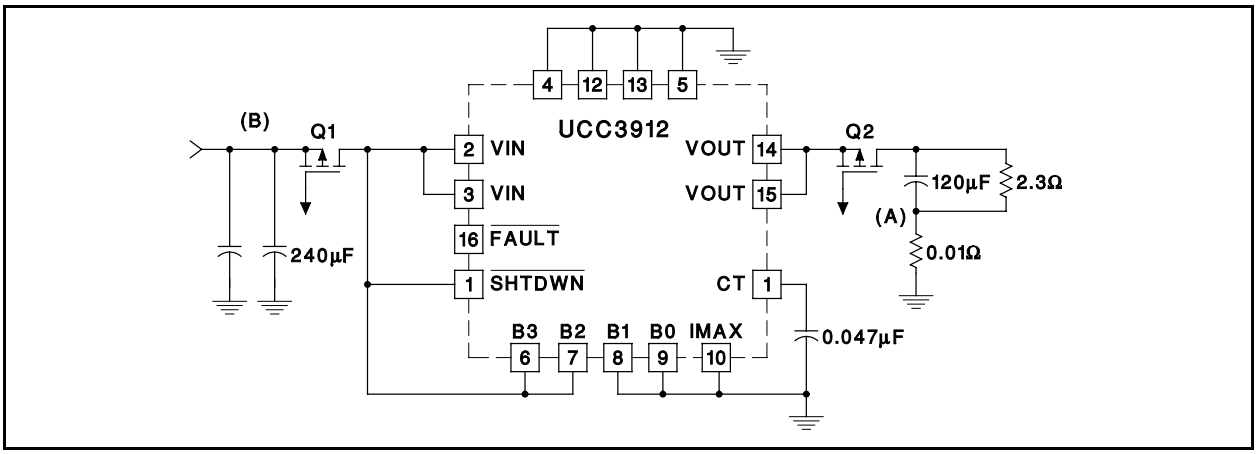

Figure 7. Typical UCC3912 Configuration and Hot Swap Test Circuit Setup.

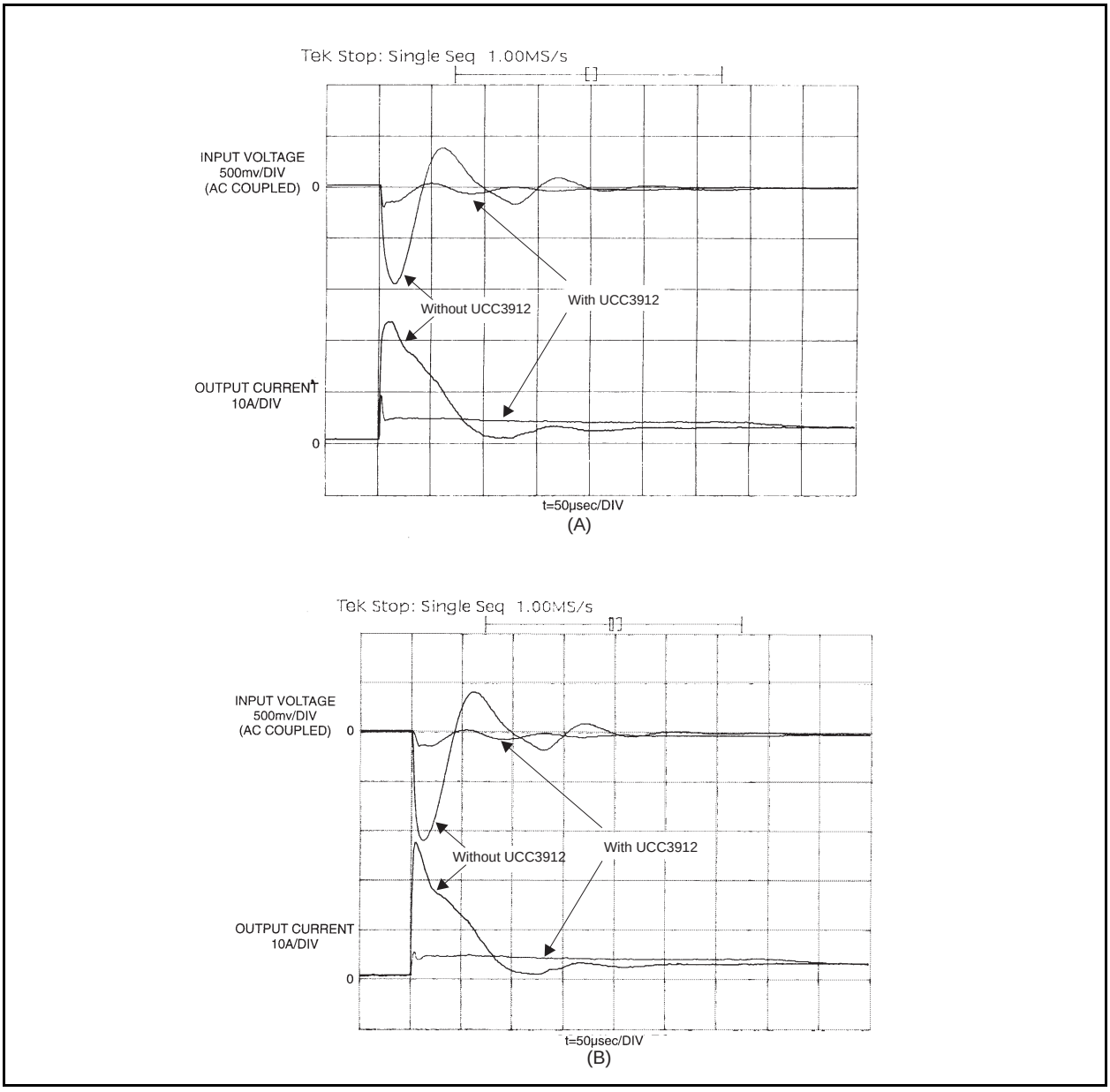

Figure 8. Hot Swap Results With and Without the UCC3912 Circuit Breaker. A) Hot Swap Performed on UCC3912 Output. B) Hot Swap Performed on UCC3912 Input.

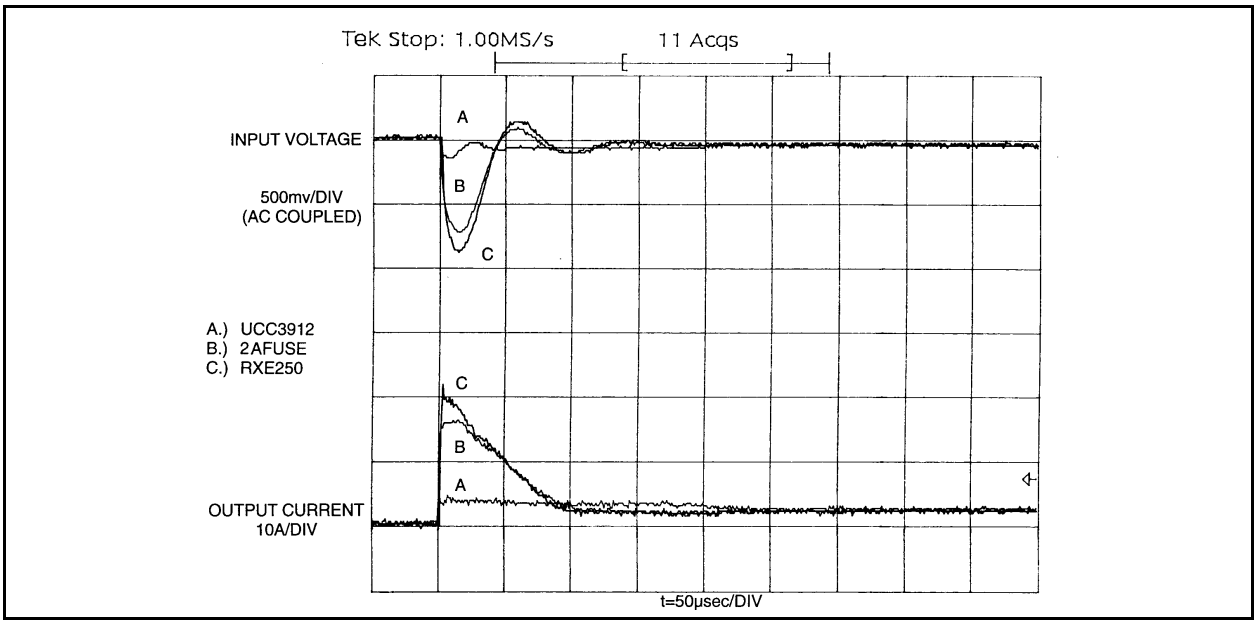

Figure 9. Hot Swap Performance Comparison Between a Fuse, PolySwitch® and the UCC3912.

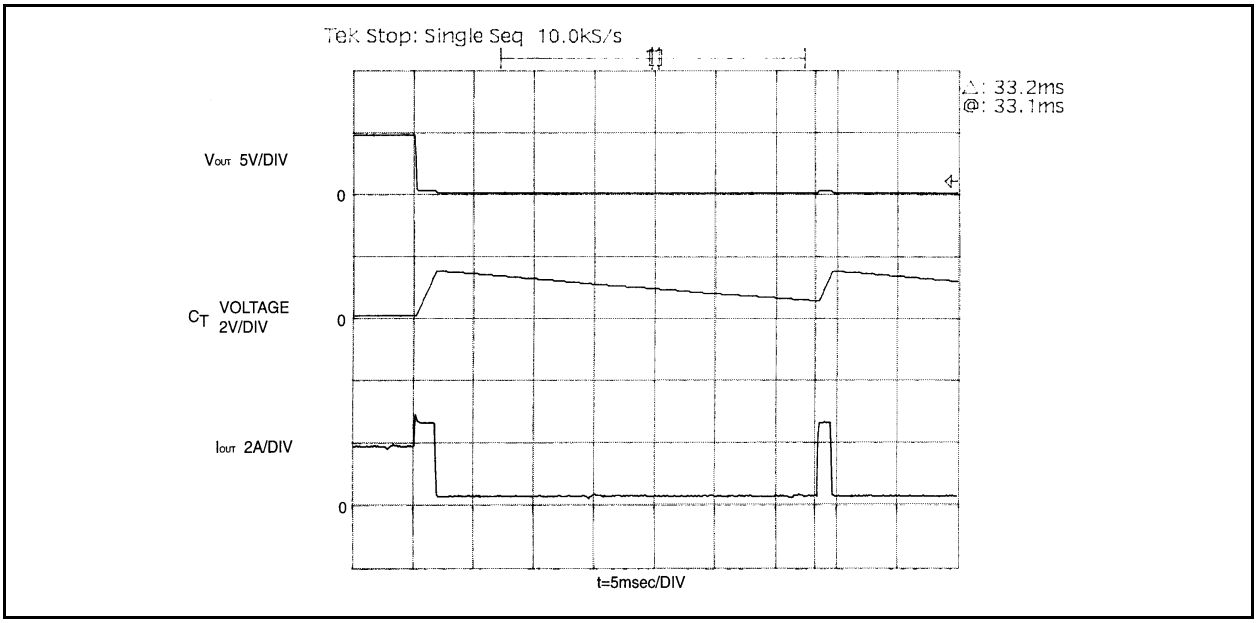

Figure 10. Short Circuit Performance of the UCC3912 Illustrating the 3% Duty Cycle Protection Technique.

Not shown in this figure is a delay of approximately 100µsec as the internal charge pump builds up gate charge for the MOSFET.

The hot swap performance of the UCC3912 was also compared to that of a fuse and PolySwitch®, two industry standard protection devices. A 2.5A PolySwitch® (RXE250) and a 2A slow-blow fuse (Littelfuse 313.002) were each substituted for the UCC3912 during a hot swap test. Figure 9 illustrates the results using the three different protection devices. Comparing the results of Figures 8 and 9, it is evident that both the fuse and PolySwitch® offer virtually no protection for transients of this speed; the current magnitudes are very close to those seen without any protection device at all. The circuit breaker, on the other hand, provides a fast transient response, keeping the current and the associated voltage transient within specification.

SHORT CIRCUIT PROTECTION

As previously described, the UCC3912 provides overcurrent and short circuit protection by modulating the output at a 3% duty cycle. During the "on" time, output current is limited to the value set by the IMAX and DAC inputs. Figure 10 illustrates the performance of the UCC3912 test circuit when a

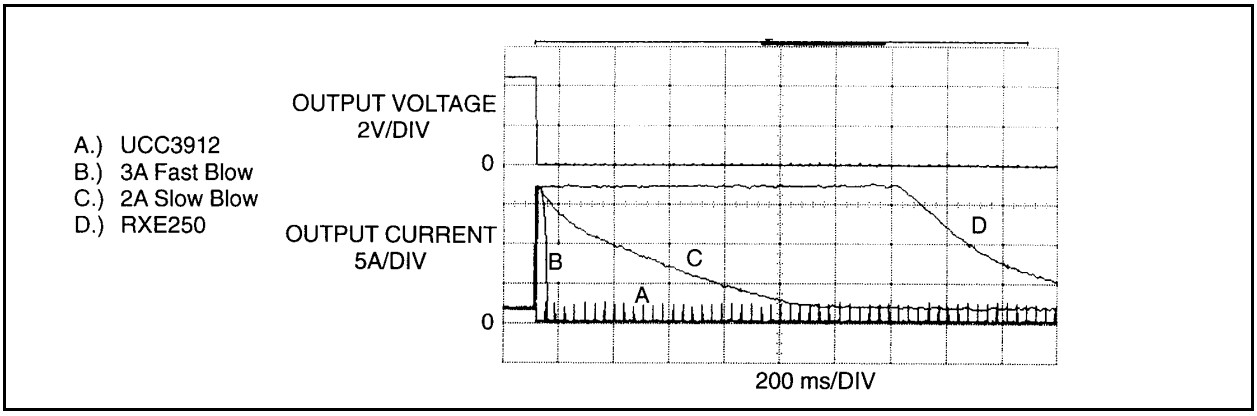

Figure 11. Short Circuit Performance Comparison of a Fuse, PolySwitch® and the UCC3912.

short-circuit is applied in place of the load. The bottom trace is the output current, modulated at a 3% duty cycle, while the center trace is the voltage across the timing capacitor. Note that the first current pulse is approximately 50% longer than subsequent pulses due to the timing capacitor initially charging from 0V.

The short circuit test was also conducted on the 2.5A PolySwitch®, 2A slow-blow fuse, and a 3A fast-acting fuse (Littelfuse 312.003). Figure 11 compares the performance of the 4 different protection techniques. The peak currents incurred with each of the fuses and the PolySwitch® reach approximately 17.5A and are limited only by the output capability of the 5V power supply. The PolySwitch® takes approximately 1.25sec before it begins to limit the current and eventually latches into high impedance mode. At this point it will remain in a high impedance state due to a sustained self heating current and will only reset after it has cooled and the fault condition has been corrected. As a result, the device requires that the input voltage be removed from the system in order to insure a circuit reset. The fuses on the other hand, respond faster than the PolySwitch®, but once blown require manual replacement before the hardware can resume operation. Table II compares the I • T and peak current characteristics of the four techniques.

Table II

Protection Device	Peak Current (Amps)	I • T (Amp-sec)
PolySwitch® RXE250	17.5	17.5
Fuse 312.003	17.5	9.75
Fuse 313.002	17.5	0.875
UCC3912	3.25	0.098

Note: 1) Peak currents are limited by power supply.
2) I • T estimated for first second of short circuit.

When compared to any of the other commonly used technologies, the performance of the UCC3912 is superior. The electronic circuit breaker responds almost immediately to a short circuit, limiting the current to 3.25A before turning off the output. The breaker then attempts to reapply power at a 3% duty cycle until the fault has been corrected. The low duty cycle, coupled with the current limiting feature keeps the power dissipation at a reasonable level, eliminating the need for extensive heating sinking. In this example the UCC3912 dissipates only 5V • 3.25A • 3% = 488mW of power during the short circuit.

POWER MANAGEMENT APPLICATIONS

In an effort to save energy, the federal government is working to impose regulations that will require electronic equipment and appliances to operate more efficiently. As an example, consider the personal computer (PC). PCs typically dissipate 100 to 200W, with an additional 150 to 350W consumed by the monitor. In order to limit the power dissipation to a recommended 30W during periods of nonusage, circuitry must be added to shutdown key components such as the monitor, high powered cache circuits and bus interfaces. The UCC3912 offers a simple solution to these types of power management applications.

The UCC3912 can be configured as a low current (<5µA) standby power switch, as shown in Figure 12. The shutdown input, SHTDWN, is utilized to turn off the internal MOSFET, removing power from the load and reducing the UCC3912 quiescent current to <5µA. When reactivated by the logic command, the current limiting features of the UCC3912 allow the load circuits to resume operation without disrupting the rest of the system.

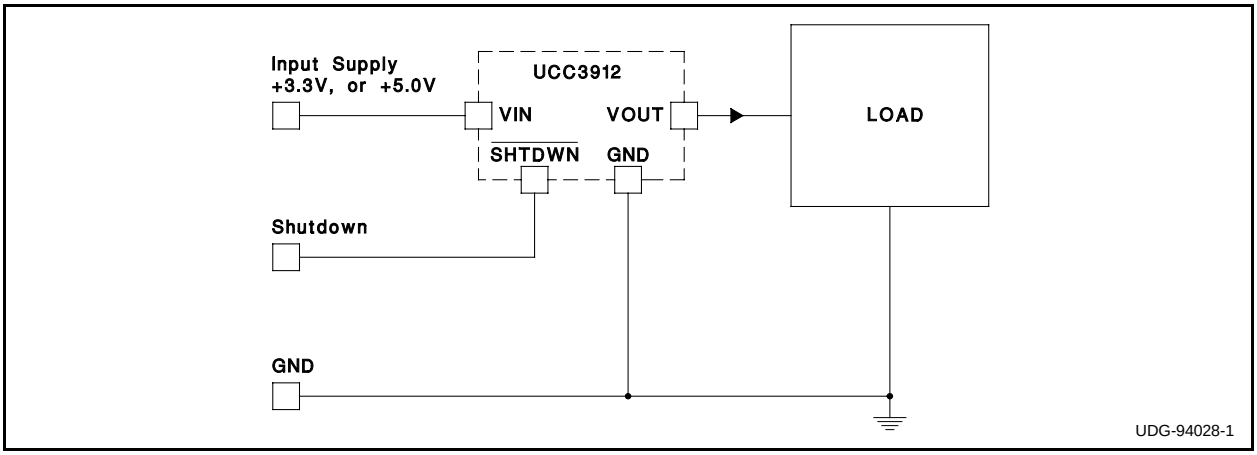

Figure 12. Low Current Standby Power Switch

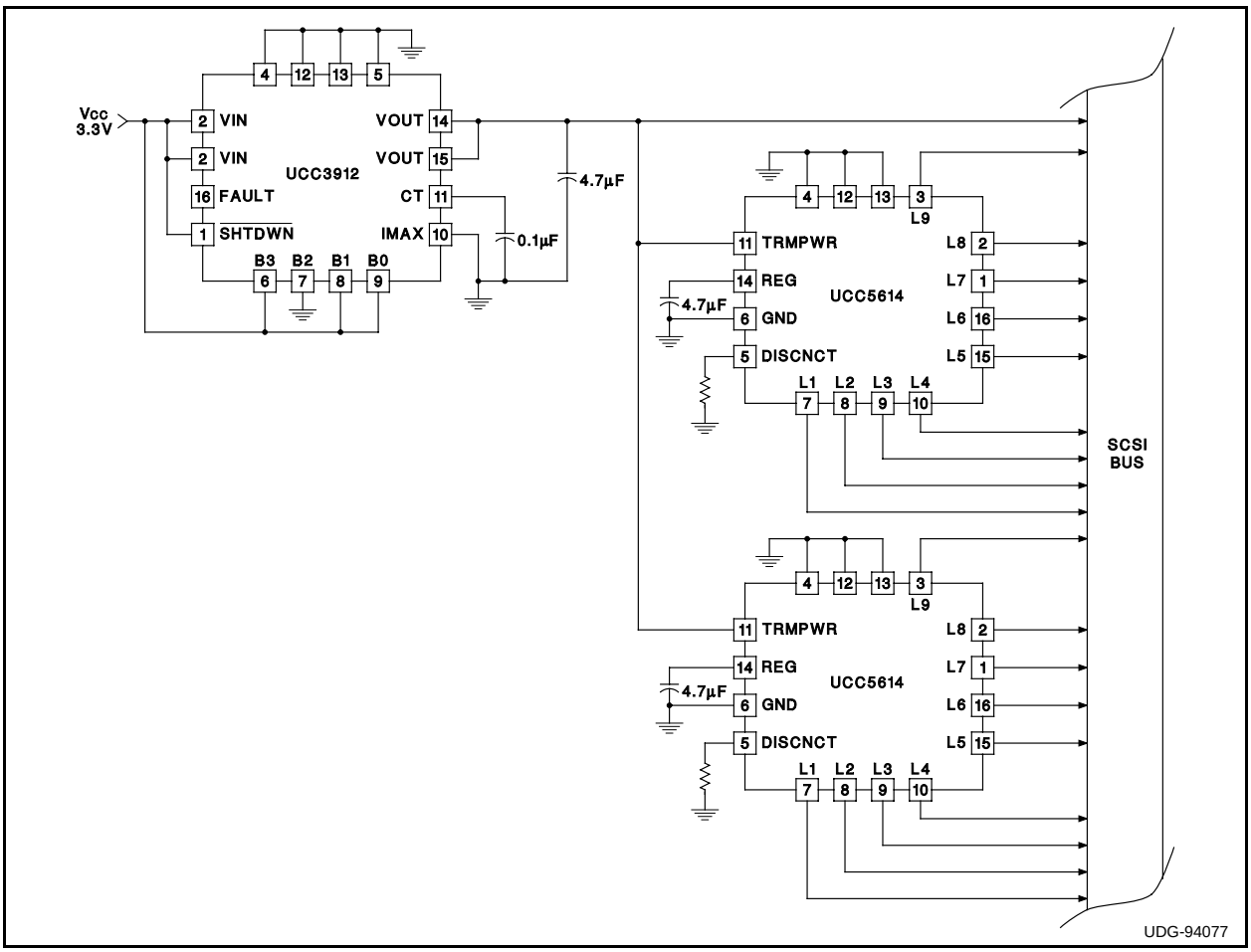

Figure 13. Typical 3.3V SCSI Application

APPLICATION CIRCUITS

The 3.3V power bus has quickly become the standard for laptop computers and other battery operated equipment. Unfortunately, SCSI standards specify an active termination voltage of 2.7V. In addition, standards require that the Termpwr source be fused and provide for unidirectional current flow. These requirements have typically forced designers to include a 5V supply in 3.3V systems - a 5%, 3.3V bus leaves only 130mV of headroom for a diode, fuse, and regulator overhead. Replacing the diode and fuse with the UCC3912 limits the voltage drop to less than 60mV while still meeting SCSI requirements. Combining the UCC3912 with a low dropout active terminator such as the UCC5614 results in a complete design. Figure 13 illustrates a typical 3.3V SCSI application.

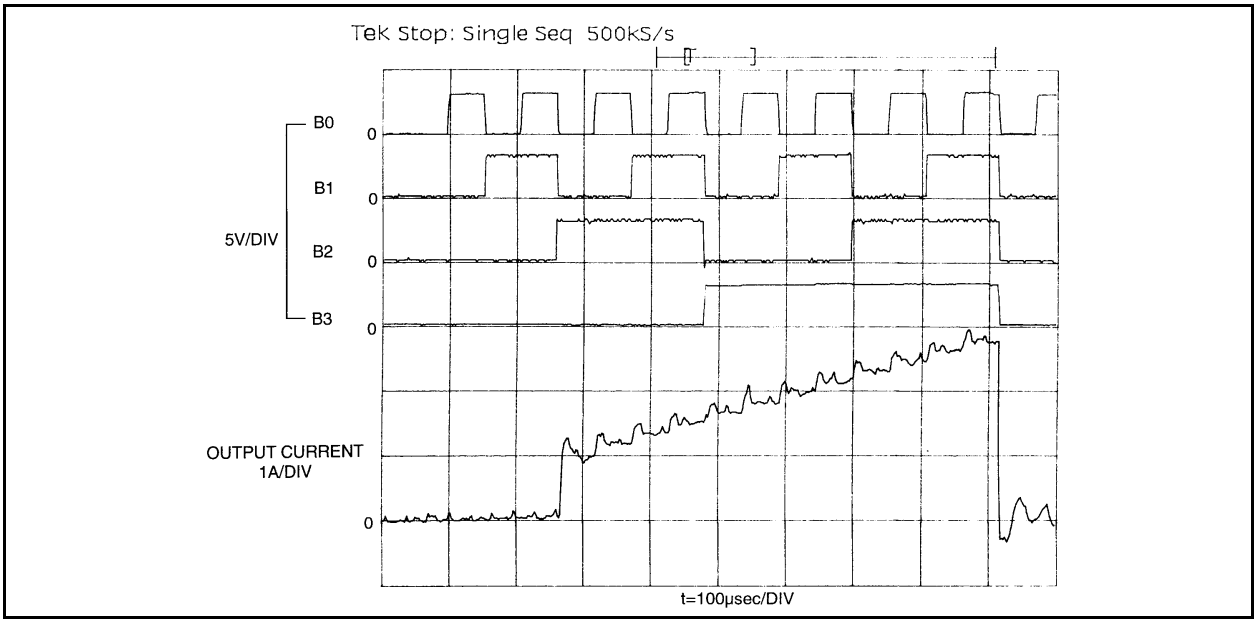

Figure 14. Controlled Current Slew Rate Using the UCC3912 4-Bit DAC.

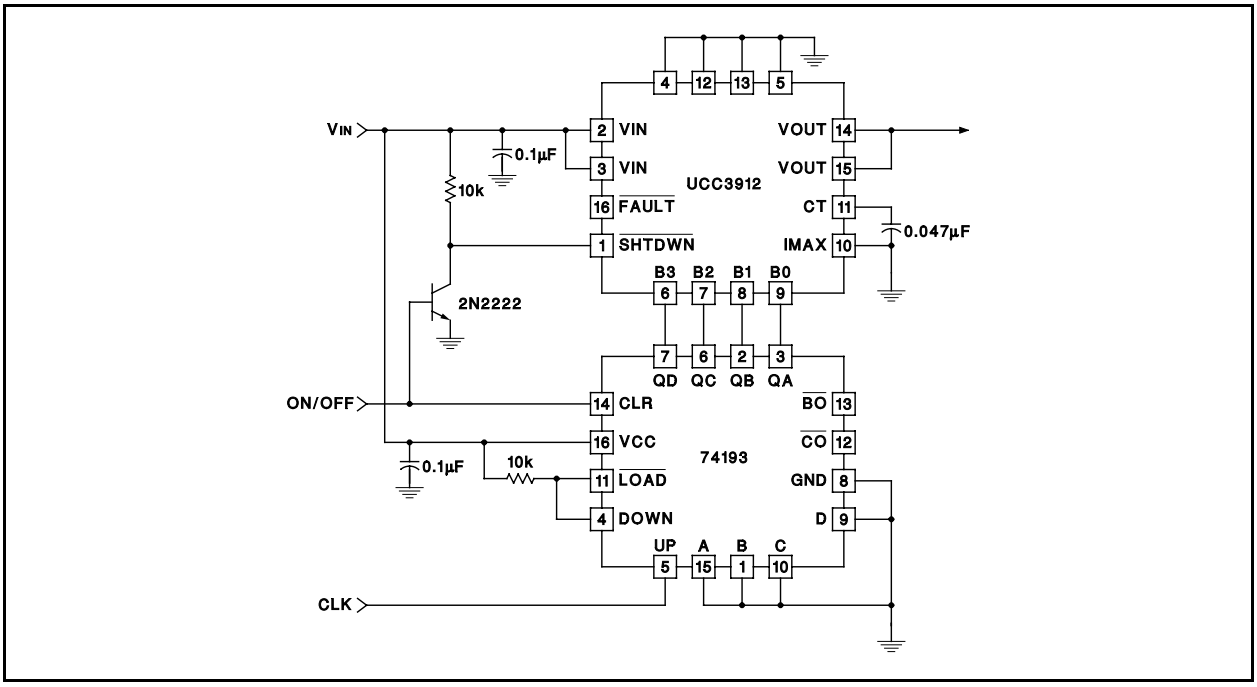

Figure 15. UCC3912 Current Control Circuit Implementation.

The UCC3912 lends itself well to more sophisticated current limiting schemes through the use of the DAC inputs. Greater control of output current slew rate can be obtained by stepping the DAC through a series of its input codes. Figure 14 illustrates the output current as the DAC inputs are controlled using the output of a 4-bit counter as shown in Figure 15. Similarly, loads such as motors often require inrush currents several times their normal running value. By using the counter in Figure 15 to count down rather than up, the motor can be quickly accelerated to speed using maximum current and then closely protected against overload.

The duty cycle protection capability of the UCC3912 can be disabled by grounding the timing capacitor input, CT. This causes the UCC3912 to remain in constant current mode during a fault condition. When operating in this manner the UCC3912 is in linear mode and will dissipate power as function of the maximum output current and differential input/output voltage. It is extremely important that adequate heatsinking is provided when operating in this configuration.

SUMMARY

As demonstrated throughout this application note, the UCC3912 provides a level of protection far superior to that offered by existing technologies. Integrating a high speed, programmable current amplifier, power MOSFET, and charge pump allows for precise control of both inrush and short circuit currents. Fast, accurate transient control helps to maintain power supply tolerance, enabling reliable hot swap implementation. In addition, preventing destructive current transients during connector mating prolongs the life of the hardware. By integrating each of these features, the UCC3912 electronic circuit breaker offers a new and complete solution to power management, hot swap, and short circuit requirements.

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