Programmable SCSI Terminator Improves Performance of Ultra160 and Ultra320 Systems

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ABSTRACT

The multi-drop SCSI bus has an inherent problem, as drives are added to the SCSI bus the impedance of the bus drops. Some Ultra160 and Ultra320 systems may not operate at rated speed because of errors or the SCSI domain validation (SDV) adjusting the speed down to a level that will operate.

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1 Introduction

The multi-drop SCSI bus has an inherent problem, as drives are added to the SCSI bus the impedance of the bus drops. Some Ultra160 and Ultra320 systems may not operate at rated speed because of errors or the SCSI domain validation (SDV) adjusting the speed down to a level that will operate. If the characteristic impedance of the bus does not match the standard terminator impedance as specified by SPI-3 and SPI-4, a programmable terminator, UCC5696, now mandatory in SPI-5 systems may be used to improve performance of low voltage differential (LVD) SCSI bus configurations. The new generations of the SCSI parallel interface (SPI) specification apply to all previous generations as well.

2 Why Terminate Signals

When signals propagating down a wire encounter a change in impedance, a reflection of the signal occurs. In the worst case, an open line, the reflected signal is inverted and propagates back down the bus. On slower signals, the reflection is added to the original signal distorting it. For faster signals, the reflection can disrupt subsequent signals on the line. Terminators are used to match the characteristic impedance of the bus in order to minimize the signal reflections.

3 What Factors Determine Bus Impedance

The cable or backplane impedance can be shown to be $\sqrt{L/C}$. For cable, the characteristic impedance of the bus is relatively high because of the high inductance of the cable offsetting the capacitance of the disk drives. Backplanes have lower impedance than cables because they have low inductance etch and higher capacitance because of feed-throughs, press in connectors, power planes, and the disk drives. Except for careful backplane design, the only adjustment to the SCSI bus impedance in the past has been the length of the bus and the number of devices. Some bus length versus device count tradeoffs have been inconsistent with the desired configurations and operating speed.

4 Lessons from SPI-5

SPI-3 and SPI-4 design, especially backplanes and cables, have been challenging because engineers did not have the tools that are available now. The SCSI signal modeling specification (SSM-2), and the passive interconnect performance specification (PIP) were introduced with SPI-5. These standards take the trial and error out of the design process or set standards by which we can measure results.

Similarly, the programmable terminator specified in SPI-5, can be used to correct problems or remove limits on the number of devices in specific SPI-3 and SPI-4 systems. It is not always possible to implement the design rules necessary to keep the SCSI bus impedance high enough for Ultra160 and Ultra320 speeds. SCSI domain validation (SDV) tests the conditions and settings of the bus components and determines the operating speed to maintain error free performance. It is possible that an Ultra320 system is operating at Ultra160 or less.

The programmable terminator, UCC5696 TI literature number SLVS406, allows the designer to match the impedance of the terminator to that of the SCSI bus and improve signal quality. When the signal quality is acceptable to SDV and the cyclic redundancy check (CRC) is clear, Ultra320 design speed is achieved.

5 Lab Test

Here is an example of an Ultra320 host bus adapter and disk drives on a 2.5-meter twist and flat multi-drop cable. The Host's on-board termination was disabled to add a UCC5696 evaluation module to each end of the bus. Each of the added unit loads is approximately 8-pF per signal pair and there is an additional 5-pF per pair from the disabled host termination. A schematic of the test setup is shown in Figure 1.

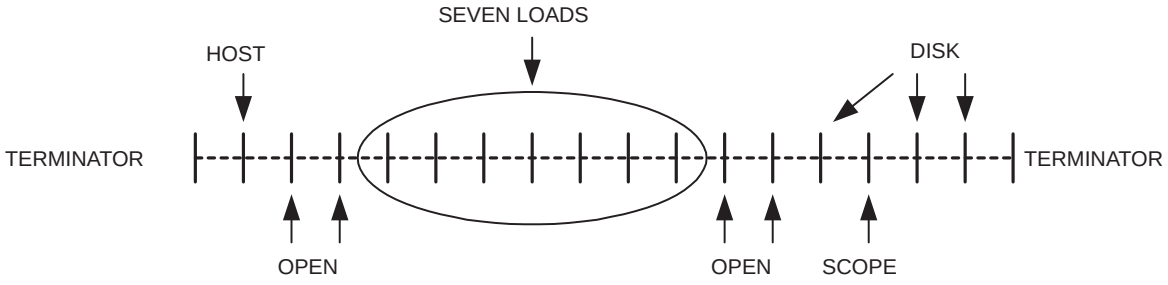

Figure 1. Lab Test Schematic

At power-up, the default impedance of the UCC5696 is 105 Ω. The limit of this system still operating at Ultra320 is seven added loads with the loads centered on the bus. Shifting the loads toward either terminator, not adding more loads, caused the system to operate at Ultra160 speed.

Next, the bus was fully loaded by adding the unit load to all the open connectors, 11 places. The system operates at Ultra160 speed with the terminators still set at the default 105 Ω. The scope observes signals at the third slot from the drive end termination. Figure 2 shows a data bit with the terminators set to 105 Ω, the incident wave is smaller than the steady state wave. The incident wave is the first 5 ns after the transition. The slower rise time of the signals limit the operating speed.

Terminator Impedance 105 Ω

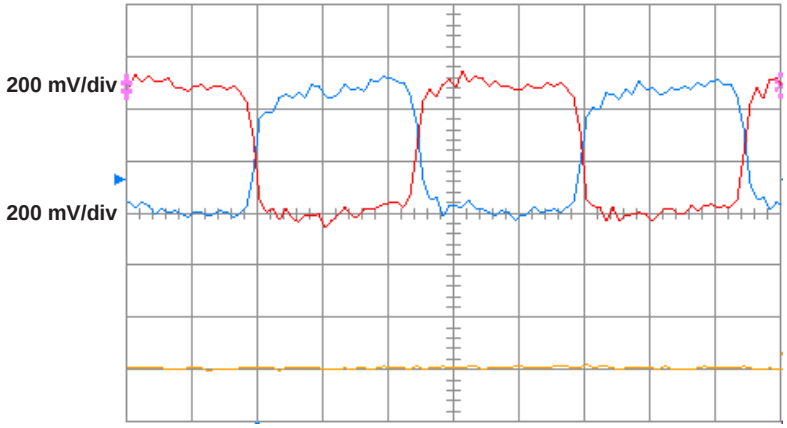

Figure 2

Both terminators were set at 65 Ω and the system did not operate. At 75 Ω, the system operated at Ultra320 speed. Figure 3 shows a data bit with the terminators set at 75 Ω. The incident wave has overshoot and is higher than the steady-state wave. The steady-state wave is loaded by the terminators and has only a 275-mV range.

Terminator Impedance 75 Ω

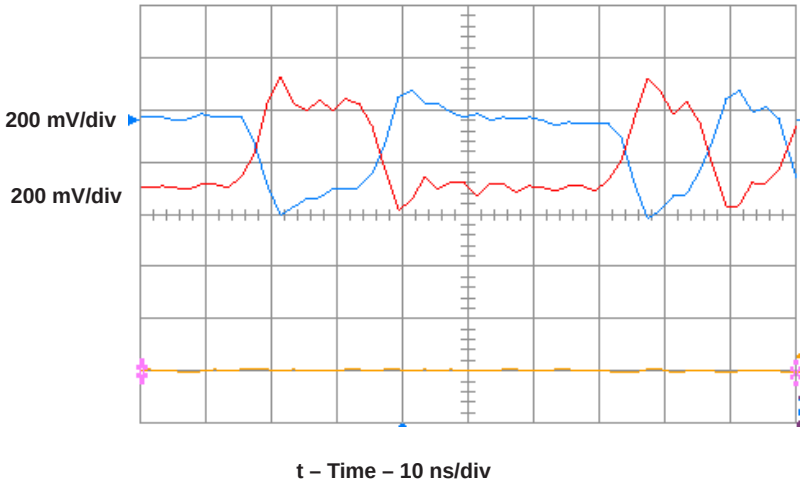

Figure 3

With the terminators set to 90 Ω, an average of the operating limits 75 Ω and 105 Ω, the system operates at Ultra320 speed. The terminators set to 90 Ω have some overshoot and are higher than the steady-state signal which has about a 350-mV range. See Figure 4.

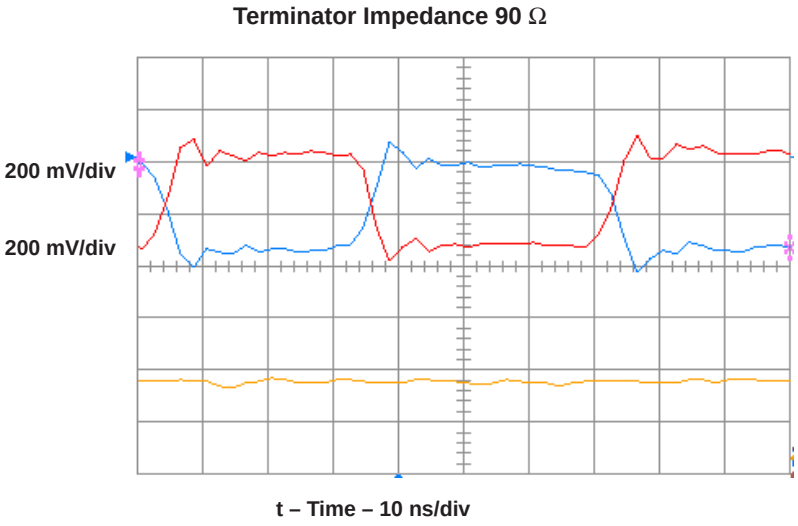

Figure 4

6 Conclusion

The UCC5696 offers a clear advantage in helping to remove the design limits from a SCSI system and achieve the intended operating speeds of the bus. The UCC5696 Data Sheet and the UCC5696 User's Guide, TI Literature No. SLUU136, discusses the I^2C programmability of the terminator. Both of these references are available on the TI website at www.ti.com.

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