

Single Cell Impedance Track Printed-Circuit Board Layout Guide

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Battery Management

ABSTRACT

Attention to layout is critical to the success of any battery-management circuit board. The mixture of high-current paths with an ultralow-current microcontroller creates the potential for design issues that can be challenging to solve. This application report presents guidelines to ensure a stable and well-performing project.

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1 Introduction

Attention to layout is critical to the success of any battery management circuit board. The mixture of high-current paths with an ultralow-current microcontroller creates the potential for design issues that are not always trivial to solve. Careful placement and routing with regard to the principles described in the following text can ensure success.

2 Power Supply Decoupling Capacitor

Power supply decoupling from V_{CC} to ground is important for optimal operation of the Impedance TrackTM gas gauge. To keep the loop area small, place this capacitor next to the IC and use the shortest possible traces. A large loop area renders the capacitor useless and forms a small-loop antenna for noise pickup.

Ideally, the traces on each side of the capacitor should be the same length and run in the same direction to avoid differential noise during ESD. If possible, place a via near the VSS pin to a ground plane layer.

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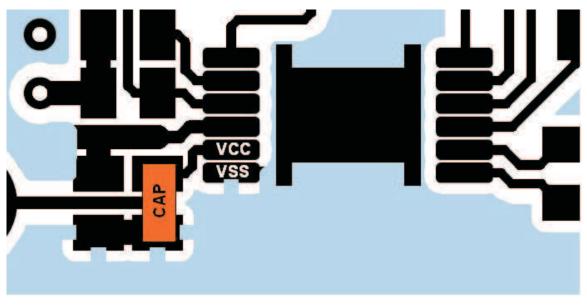


Figure 1. Recommended Placement of VCC Decoupling Capacitor

3 Capacitors

Power supply decoupling for the gas gauges requires a pair of $0.1-\mu F$ ceramic capacitors for (BAT) and (VCC) pins. These should be placed reasonably close to the IC, without using long traces back to VSS.

The LDO voltage regulator, whether it be external or internal to the main IC, requires a 0.47- μ F ceramic capacitor to be placed fairly close to the regulation output pin. This capacitor is for amplifier loop stabilization and as an energy well for the 2.5-V supply.

4 Communication Line Protection Components

The 5.6-V Zener diodes, used to protect the communication pins of the gas gauge from ESD, should be located as close as possible to the pack connector. The grounded end of these Zener diodes should be returned to the Pack(–) node, rather than to the low-current digital ground system. This way, ESD is diverted away from the sensitive electronics as much as possible.

In a pack-side application it is sometimes necessary to cause transitions on the communication lines to trigger events that manage the gas gauge power modes. An example of one of these transitions is detecting a sustained low logic level on the communication lines to detect that a pack has been removed. Given that most of the gas gauges do not have internal pulldown networks, it is necessary to add a weak pulldown resistor to accomplish this when there's an absence of a strong pullup resistor on the system side. If the weak pulldown resistor is used, it may take less board space to use a small capacitor in parallel instead of the zener diode to absorb any ESD transients that are received through communication lines.



5 Protector FET Bypass and Pack Terminal Bypass Capacitors

The general principle is to use wide copper traces to lower the inductance of the bypass capacitor circuit. In Figure 2, an example layout demonstrates this technique.

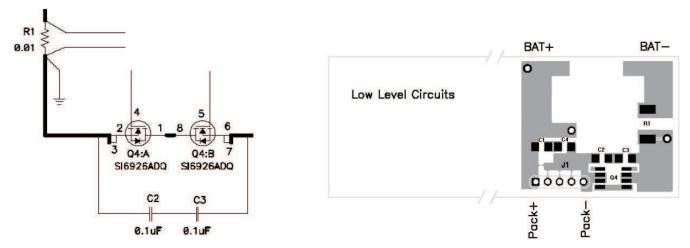


Figure 2. Use Wide Copper Traces to Lower the Inductance of Bypass Capacitors C1, C2, C3 and C4

6 Ground System

The single-cell gas gauges require a low-current ground system separate from the high-current PACK(–) path. ESD ground is defined along the high-current path from the Pack(–) terminal to the protector FETs. It is important that the low-current ground systems only connect to the PACK(–) path at the sense resistor Kelvin pick-off point. The use of an optional inner layer ground plane is recommended for the low-current ground system. In Figure 3, the green is an example of using the low-current ground as a shield for the gas gauge circuit. Notice how it is kept seperate from the high-current ground which is shown in red. The high-current path is joined with the low-current path only at one point shown with the small blue connection between the two planes.



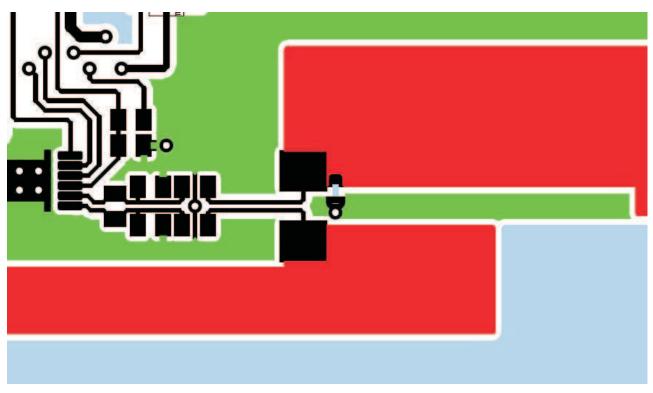


Figure 3. Differential Filter Components With Symmetrical Layout

7 Kelvin Connections

Kelvin voltage sensing is extremely important in order to accurately measure current and cell voltage. Notice how the differential connections at the sense resistor do not add any voltage drop across the copper etch that carries the high current path through the sense resistor. See Figure 3 and Figure 4.

8 Board Offset Considerations

Although the most important component for board offset reduction is the decoupling capacitor for Vcc, additional benefit is possible by using this recommended pattern for the coulomb counter differential low-pass filter network. Maintain the symmetrical placement pattern shown for optimum current offset performance. Use symmetrical shielded differential traces, if possible, from the sense resistor to the $100-\Omega$ resistors as shown in Figure 4.



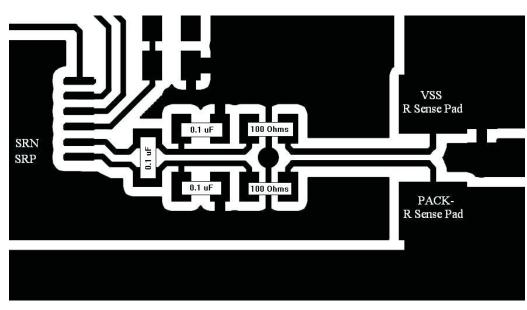


Figure 4. Differential Connection between SRP and SRN Pins with Sense Resistor

9 ESD Spark Gap

Protect I²C clock, data, and other communication lines from ESD with a spark gap at the connector. The pattern below is recommended, with 0.2-mm spacing between the points.

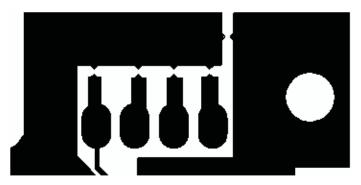
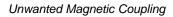


Figure 5. Recommended Spark-Gap Pattern Helps Protect Communication Lines From ESD

10 Unwanted Magnetic Coupling

A battery fuel gauge circuit board is a challenging environment due to the fundamental incompatibility of high-current traces and ultralow-current semiconductor devices. The best way to protect against unwanted trace-to-trace coupling is with a component placement such as that shown in Figure 6, where the high-current section is on the opposite side of the board from the electronic devices. Clearly this is not possible in many situations due to mechanical constraints. Still, every attempt should be made to route high-current traces away from signal traces, which enter the gas gauge directly.

IC references and registers can be disturbed and in rare cases damaged due to magnetic and capacitive coupling from the high-current path. During surge-current and ESD events, the high-current traces appear inductive and can couple unwanted noise into sensitive nodes of the gas gauge electronics.





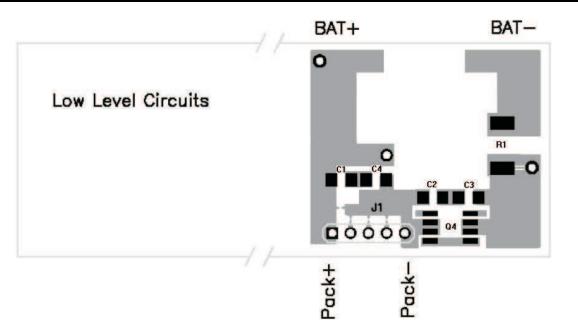


Figure 6. Separating High- and Low-Current Sections Provides an Advantage in Noise Immunity

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