bq27500-V100 to bq27500-V120 CHANGE LIST

Ming Yu *Battery Management Solutions*

ABSTRACT

This document describes the change made from bq27500-V100 to bq27500-V120. The latest ordering information and data sheet is on the TI Web site. Note that bq27500-V100 uses FW version 1.08 and the bq27500-V120 uses FW version 1.20.

1 Introduction

bq27500-V120 firmware has been released to enable several feature additions.

The following new orderable part numbers have been released to support this firmware-upgraded device:

- bq27500DRZR-V120
- bq27500DRZT-V120

The latest version of the evaluation software is required to be able to read and write all the data flash configuration locations.

2 Change Details

Table 1. Change Details

CHANGE	bq27500-V120	bq27500-V100	COMMENTS
Enable timeout on I^{2}C™ transactions	bq27500 re-initializes the I^{2}C engine if the timeout condition is met.	bq27500 does not take any action, and it is up to other I^{2}C masters to restart I^{2}C	Makes bq27500 more robust to other I^{2}C masters
Reduce bq27500 initialization time	Initialization time is less than 2 seconds	Initialization time is approximately 3-4 seconds	Reduced the initial wait time during system power up
Add truncation and rounding calculation in ImpedanceTrack™ (IT) algorithm	Truncation and rounding method added for impedance calculation	No truncation and rounding calculation in IT	Improve bq27500 gauging accuracy at low temperature
Add Coulomb Counter offset calibration delay at POR or RESET	The first Coulomb Counter offset calibration is delayed 225 seconds at POR or RESET	The first Coulomb Counter offset calibration is immediately after POR or RESET	To avoid false calibration if a large inrush current occurs when power is applied
Eliminate partial reset detection	No partial reset detection	Has partial reset detection	Removing the partial reset detection and force a full reset refreshes the RAM with initialization value. This eliminates the impact of old value stored in RAM.
Enable 400-kHz I^{2}C	I^{2}C speed up to 400 kHz	I^{2}C speed up to 100 kHz	Required by high-speed system.

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Table 1. Change Details (continued)

CHANGE	bq27500-V120	bq27500-V100	COMMENTS
Change power state to enable Sleep Plus mode	Both Sleep and Sleep Plus mode are enabled. In Sleep Plus mode, HFO stays on and no clock stretch occurs on I^2C transaction. The Sleep Plus mode current consumption is higher than that of Sleep mode due to HFO is running.	Only Sleep mode is enabled, In Sleep mode, High Frequency Oscillator (HFO) is turned off. An approximate 4- to 8-ms clock stretch occurs on all I^2C transaction during Sleep mode	In some applications, I^2C communication requires higher speed, which does not allow the 4- to 8-ms clock stretch from bq27500.
Enable OCV measurement for small duration and high spike load by change default data flash setting (Hidden DF)	OCV wait time is set to 60 seconds, and discharge relax time is set to 60 seconds	OCV wait time is set to 1800 seconds, and discharge relax time is set to 1800 seconds.	Allow OCV update for push-mail-type application, which has load profile of a very short duration and high spike.

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