

## SBData Commands for PowerLAN<sup>™</sup> Master Gateway Controller

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#### ABSTRACT

The Smart Battery Data (SBData) Interface is a list of commands that have become a standard in lithium-ion battery management applications. The bq78PL116 supports this standard command set and also includes additional commands to allow some control of its unique operation. These additional commands are called SBData Commands for the PowerLAN<sup>™</sup> Master Gateway Controller and use standard SMBus transactions.

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Background

#### 1 Background

The communications protocol described in this application report uses standard SMBus transactions. See the System Management Bus Specification version 1.1 for details on this protocol. In particular, the transactions Write Word and Read Word are used. The specifics of the SMBus transactions – like timing, ACK/NACK, PEC, etc. – are not described. Transactions can be done with or without the use of the Packet Error Checking (PEC).

- **NOTE:** This protocol is available in the bq78PL114S12 and the bq78PL116. This application report can be applied to both products with the following exceptions for the bq78PL114S12:
  - 1. The bq78PL114S12 does not have the PASSWORD command nor an access level feature. When unlocking the device, simply use the UNLOCK command.
  - 2. The bq78PL114S12 does not have the RESET FUSE and TOGGLE SHIP BIT commands.
  - 3. The COMMAND and DATA registers for the bq78PL114S12 are at 0x50 and 0x51, respectively.
  - 4. The bq78PL114S12 requires the use of PEC.

## 2 **Protocol Description**

#### 2.1 Command and Data Registers

The SBData Commands for the PowerLAN<sup>™</sup> Master Gateway Controller use two SBData address locations to perform tasks that are specific to the PowerLAN<sup>™</sup> Master Gateway Controller (hereafter referred to as PowerLAN<sup>™</sup> Gateway). The first location, called COMMAND, is used to get device status or send commands. The second location, called DATA, is used to read Parameter Data from the bq78PL116 and also load values for commands.

In the bq78PL116, these locations are COMMAND = 0x80 and DATA = 0x81. A summary of COMMAND and DATA is shown in the following tables.

| SBData<br>Command | Mode  | Description | Format              | Size (Bytes) | Description  |
|-------------------|-------|-------------|---------------------|--------------|--|
| 0x80              | Read  | COMMAND     | Unsigned<br>Integer | 2            | A read returns the device status.  |
| 0x80              | Write | COMMAND     | Unsigned<br>Integer | 2            | A write implements one of the PowerLAN <sup>™</sup> commands.                              |
| 0x81              | Read  | DATA        | Unsigned<br>Integer | 2            | Preceded by a COMMAND write, a DATA read returns the value of the COMMAND Data             |
| 0x81              | Write | DATA        | Unsigned<br>Integer | 2            | Followed by a COMMAND write, a DATA write sends data to Parameter associated with COMMAND. |

Table 1. PowerLAN<sup>™</sup> SBData Commands for bq78PL116

Read and Write modes are determined by the least significant bit (LSB) of the device address byte. An LSB = 0 indicates a write, and an LSB = 1 indicates a read. The default address for the bq78PL116 is 0x16 for writes and 0x17 for reads.

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## 2.2 PowerLAN<sup>™</sup> Gateway Status

The status of the PowerLAN<sup>™</sup> Gateway can be read for a variety of reasons. Reading the status of the bq78PL116 while performing transactions promotes reliable communications. Querying device status can provide error checking, indication of a locked or unlocked device, and when a command is completed. The 12 status values are described in Table 2.

| Value           | Description                    |
|-----------------|--------------------------------|
| 0x0000          | Ready.                         |
| 0x8001          | Busy.                          |
| 0x8081          | Invalid Command, Locked        |
| 0x808A          | Invalid Command, Unlocked      |
| 0x8101          | Read Error, Safety Timers      |
| 0x8102          | Read Error, Safety Limits      |
| 0x8103          | Read Error, Pack Configuration |
| 0x8104          | Read Error, User Command       |
| 0x8105          | Write Error, Safety Timers     |
| 0x8106          | Write Error, Safety Limits     |
| 0x8107          | Write Error, Safety Timers     |
| 0x8200 – 0x82FF | SBData layer Errors            |

 Table 2. Device Status Words

## 2.3 Commands

The commands provided in this protocol allow the user to perform the following simple tasks:

- Read and write a subset of the Parameter Set. The parameter set is described in the *bq78PL116 Technical Reference Manual* (<u>SLUU481</u>). The accessible parameter subset consists of Safety Rule settings, Charge Control settings, and two Configuration registers. Not all parameters are writable through SBData commands for the PowerLAN<sup>™</sup> Gateway. See the tables later in this document for a complete listing.
- Calibration of current offset and gain and temperature offset.
- The Commit command is provided to save calibration values.
- Relearn/Initialize command is included so that changes to the parameter set can be relearned after a change.
- Reset Fuse command clears the permanent failure condition and the Fuse bit.
- Toggle Ship Bit command places bq78PL116 into the lowest power state with wake up only when the SBData pins (SBCLK, SBDAT) are pulled up.

Table 3 shows the listing of the SBData Commands for the PowerLAN<sup>™</sup> Gateway.

| Command Name      | Command Value | Description   |
|-------------------|---------------|---|
| POWERPUMP ENABLE  | 0x180F        | Clear bit 15 of System Control to enable PowerPump <sup>™</sup> technology  |
| POWERPUMP DISABLE | 0x190F        | Set bit 15 of System Control to disable PowerPump <sup>™</sup> technology   |
| UNLOCK            | 0x1A91        | Unlock device for 60 seconds of access to SBData Commands for<br>PowerLAN™ Gateway. After this time, the device is locked unless another<br>SBData Command for the PowerLAN™ Gateway is sent. |
| LOCK              | 0x1A19        | Lock device from access to SBData Commands for PowerLAN <sup>™</sup> Gateway. A locked device only prevents access to SBData commands for the PowerLAN <sup>™</sup> Gateway                   |
| PASSWORD          | 0x1Bii        | Write word (two bytes) to password register. Valid values for ii are 00-03.   |
| CURRENT CAL ZERO  | 0x2000        | Calibrate current offset.   |
| CURRENT CAL GAIN  | 0x2001        | Calibrate current gain.   |
| TEMP CAL          | 0x2002        | Calibrate Temperature sensors.  |

| Table 3. SBData | <b>Commands for</b> | PowerLAN™ | Gateway |
|-----------------|---------------------|-----------|---------|
|-----------------|---------------------|-----------|---------|

|                    |               | ,  |
|--------------------|---------------|--|
| Command Name       | Command Value | Description  |
| COMMIT             | 0x2003        | Commit data to flash.  |
| RELEARN INITIALIZE | 0x2007        | Relearn/Initialize command.  |
| RESET FUSE         | 0x200B        | Clear the permanent failure condition (FUSE); clear SPROT output.    |
| TOGGLE SHIP BIT    | 0x2010        | Toggle the ship mode bit.  |
| WRITE TIMER        | 0x21ii        | Write the value of a Safety Timer[ii] = parameter 0x00pp.            |
| WRITE THRESHOLD    | 0x22jj        | Write the value of a Safety Limit[jj] = parameter PPpp.              |
| READ TIMER         | 0x23ii        | Read Safety Timer [ii] through Least Significant Byte (LSB) of DATA. |
| READ THRESHOLD     | 0x24jj        | Read Safety Limit [jj] through DATA.                                 |

#### Table 3. SBData Commands for PowerLAN<sup>™</sup> Gateway (continued)

## 2.3.1 PASSWORD (Seal/Unseal)

The PASSWORD command writes the password two bytes at a time. The bq78PL116 can be configured so that user access is restricted. This historically has been referred to as sealing or unsealing the pack in TI Battery Management devices (bq20zxx). The three access levels are shown in Table 4.

| Table 4. | bq78PL116 | User Ac | cess Levels |
|----------|-----------|---------|-------------|
|----------|-----------|---------|-------------|

| Level | Description   |  |
|-------|---|--|
| 0     | Access to SBData commands 0x00 to 0x23 and 0x3C to 0x59                                 |  |
| 1     | evel 0 Access and Access to Extended SBData commands for PowerLAN™ Gateway (0x80, 0x81) |  |
| 2     | Level 0 & 1 Access and full access to bq78PL116. (default)                              |  |

The default setting is access level 2 and the password for each level is blank (empty). Without implementation of the access level passwords, any user with bqWizard<sup>™</sup> software and access to the SMBus pins on the bq78PL116 battery pack can interrogate the device, change parameter settings, and copy the flash contents (.dat file). If the user wishes to implement data flash security, passwords for access levels 1 and 2 must be assigned. Password programming is initially done using the bqWizard<sup>™</sup> software and then later saved in the production clone file (.dat), also known as *golden flash file*.

Passwords are strings consisting of eight characters. Password values are created in the bqWizard<sup>™</sup> software. When providing password values in the SBData commands for the PowerLAN<sup>™</sup> Gateway, the ASCII representation of the string characters is used.

## 2.3.2 LOCK/UNLOCK

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SBData commands for the PowerLAN<sup>™</sup> Gateway in Table 3 are locked from use (except LOCK, UNLOCK, POWERPUMP ENABLE, POWERPUMP DISABLE). This means that use of the commands requires that the UNLOCK command be issued prior to command usage. If passwords are assigned, the UNLOCK command must be proceeded by the PASSWORD command.

The LOCK/UNLOCK feature also includes a timeout. The Unlocked condition expires after 60 seconds if the UNLOCK command is not sent.

## 2.3.3 POWERPUMP DISABLE/ENABLE

The most significant bit (MSB) of the System Control parameter, bit 15, is used to enable or disable PowerPump<sup>™</sup> operation. If bit 15 of this register is 1, the PowerPump<sup>™</sup> operation is disabled. If it is zero, the PowerPump<sup>™</sup> operation is enabled. The POWERPUMP ENABLE and POWERPUMP DISABLE commands clear or set bit 15 of the System Control register, respectively.

All the other bits in the System Control parameter have no function and must always remain as zero. This means System Control can only be 0x8000 or 0x0000.



## 2.3.4 CURRENT CAL GAIN/ CURRENT CAL ZERO/TEMP CAL

The commands CURRENT CAL ZERO and CURRENT CAL GAIN permit the calibration of the current measurement system. The command TEMP CAL permits calibration of the temperature sensors in the system. The bq78PL116 has one device sensor and up to four external sensors.

The typical production flow is to calibrate and program flash of the device (.dat file load) using the bq78PL11x API. However, an alternative production flow is available where loose bq78PL116 devices have their flash programmed in a test circuit with a 48QFN socket using the bq78PL11x API and then later are inserted onto each production PCB assembly. The bq78PL116 current measurement and temperature measurement systems then are calibrated using the CURRENT CAL GAIN, CURRENT CAL ZERO, and TEMP CAL commands.

Calibration of the temperature measurement system must be established prior to current calibration. Update to calibration values must always be followed by a COMMIT command.

## 2.3.5 COMMIT

The COMMIT command is used to save calibration values to flash after the calibration commands are used. This is the only use for the COMMIT command.

## 2.3.6 RELEARN/INITIALIZE

The RELEARN/INITIALIZE command is used to reload parameters that are not updated during normal firmware system flow and to reset the major firmware subsystems. It also clears long-term counters, transfers bq76PL102 voltage calibration data, and updates Relative State of Charge (RSOC) based on present cell voltages.

Typical usage of this command is after any changes are made to the Hardware Configuration parameter. It is also used to reset the gas gauge timers in order to trigger a Qmax update. See the *bq78PL116 Technical Reference Manual* (SLUU481) for more details.

## 2.3.7 RESET FUSE

The RESET FUSE command is used to clear the permanent failure condition that can be entered when certain Second Level Safety Rules are activated. A permanent failure causes all of the pack disconnect control pins (DSG, CHG, and PRE) to permanently go to zero, thereby permanently shutting off the battery pack.

## 2.3.8 TOGGLE SHIP MODE BIT

Ship mode operation is intended for the time between production and initial usage. Entrance and exit are intended to only happen once. This mode allows for lowest power consumption during long periods of initial storage.

#### 2.3.9 WRITE TIMER

Use the WRITE TIMER (0x21ii) command to change the value of the Safety Timers. See Table 5 for a description of the timers. The ii in the command code represents one of the entries in Table 3 (ii = 0, 1, 2, 3, ...).

The new word value of the safety timer is written to DATA (0x81). Because the timers are only one byte long, the top byte of the word value is always 0x00 making the word format appear as 0x00tt. Then, WRITE TIMER is written to COMMAND (0x80) in order to write the value 0x00tt.

## 2.3.10 WRITE THRESHOLD

Use the WRITE THRESHOLD (0x22jj) command to change the value of the Safety Thresholds. See Table 6 for description of these parameters. The jj in the command code represents one of the entries in Table 3 (jj = 0, 1, 2, 3, ...).

## 2.3.11 READ TIMER

Use the READ TIMER (0x23ii) command to read the value of the Safety Timers. See Table 5 for description of timers. The ii in the command code represents one of the entries in Table 3 (ii = 0, 1, 2, 3,  $\dots$ ).

## 2.3.12 READ THRESHOLD

Use the READ THRESHOLD (0x24jj) command to read the value of the Safety Thresholds. See Table 6 for description of these parameters. The jj in the command code represents one of the entries in Table 3 (jj = 0, 1, 2, 3, ...).

| Index (ii) | Name   | Units (Hexadecimal) |
|------------|--|---------------------|
| 0x00       | COV Time                                     | Seconds             |
| 0x01       | CUV Time                                     | Seconds             |
| 0x02       | POV Time                                     | Seconds             |
| 0x03       | PUV Time                                     | Seconds             |
| 0x04       | Over Current Charge Tier 1 Recovery          | Seconds             |
| 0x05       | Over Current Charge Tier 1 Time              | Seconds             |
| 0x06       | Over Current Discharge Tier 1 Recovery       | Seconds             |
| 0x07       | Over Current Discharge Tier 1 Time           | Seconds             |
| 0x08       | Over Current Charge Tier 2 Recovery          | Seconds             |
| 0x09       | Over Current Charge Tier 2 Time              | Seconds             |
| 0x0A       | Over Current Discharge Tier 2 Recovery       | Seconds             |
| 0x0B       | Over Current Discharge Tier 2 Time           | Seconds             |
| 0x0C       | Hardware Over Current Charge Recovery        | Seconds             |
| 0x0D       | Hardware Over Current Discharge Recovery     | Seconds             |
| 0x0E       | Hardware Over Current Short Circuit Recovery | Seconds             |
| 0x0F       | EUV Time                                     | Seconds             |
| 0x10       | Over Temperature Charge Time                 | Seconds RDTE        |
| 0x11       | Over Temperature Discharge Time              | Seconds RDTE        |
| 0x12       | Host Watchdog TimeOut                        | Seconds RDTE        |
| 0x13       | SOV Time                                     | Seconds RDTE        |
| 0x14       | Reserved                                     |                     |
| 0x15       | SOC Charge Time                              | Seconds RDTE        |
| 0x16       | SOC Discharge Time                           | Seconds RDTE        |
| 0x17       | SOT Charge Time                              | Seconds RDTE        |
| 0x18       | SOT Discharge Time                           | Seconds RDTE        |
| 0x19       | Open Temperature Sensor Time                 | Seconds RDTE        |
| 0x1A       | FET Fail Time                                | Seconds RDTE        |
| 0x1B       | Fuse Fail Time                               | Seconds RDTE        |
| 0x1C       | VLAN Fail Time                               | Seconds RDTE        |
| 0x1D       | Current Measurement Fail Time                | Seconds RDTE        |
| 0x1E       | Charge Completion Time                       | Seconds RDTE        |
| 0x1F       | Charge Completion FET Activation Time        | Seconds RDTE        |
| 0x20       | Discharge Completion Time                    | Seconds             |
| 0x21       | Discharge Completion FET Activation Time     | Seconds             |
| 0x22       | Board Over Temperature Time                  | Seconds RDTE        |
| 0x23       | Reserved                                     |                     |
| 0x24       | FD Set Voltage Time                          | Seconds             |
| 0x25       | TDA Set Voltage Time                         | Seconds             |

Table 5. Safety Parameter Timers (Write 0x21ii or Read 0x23ii)

| Index (ii) | Name                             | Units (Hexadecimal) |
|------------|----------------------------------|---------------------|
| 0x26       | Discharge Under Temperature Time | Seconds RDTE        |
| 0x27       | OCA activation time              | Seconds RDTE        |

## Table 5. Safety Parameter Timers (Write 0x21ii or Read 0x23ii) (continued)

## Table 6. Safety Parameter Thresholds (Write 0x22jj or Read 0x24jj)

| Index (jj) | Name                                      | Units (Hexadecimal) |
|------------|---|---------------------|
| 0x00       | COV Threshold                             | mV                  |
| 0x01       | COV Recovery                              | mV                  |
| 0x02       | COV High Temperature Threshold            | mV                  |
| 0x03       | COV High Temperature Adjust               | Kelvin              |
| 0x04       | CUV Threshold                             | mV                  |
| 0x05       | CUV Recovery                              | mV                  |
| 0x06       | POV Threshold                             | mV                  |
| 0x07       | POV Recovery                              | mV                  |
| 0x08       | PUV Threshold                             | mV                  |
| 0x09       | PUV Recovery                              | mV                  |
| 0x0A       | Over Current Charge Tier 1 Threshold      | mA                  |
| 0x0B       | Over Current Discharge Tier 1 Threshold   | mA                  |
| 0x0C       | Over Current Charge Tier 2 Threshold      | mA                  |
| 0x0D       | Over Current Discharge Tier 2 Threshold   | mA                  |
| 0x0E       | HSC Max Attempts                          | Integer             |
| 0x0F       | HOC Max Attempts                          | Integer             |
| 0x10       | Hardware Over Current Charge Threshold    | Integer             |
| 0x11       | Hardware Over Current Charge Time         | Integer             |
| 0x12       | Hardware Over Current Discharge Threshold | Integer             |
| 0x13       | Hardware Over Current Discharge Time      | Integer             |
| 0x14       | Hardware Short Circuit Threshold          | Integer             |
| 0x15       | Hardware Short Circuit Time               | Integer             |
| 0x16       | EUV Threshold                             | mV                  |
| 0x17       | EUV Recovery                              | mV                  |
| 0x18       | OT Charge Threshold                       | mV                  |
| 0x19       | OT Charge Recovery                        | mV                  |
| 0x1A       | OT Discharge Threshold                    | mV                  |
| 0x1B       | OT Discharge Recovery                     | mV                  |
| 0x1C       | SOV Threshold                             | mV                  |
| 0x1D       | Cell Imbalance Current                    | mA                  |
| 0x1E       | Cell Imbalance Fail Voltage               | mV                  |
| 0x1F       | Cell Imbalance Time                       | Seconds             |
| 0x20       | Cell Imbalance SOC Inhibit Threshold      | %                   |
| 0x21       | SOC Charge Threshold                      | mA                  |
| 0x22       | SOC Discharge Threshold                   | mA                  |
| 0x23       | SOT Charge Threshold                      | Kelvin              |
| 0x24       | SOT Discharge Threshold                   | Kelvin              |
| 0x25       | Open Temperature Sensor Threshold         | Kelvin              |
| 0x26       | Reserved                                  |                     |
| 0x27       | Fuse Fail Limit                           | mA                  |
| 0x28       | IGR Limit                                 | Integer             |
| 0x29       | IGR Fail Count                            | Integer             |

| Index (jj)   | Name  | Units (Hexadecimal)                    |  |
|--------------|---|--|--|
| 0x2A         | IGR Ratio Limit                             | Integer                                |  |
| 0x2B         | IGR Ratio Fail Count                        | Integer                                |  |
| 0x2C         | Rate Limit Threshold                        | Integer                                |  |
| 0x2D         | Rate Limit Activation Count                 | Integer                                |  |
| 0x2E         | Charge Inhibit Temperature Low              | Kelvin                                 |  |
| 0x2F         | Charge Inhibit Recovery Temperature Low     | Kelvin                                 |  |
| 0x30         | Charge Inhibit Temperature High             | Kelvin                                 |  |
| 0x31         | Charge Inhibit Recovery Temperature High    | Kelvin                                 |  |
| 0x32         | Pre-charge Temperature                      | Kelvin                                 |  |
| 0x33         | Pre-charge Voltage                          | mV                                     |  |
| 0x34         | Pre-charge Voltage Timeout                  | Seconds RDTE                           |  |
| 0x35         | Charge Suspend Temperature Low              | Kelvin                                 |  |
| 0x36         | Charge Suspend Recovery Temperature Low     | Kelvin                                 |  |
| 0x37         | Charge Suspend Temperature High             | Kelvin                                 |  |
| 0x38         | Charge Suspend Recovery Temperature High    | Kelvin                                 |  |
| 0x39         | HOC Max Attempts                            | Hardware over current max tries        |  |
| 0x3A         | Charge Completion Time                      | Seconds RDTE                           |  |
| 0x3B         | Reserved                                    | Reserved                               |  |
| 0x3C         | Reserved                                    |  |  |
| 0x3D         | Reserved                                    |  |  |
| 0x3E         | Reserved                                    |  |  |
| 0x3F         | Reserved                                    |  |  |
| 0x40         | Reserved                                    |  |  |
| 0x41         | Charge Completion Pack Voltage Qualifier    | mV                                     |  |
| 0x42         | Charge Completion Taper Current Qualifier   | mV                                     |  |
| 0x43         | Discharge Completion Pack Voltage Qualifier | mV                                     |  |
| 0x44         | FD Clear SOC Threshold                      | %                                      |  |
| 0x45         | FD Clear Voltage                            | mV                                     |  |
| 0x46         | FC Clear SOC Threshold                      | %                                      |  |
| 0x47         | FC Set SOC Threshold                        | %                                      |  |
| 0x48         | Hardware Configuration                      | Bit Wise Defined                       |  |
| 0x49         | Reserved                                    |  |  |
| 0x4A         | Minimum cell differential for balancing     | mV                                     |  |
| 0x4B         | Transition to idle current                  | mA                                     |  |
| 0x4C         | Transition to idle time                     | Seconds                                |  |
| 0x4D         | Transition to Discharge Current             | mA                                     |  |
| 0x4E         | Transition to Charge Current                | mA                                     |  |
| 0x4E<br>0x4F | Reserved                                    |  |  |
| 0x50         | Current Delta                               | mA                                     |  |
| 0x50<br>0x51 | Sense Resistance                            | Micro Ohms (Read Only)                 |  |
| 0x52         | FCC Learn Qualifier                         | %                                      |  |
| 0x52         | Cycle Fade                                  | ~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~ |  |
| 0x53<br>0x54 | Min OCV Slope                               | mV/% RSOC                              |  |
| 0x54<br>0x55 | OCV Idle Qualifier                          | Minutes                                |  |
| 0x55<br>0x56 | Stale FCC Timeout                           |  |  |
| 0,00         | Reserved                                    | Minutes                                |  |
| 0x57         |   |  |  |

Table 6. Safety Parameter Thresholds (Write 0x22jj or Read 0x24jj) (continued)

| Index (jj) | Name                                  | Units (Hexadecimal) |
|------------|---------------------------------------|---------------------|
| 0x59       | Hardware LP Discharge Duration        | Integer             |
| 0x5A       | Hardware LP Charge Threshold          | Integer             |
| 0x5B       | Hardware LP Charge Duration           | Integer             |
| 0x5C       | EPD Pump Time                         | Cycle Counts        |
| 0x5D       | EPD Write Time                        | Cycle Counts        |
| 0x5E       | Default Charging Current              | mA                  |
| 0x5F       | Default Charging Voltage              | mV                  |
| 0x60       | Capacity Algorithm                    | Bit Wise Defined    |
| 0x61       | User Rate                             | mA                  |
| 0x62       | Precharge Current                     | mA                  |
| 0x63       | Reserved                              |                     |
| 0x64       | Reserved                              |                     |
| 0x65       | Reserved                              |                     |
| 0x66       | Reserved                              |                     |
| 0x67       | Board Over Temperature                | Kelvin              |
| 0x68       | Board Over Temperature Recovery       | Kelvin              |
| 0x69       | TDA Clear SOC Threshold               | %                   |
| 0x6A       | TCA Clear SOC Threshold               | %                   |
| 0x6B       | Pre-charge Recovery                   | mV                  |
| 0x6C       | FD Set SOC Threshold                  | %                   |
| 0x6D       | FD Set Voltage                        | mV                  |
| 0x6E       | TDA Set SOC Threshold                 | %                   |
| 0x6F       | TCA Set SOC Threshold                 | %                   |
| 0x70       | TDA Set Volt                          | mV                  |
| 0x71       | TDA Clear Volt                        | mV                  |
| 0x72       | Discharge Under Temperature Threshold | Kelvin              |
| 0x73       | Discharge Under Temperature Recovery  | Kelvin              |
| 0x74       | OCA Set Voltage                       | mV                  |
| 0x75       | Reserved                              |                     |
| 0x76       | System Control                        | Bit Wise Defined    |
| 0x77       | Display Driver Frequency              | Hz                  |

Table 6. Safety Parameter Thresholds (Write 0x22jj or Read 0x24jj) (continued)

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#### Usage

## 3 Usage

#### 3.1 SMBus Read/Write Word

Most if not all the SBData Commands for the PowerLAN<sup>™</sup> Gateway involve the use of the SMBus transactions called Read Word and Write Word. They can be conducted with or without Packet Error Checking (PEC). See the SMBus Specification Rev 1.1 for complete details on how the SMBus protocol works.

#### 3.1.1 SMBus Read Word

The SMBus Read Word with PEC is shown here for convenience. Consult the full SMBus Specification for complete explanation of this transaction. PEC usage is not required.

The following notations are used in this discussion:

- [S] = Start Bit (SMBDAT transition low, clock high)
- [P] = Stop Bit (SMBCLK transition high, clock high)
- [R] = Read Bit (1)
- [W] = Write Bit (0)
- [ACK] = Acknowledge
- [NACK] = Not acknowledge
- [PEC] = Packet Error Checking byte

#### Table 7. SMBus Read Word With PEC

| Bits | 1 | 7       | 1 | 1   | 8       | 1   | 8        | 1   | 8        | 8   | 1   | 1 |
|------|---|---------|---|-----|---------|-----|----------|-----|----------|-----|-----|---|
|      | S | ADDRESS | W | ACK | COMMAND | ACK | DATA LSB | ACK | DATA MSB | PEC | ACK | Р |

#### 3.1.2 SMBus Write Word

The SMBus Write Word with PEC is shown here for convenience. Consult the full SMBus Specification for complete explanation of this transaction. PEC usage is not required.

#### **Table 8. SMBus Write Word With PEC**

| ſ | Bits | 1 | 7       | 1 | 1   | 8       | 1   | 8        | 1   | 8        | 8   | 1   | 1 |
|---|------|---|---------|---|-----|---------|-----|----------|-----|----------|-----|-----|---|
|   |      | s | ADDRESS | W | ACK | COMMAND | ACK | DATA LSB | ACK | DATA MSB | PEC | ACK | Р |

## 3.2 Read Device Status

The PowerLAN<sup>™</sup> Gateway status is queried with a SMBus Read Word command to register 0x80.

#### 3.2.1 Read 0x80 (BUSY Status Is Returned in Example):

| Bits | 1 | 7        | 1 | 1   | 8         | 1   | 8         | 1   | 8         | 1   | 1 |
|------|---|----------|---|-----|-----------|-----|-----------|-----|-----------|-----|---|
|      | S | 0001 011 | 1 | ACK | 1000 0000 | ACK | 0000 0001 | ACK | 1000 0000 | ACK | Р |



## 3.3 Unlock a Password-Protected Device

Unlocking a password-protected device requires four pairs of SMBus Write Word transactions followed by a single SMBus Write Word transaction. The password in this example is "POWERLAN". The ASCII representation of POWERLAN, in hexadecimal, is 50, 4F, 57, 45, 52, 4C, 41, 4E. It is described as follows:

## 3.3.1 Write 0x504F ("PO") to 0x81 and Then Write 0x1B00 to 0x80:

| Bits | 1 | 7        | 1 | 1   | 8         | 1   | 8         | 1   | 8         | 1   | 1 |
|------|---|----------|---|-----|-----------|-----|-----------|-----|-----------|-----|---|
|      | S | 0001 011 | 0 | ACK | 1000 0001 | ACK | 0100 1111 | ACK | 0101 0000 | ACK | Р |
|      |   |          |   |     |           |     |           |     |           |     |   |
|      |   |          |   | I   |           | I   |           |     |           |     |   |
| Bits | 1 | 7        | 1 | 1   | 8         | 1   | 8         | 1   | 8         | 1   | 1 |

## 3.3.2 Write 0x5745 ("WE") to 0x81 and Then Write 0x1B01 to 0x80:

| Bits | 1 | 7        | 1 | 1   | 8         | 1   | 8         | 1   | 8         | 1   | 1 |
|------|---|----------|---|-----|-----------|-----|-----------|-----|-----------|-----|---|
|      | S | 0001 011 | 0 | ACK | 1000 0001 | ACK | 0100 0101 | ACK | 0101 0111 | ACK | Р |
|      |   |          |   |     |           |     |           |     |           |     |   |
|      |   |          |   |     |           |     |           |     |           |     |   |
| Bits | 1 | 7        | 1 | 1   | 8         | 1   | 8         | 1   | 8         | 1   | 1 |

## 3.3.3 Write 0x524C ("RL") to 0x81 and Then Write 0x1B02 to 0x80:

| Bits | 1 | 7        | 1 | 1   | 8         | 1   | 8         | 1   | 8         | 1   | 1 |
|------|---|----------|---|-----|-----------|-----|-----------|-----|-----------|-----|---|
|      | S | 0001 011 | 0 | ACK | 1000 0001 | ACK | 0100 1100 | ACK | 0101 0010 | ACK | Р |
|      |   |          |   |     |           |     |           |     |           |     |   |
| Bits | 1 | 7        | 1 | 1   | 8         | 1   | 8         | 1   | 8         | 1   | 1 |
|      | S | 0001 011 | 0 | ACK | 1000 0000 | ACK | 0000 0010 | ACK | 0001 1011 | ACK | Р |

## 3.3.4 Write 0x414E ("AN") to 0x81 and Then Write 0x1B03 to 0x80:

| Bits | 1 | 7        | 1 | 1   | 8         | 1   | 8         | 1   | 8         | 1   | 1 |
|------|---|----------|---|-----|-----------|-----|-----------|-----|-----------|-----|---|
|      | S | 0001 011 | 0 | ACK | 1000 0001 | ACK | 0100 1110 | ACK | 0100 0001 | ACK | Р |
|      |   |          |   |     |           |     |           |     |           |     |   |
| Bits | 1 | 7        | 1 | 1   | 8         | 1   | 8         | 1   | 8         | 1   | 1 |
|      | S | 0001 011 | 0 | ACK | 1000 0000 | ACK | 0000 011  | ACK | 0001 1011 | ACK | Р |

# 3.3.5 Write 0x1A91 to 0x80 to UNLOCK the bq78PL116's SBData Commands for PowerLAN™ Gateway.

| Bits | 1 | 7        | 1 | 1   | 8         | 1   | 8        | 1   | 8         | 1   | 1 |
|------|---|----------|---|-----|-----------|-----|----------|-----|-----------|-----|---|
|      | S | 0001 011 | 0 | ACK | 1000 0000 | ACK | 0000 011 | ACK | 0101 1011 | ACK | Р |

If the password is blank (default), only preceding step 5 needs to be performed.

**NOTE:** All explanations from here forward assume that the bq78PL116 is unlocked and has a Ready Status. The user must make use of the Read Device Status procedure to ensure that communications are effective.



#### Usage

#### 3.4 Lock a Device

Locking a device can happen automatically if more than one minute passes without the occurrence of any SBData Commands for the PowerLAN<sup>™</sup> Gateway. To intentionally lock the device, perform the following:

#### 3.4.1 Write 0x1A19 to 0x81:

| Bits | 1 | 7        | 1 | 1   | 8         | 1   | 8         | 1   | 8         | 1   | 1 |
|------|---|----------|---|-----|-----------|-----|-----------|-----|-----------|-----|---|
|      | S | 0001 011 | 0 | ACK | 1000 0000 | ACK | 0001 1001 | ACK | 0101 1010 | ACK | Р |

#### 3.5 Read a Safety Parameter Timer

Reading a Safety Parameter Timer value from those listed in Table 5 requires that a SMBus Write Word command be sent using a properly indexed (ii) parameter code through register 0x80. Then, the value is read back using a SMBus Read Word command and register 0x81. Only the LSB of the returned word is used because all timer values are only one byte.

#### 3.5.1 Write 0x23ii to 0x80 (0x2300 = Read COV Time):

| [ | Bits | 1 | 7        | 1 | 1   | 8         | 1   | 8         | 1   | 8         | 1   | 1 |
|---|------|---|----------|---|-----|-----------|-----|-----------|-----|-----------|-----|---|
|   |      | S | 0001 011 | 0 | ACK | 1000 0000 | ACK | 0000 0000 | ACK | 0010 0011 | ACK | Р |

#### 3.5.2 Read 0x81 (Default Result for COV Time is 0x02):

| В | its | 1 | 7        | 1 | 1   | 8         | 1   | 8         | 1   | 8         | 1   | 1 |
|---|-----|---|----------|---|-----|-----------|-----|-----------|-----|-----------|-----|---|
|   |     | S | 0001 011 | 0 | ACK | 1000 0001 | ACK | 0000 0010 | ACK | 0000 0000 | ACK | Р |

#### 3.6 Read a Safety Parameter Threshold

Reading a Safety Parameter Threshold value from those listed in Table 6 requires that a SMBus Write Word command be sent using a properly indexed (ii) parameter code through register 0x80. Then, the value is read back using a SMBus Read Word command and register 0x81.

#### 3.6.1 Write 0x24ii to 0x80 (0x2400 = Read COV Threshold):

| Bits | 1 | 7        | 1 | 1   | 8         | 1   | 8         | 1   | 8         | 1   | 1 |
|------|---|----------|---|-----|-----------|-----|-----------|-----|-----------|-----|---|
|      | S | 0001 011 | 0 | ACK | 1000 0000 | ACK | 0000 0010 | ACK | 0010 0100 | ACK | Р |

#### 3.6.2 Read 0x81 (Default Result for COV Threshold is 0x109A):

| Bits | 1 | 7        | 1 | 1   | 8         | 1   | 8         | 1   | 8         | 1   | 1 |
|------|---|----------|---|-----|-----------|-----|-----------|-----|-----------|-----|---|
|      | S | 0001 011 | 0 | ACK | 1000 0001 | ACK | 1001 1010 | ACK | 0001 0000 | ACK | Р |

## 3.7 Write a Safety Parameter Timer

Writing a Safety Parameter Timer value listed in Table 5 requires that the threshold value be written to 0x81 using a SMBus Write Word command. Then, the properly indexed command value is written to 0x80 using a SMBus Write Word command.

## 3.7.1 Write 0x0004 to 0x81 (COV Time = 4 seconds):

| Bits | 1 | 7        | 1 | 1   | 8         | 1   | 8         | 1   | 8         | 1   | 1 |
|------|---|----------|---|-----|-----------|-----|-----------|-----|-----------|-----|---|
|      | S | 0001 011 | 0 | ACK | 1000 0001 | ACK | 0000 0100 | ACK | 0000 0000 | ACK | Р |

## 3.7.2 Write 0x21ii to 0x80 (COV Time Command = 0x2100):

| Bits | 1 | 7        | 1 | 1   | 8         | 1   | 8         | 1   | 8         | 1   | 1 |
|------|---|----------|---|-----|-----------|-----|-----------|-----|-----------|-----|---|
|      | S | 0001 011 | 0 | ACK | 1000 0000 | ACK | 0000 0100 | ACK | 0010 0001 | ACK | Р |

## 3.8 Write a Safety Parameter Threshold

Writing a Safety Parameter Threshold value listed in Table 6 requires that the threshold value be written to 0x81 using a SMBus Write Word command. Then, the properly indexed command value is written to 0x80 using a SMBus Write Word command.

#### 3.8.1 Write 0x1068 to 0x81 (COV Threshold = 4200mV):

| Bi | ts | 1 | 7        | 1 | 1   | 8         | 1   | 8         | 1   | 8         | 1   | 1 |
|----|----|---|----------|---|-----|-----------|-----|-----------|-----|-----------|-----|---|
|    |    | S | 0001 011 | 0 | ACK | 1000 0001 | ACK | 0110 1000 | ACK | 0001 0000 | ACK | Р |

#### 3.8.2 Write 0x22ii to 0x80 (COV Time Command = 0x2200):

| Bits | 1 | 7        | 1 | 1   | 8         | 1   | 8         | 1   | 8         | 1   | 1 |
|------|---|----------|---|-----|-----------|-----|-----------|-----|-----------|-----|---|
|      | s | 0001 011 | 0 | ACK | 1000 0000 | ACK | 0000 0100 | ACK | 0010 0001 | ACK | Р |

## 3.9 Enable PowerPump<sup>™</sup> Circuitry

Enabling PowerPump<sup>™</sup> circuitry requires a SMBus Word Write to the 0x80 register.

#### 3.9.1 Write 0x180F to 0x80:

| Bits | 1 | 7        | 1 | 1   | 8         | 1   | 8         | 1   | 8         | 1   | 1 |
|------|---|----------|---|-----|-----------|-----|-----------|-----|-----------|-----|---|
|      | S | 0001 011 | 0 | ACK | 1000 0000 | ACK | 0000 1111 | ACK | 0001 1000 | ACK | Р |

## 3.10 Disable PowerPump<sup>™</sup> Circuitry

Disabling PowerPump<sup>™</sup> circuitry requires a SMBus Word Write to the 0x80 register.

#### 3.10.1 Write 0x190F to 0x80:

| ſ | Bits | 1 | 7        | 1 | 1   | 8         | 1   | 8         | 1   | 8         | 1   | 1 |
|---|------|---|----------|---|-----|-----------|-----|-----------|-----|-----------|-----|---|
|   |      | s | 0001 011 | 0 | ACK | 1000 0000 | ACK | 0000 1111 | ACK | 0001 1001 | ACK | Р |



## 3.11 Current Zero Offset Calibration

Calibration of the current measurement system for offset is done using a single SBData Word Write to register 0x80. Prior to executing this command, ensure that no current is flowing in the sense resistor. Continue to ensure zero current flow until after the status of the device is returned to READY (0x0000). Maintain power to the device until the COMMIT command can be executed. The COMMIT command must be executed in order for the calibration to be recorded. The COMMIT command must be executed in order for the calibration to be recorded.

## 3.11.1 Write 0x2000 to 0x80:

| [ | Bits | 1 | 7        | 1 | 1   | 8         | 1   | 8         | 1   | 8         | 1   | 1 |
|---|------|---|----------|---|-----|-----------|-----|-----------|-----|-----------|-----|---|
|   |      | s | 0001 011 | 0 | ACK | 1000 0000 | ACK | 0000 0000 | ACK | 0010 0000 | ACK | Р |

## 3.12 Current Gain Calibration

Calibration of the current measurement system for gain is done using a SBData Word Write to register 0x81 to load the value of current (in mA) present in the resistor. Then, a SBData Word write to register 0x80 is used to issue the gain calibration. Prior to executing this command, ensure that a known current is flowing in the sense resistor. Continue to have this current to flow until after the status of the device is returned to READY (0x0000). Maintain power to the device until the COMMIT command can be executed. The COMMIT command must be executed in order for the calibration to be recorded.

#### 3.12.1 Write 0x07D0 to 0x81 (Current = 2000 mA):

| Bits | 1 | 7        | 1 | 1   | 8         | 1   | 8         | 1   | 8         | 1   | 1 |
|------|---|----------|---|-----|-----------|-----|-----------|-----|-----------|-----|---|
|      | S | 0001 011 | 0 | ACK | 1000 0001 | ACK | 1101 0000 | ACK | 0000 0111 | ACK | Р |

## 3.12.2 Write 0x2001 to 0x80:

| Bits | 1 | 7        | 1 | 1   | 8         | 1   | 8         | 1   | 8         | 1   | 1 |
|------|---|----------|---|-----|-----------|-----|-----------|-----|-----------|-----|---|
|      | S | 0001 011 | 0 | ACK | 1000 0000 | ACK | 0000 0001 | ACK | 0010 0000 | ACK | Р |

#### 3.13 Temperature Offset Calibration

Calibration of the temperature measurement system for offset is done using a SBData Word Write to register 0x81 to load the value of ambient temperature (in °K). Then, a SBData Word write to register 0x80 is used to issue the offset calibration. Maintain power to the device until the COMMIT command can be executed. The COMMIT command must be executed in order for the calibration to be recorded.

#### 3.13.1 Write 0x012A to 0x81 (Temperature = 25°C or 298°K):

| Bits | 1 | 7        | 1 | 1   | 8         | 1   | 8         | 1   | 8         | 1   | 1 |
|------|---|----------|---|-----|-----------|-----|-----------|-----|-----------|-----|---|
|      | S | 0001 011 | 0 | ACK | 1000 0001 | ACK | 0010 1010 | ACK | 0000 0001 | ACK | Р |

#### 3.13.2 Write 0x2002 to 0x80:

| Bits | 1 | 7        | 1 | 1   | 8         | 1   | 8          | 1   | 8         | 1   | 1 |
|------|---|----------|---|-----|-----------|-----|------------|-----|-----------|-----|---|
|      | S | 0001 011 | 0 | ACK | 1000 0000 | ACK | 00000 0010 | ACK | 0010 0000 | ACK | Р |

## 3.14 Commit Calibration Data

The COMMIT command is used to write the calibration information to flash memory for permanent storage. Execution of the commit command requires a SMBus Write Word to register 0x80.

## 3.14.1 Write 0x2003 to 0x80:

| Bits | 1 | 7        | 1 | 1   | 8         | 1   | 8         | 1   | 8         | 1   | 1 |
|------|---|----------|---|-----|-----------|-----|-----------|-----|-----------|-----|---|
|      | S | 0001 011 | 0 | ACK | 1000 0000 | ACK | 0000 0011 | ACK | 0010 0000 | ACK | Р |

## 3.15 Clear Permanent Failure Condition (FUSE)

Clearing the permanent failure condition, or Fuse, requires a single SMBus Word Write to the 0x80 register.

#### 3.15.1 Write 0x200B to 0x80:

| Bits | 1 | 7        | 1 | 1   | 8         | 1   | 8         | 1   | 8         | 1   | 1 |
|------|---|----------|---|-----|-----------|-----|-----------|-----|-----------|-----|---|
|      | S | 0001 011 | 0 | ACK | 1000 0000 | ACK | 0000 1011 | ACK | 0010 0000 | ACK | Р |

## 3.16 Set Ship Mode

Setting the device into ship mode requires a single SMBus Word Write to the 0x80 register.

## 3.16.1 Write 0x2010 to 0x80:

| Bits | 1 | 7        | 1 | 1   | 8         | 1   | 8         | 1   | 8         | 1   | 1 |
|------|---|----------|---|-----|-----------|-----|-----------|-----|-----------|-----|---|
|      | S | 0001 011 | 0 | ACK | 1000 0000 | ACK | 0001 0000 | ACK | 0010 0000 | ACK | Р |

## 3.17 Relearn/Initialize

Issuing a RELEARN/INITIALIZE command requires a single SMBus Word Write to the 0x80 register.

#### 3.17.1 Write 0x2007 to 0x80:

| Bits | 1 | 7        | 1 | 1   | 8         | 1   | 8         | 1   | 8         | 1   | 1 |
|------|---|----------|---|-----|-----------|-----|-----------|-----|-----------|-----|---|
|      | S | 0001 011 | 0 | ACK | 1000 0000 | ACK | 0000 0111 | ACK | 0010 0000 | ACK | Р |

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