

# ***bq77905 Shutdown for Current Reduction***

Willy Massoth

BMS: Battery Monitoring &amp; Protection

## **ABSTRACT**

The *bq77905 3-5S Low-Power Protector* for lithium-ion batteries features a low 6- $\mu$ A typical supply current to extend battery life. Power tools or other applications where the battery is in storage or unused for long periods may want to prevent battery discharge during idle times. The schematic examples and test results in this document help the battery electronics designer when implementing a circuit topology to reduce battery current.

## **Contents**

1	Introduction .....	2
2	Single Device .....	3
3	Stacked Devices .....	7
4	References .....	12

## **List of Figures**

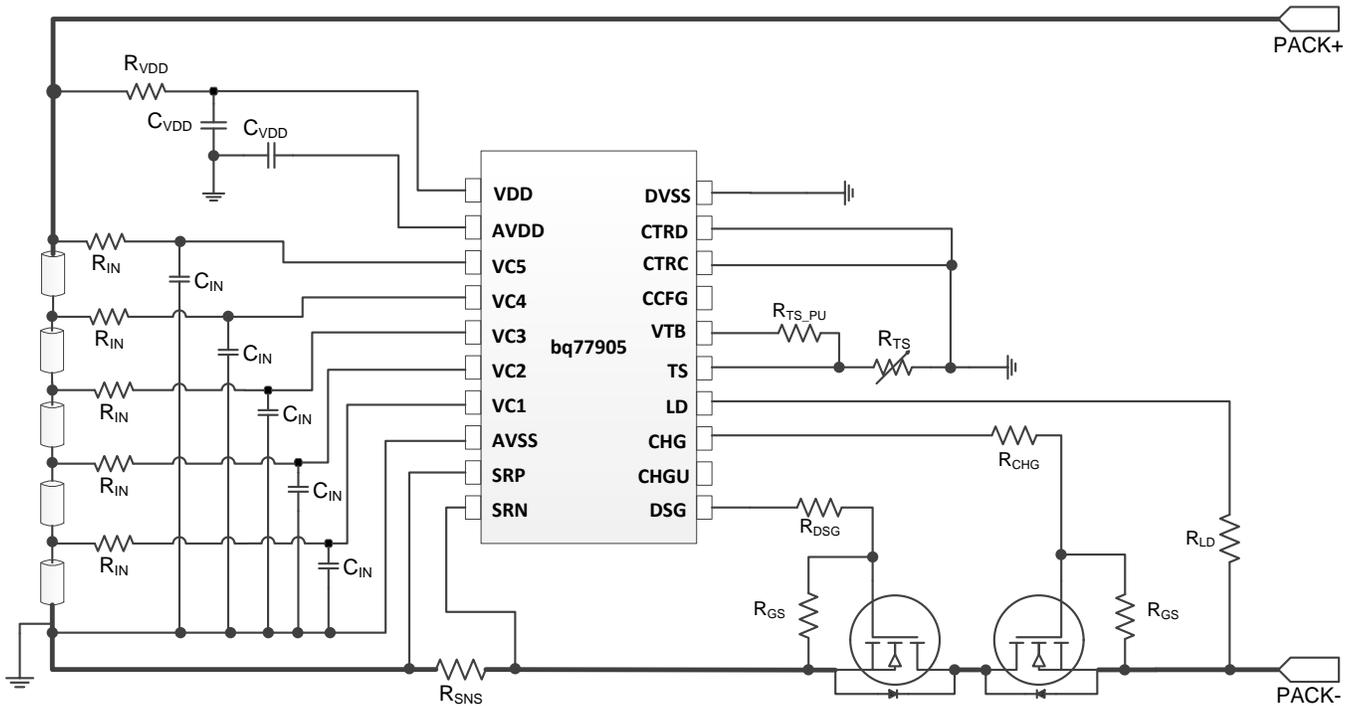
1	Common Circuit Implementation.....	2
2	Ineffective VDD Switch.....	3
3	Shutdown Circuit.....	4
4	Single Device Shutdown Example .....	5
5	Single Device Turn Off .....	6
6	Ineffective Switch With Stacked Devices Due To Leakage Path .....	7
7	Stacked Circuit Shutdown With CTRC and CTRD Leakage .....	8
8	Stacked Device Shutdown Circuit .....	9
9	Stacked Switch Example Test Circuit .....	10
10	Overtemperature Fault on Top Device .....	11
11	Stacked Devices Turn Off Using Test Circuit .....	12

## **Trademarks**

All trademarks are the property of their respective owners.

## 1 Introduction

The bq77905 3-5S low-power protector is an easy-to-use component for lithium-ion battery circuits. With the common simple schematic shown in Figure 1, the part is continuously powered. The current load on the battery is the low IC operating current, the load current of the  $R_{GS}$  resistors, and the open wire test currents. The low operating current of the bq77905 can give a long battery life, but some systems which are infrequently used may want to reduce the current.

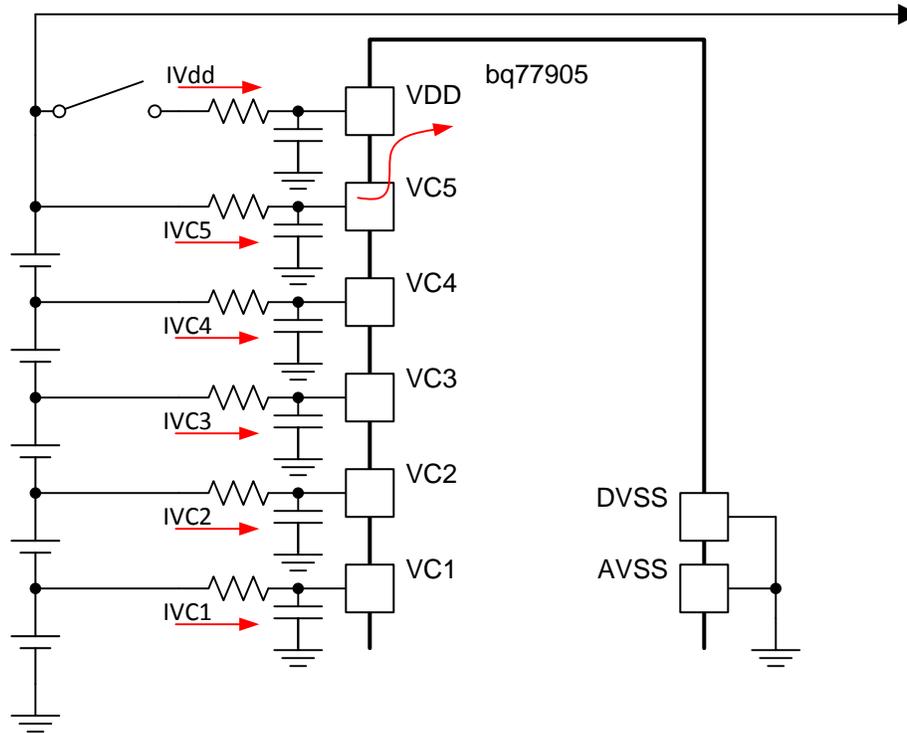


Copyright © 2016, Texas Instruments Incorporated

Figure 1. Common Circuit Implementation

## 2 Single Device

A typical attempt to reduce current is to disconnect power to the IC VDD pin while leaving the remainder of the IC connected similar to Figure 2. This approach is not effective with the bq77905 since there are internal leakage paths between VC5 and VDD. Disconnecting VDD with VC5 connected biases the part in a way which increases total current and provides an incorrect voltage for the top cell due to the voltage drop on the VC5 resistor.



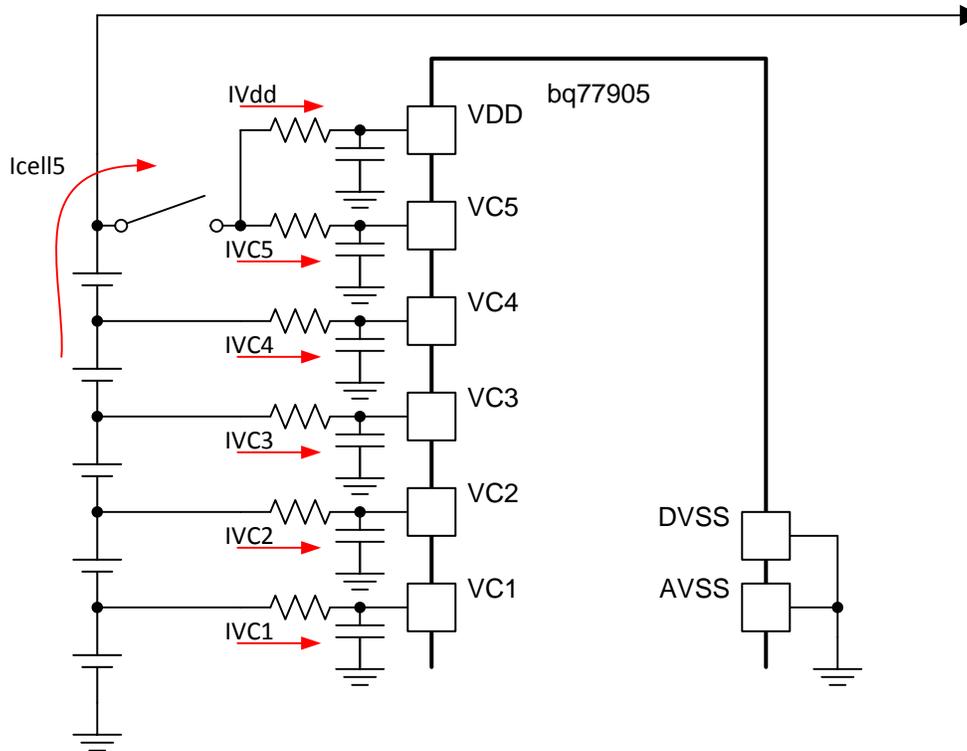
Copyright © 2017, Texas Instruments Incorporated

Figure 2. Ineffective VDD Switch

Table 1. Input Current Comparison

Input	Input Current, $\mu\text{A}$			
	Switch VDD Only		Switch Cell 5	
	ON	OFF	ON	OFF
VDD	6.03	0.000	6.03	0.000
VC5	0.109	37.6	0.109	0.000
VC4	0.114	0.114	0.115	0.000
VC3	0.112	0.112	0.113	0.000
VC2	0.101	0.101	0.102	0.000
VC1	0.108	0.108	0.109	0.000

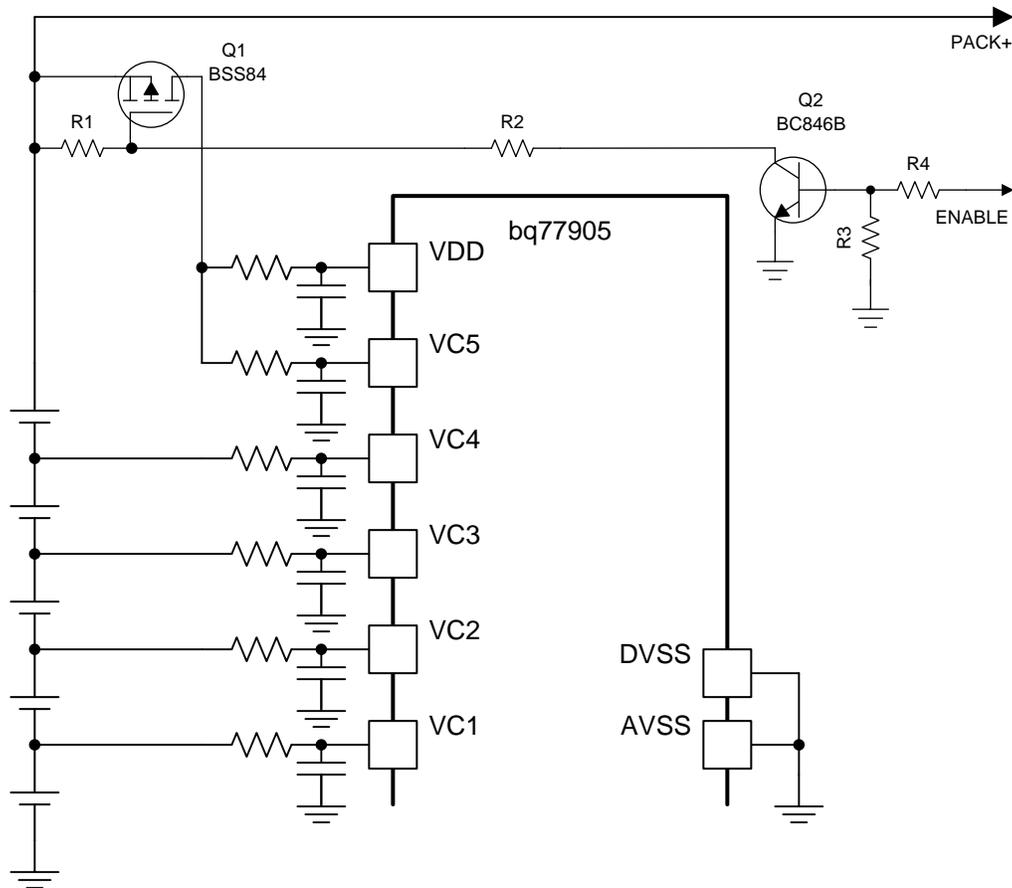
Moving the switch from the VDD to the common net from cell 5 breaks both the VDD and VC5 inputs to the part. This eliminates the current into the part. When the part shuts down, the open wire test current to the lower input pins is turned off. [Figure 3](#) shows the switch in the cell 5 connection. [Table 1](#) shows a comparison of switching only VDD and switching the common cell 5 connection.



Copyright © 2017, Texas Instruments Incorporated

**Figure 3. Shutdown Circuit**

A switch can be implemented and controlled as desired in the system. One method is to control a P-channel FET with either an N-channel FET or NPN. Figure 4 shows an example circuit with an ENABLE signal that could be connected to PACK+ to enable the pack. Table 2 shows the value used for the example test. With a low duty cycle the ON current is not a significant concern, but values could be optimized and transient protection added for a system design.



Copyright © 2017, Texas Instruments Incorporated

Figure 4. Single Device Shutdown Example

Table 2. Single Device Shutdown Example Component Values

Reference Designator	Value (kΩ)
R1	510
R2	510
R3	5.1
R4	30

Figure 5 shows example waveforms when ENABLE is disconnected from PACK+. The 10-M $\Omega$  scope probes load the circuit and will decrease the turn off time. The gate voltage falls as VDD drops until the gate is turned off by undervoltage or the shutdown threshold. With the drop in gate voltage, the part should not be turned off when the pack is loaded.

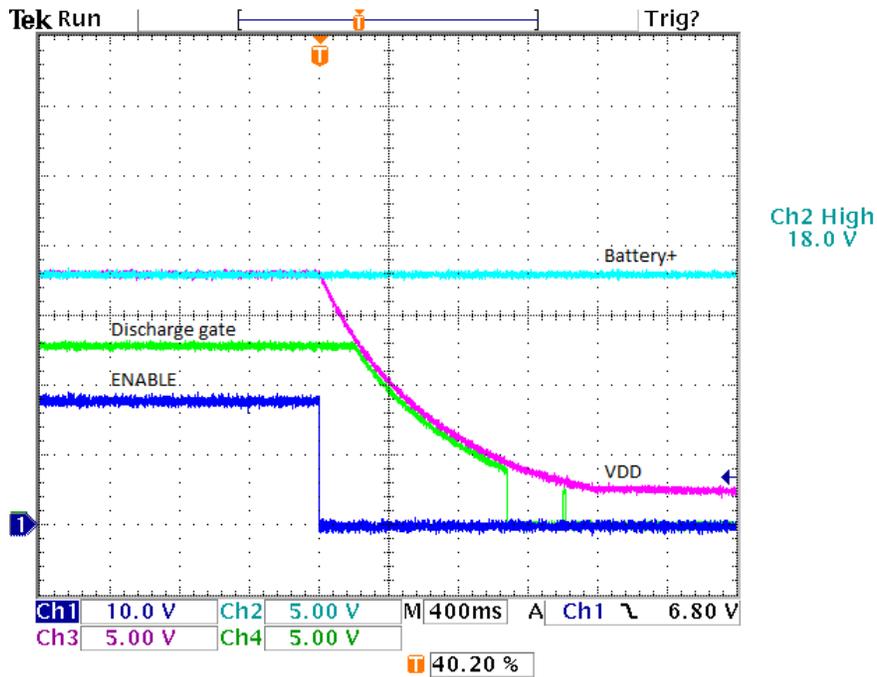
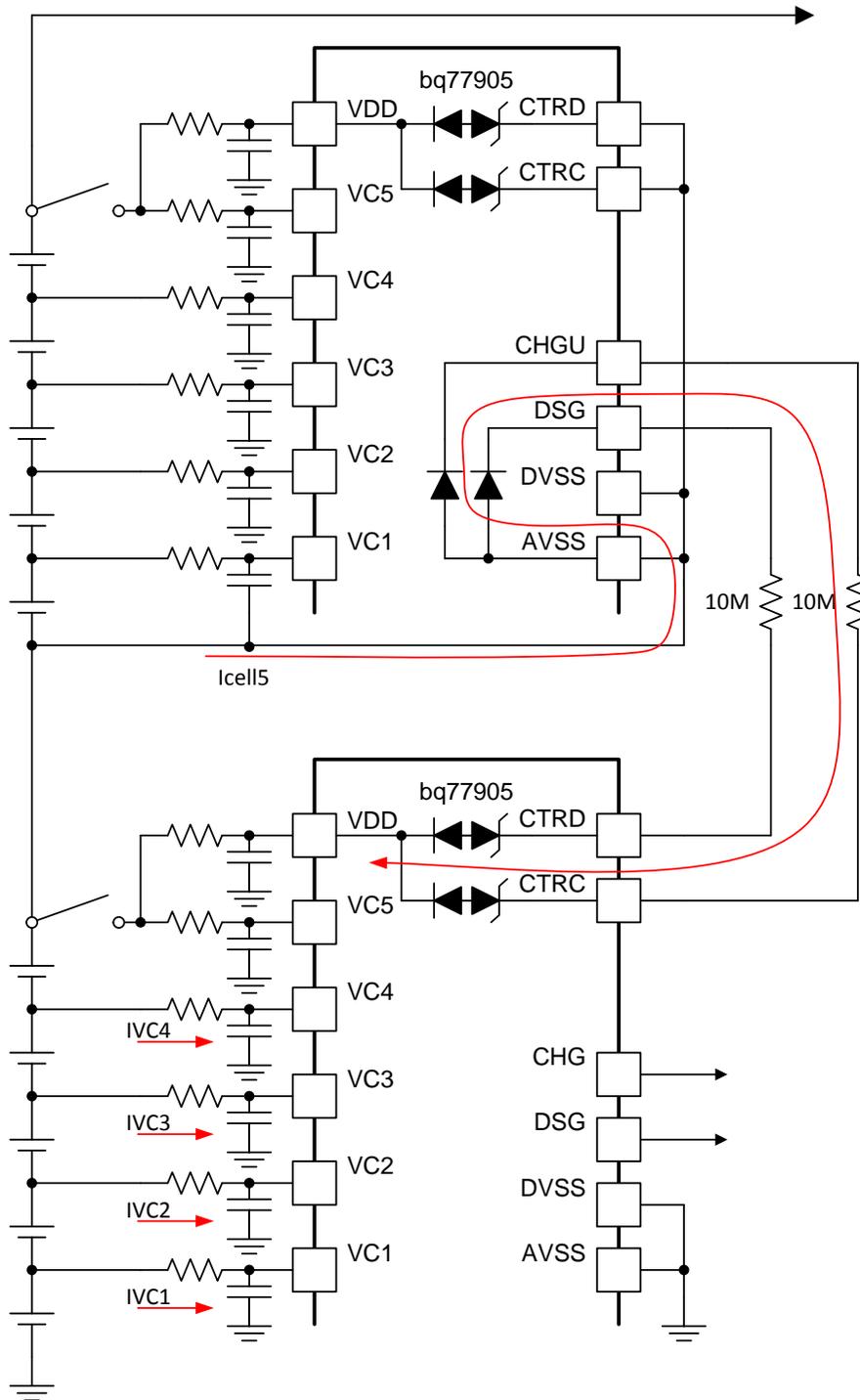


Figure 5. Single Device Turn Off

### 3 Stacked Devices

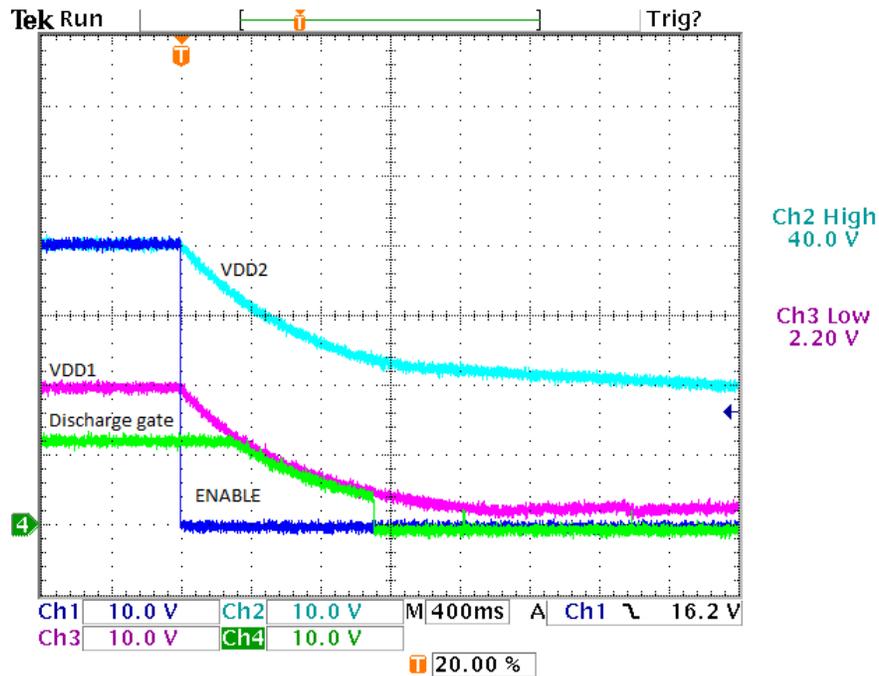
When devices are stacked for higher cell count packs the top cell for each part needs to be switched, but there is another consideration. The stacking interface includes a clamp to the VDD of the next lower part. This clamp can power the lower part from the FET outputs of the upper part since, even when off, the DSG and CHGU pins cannot fall substantially below the VSS voltage of the upper device. Figure 6 shows a switching concept and the internal clamps that prevent the power down of the lower part.



Copyright © 2017, Texas Instruments Incorporated

Figure 6. Ineffective Switch With Stacked Devices Due To Leakage Path

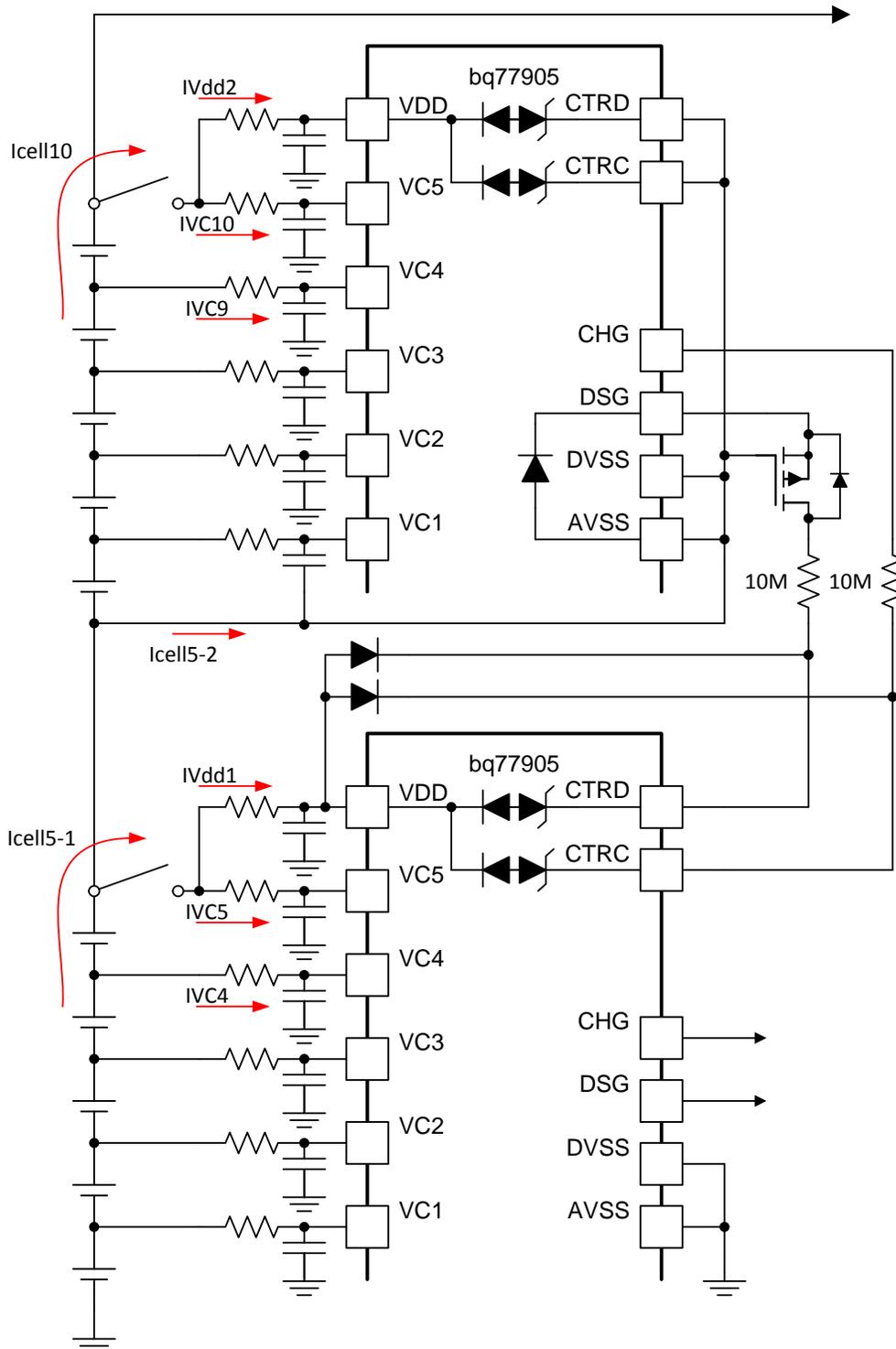
Figure 7 shows an example of switching only the upper cells to the devices. The scope probes load the circuit but the variation of VDD1 can be observed as the lower part oscillates between the  $V_{SHUT}$  and  $V_{POR}$  and levels.



**Figure 7. Stacked Circuit Shutdown With CTCR and CTRD Leakage**

To avoid the leakage from the upper FET outputs to the lower device power through the substrate diodes, the upper FET control signals must be allowed to fall below the VSS level. This function is built into the CHG pin, but must be externally implemented with the DSG pin. To prevent the CTRD and CTCR pins of the lower device from falling to VSS, and re-enabling the FETs in the case of a fault with the upper device during operation, diodes are used from the VDD pin of the lower device.

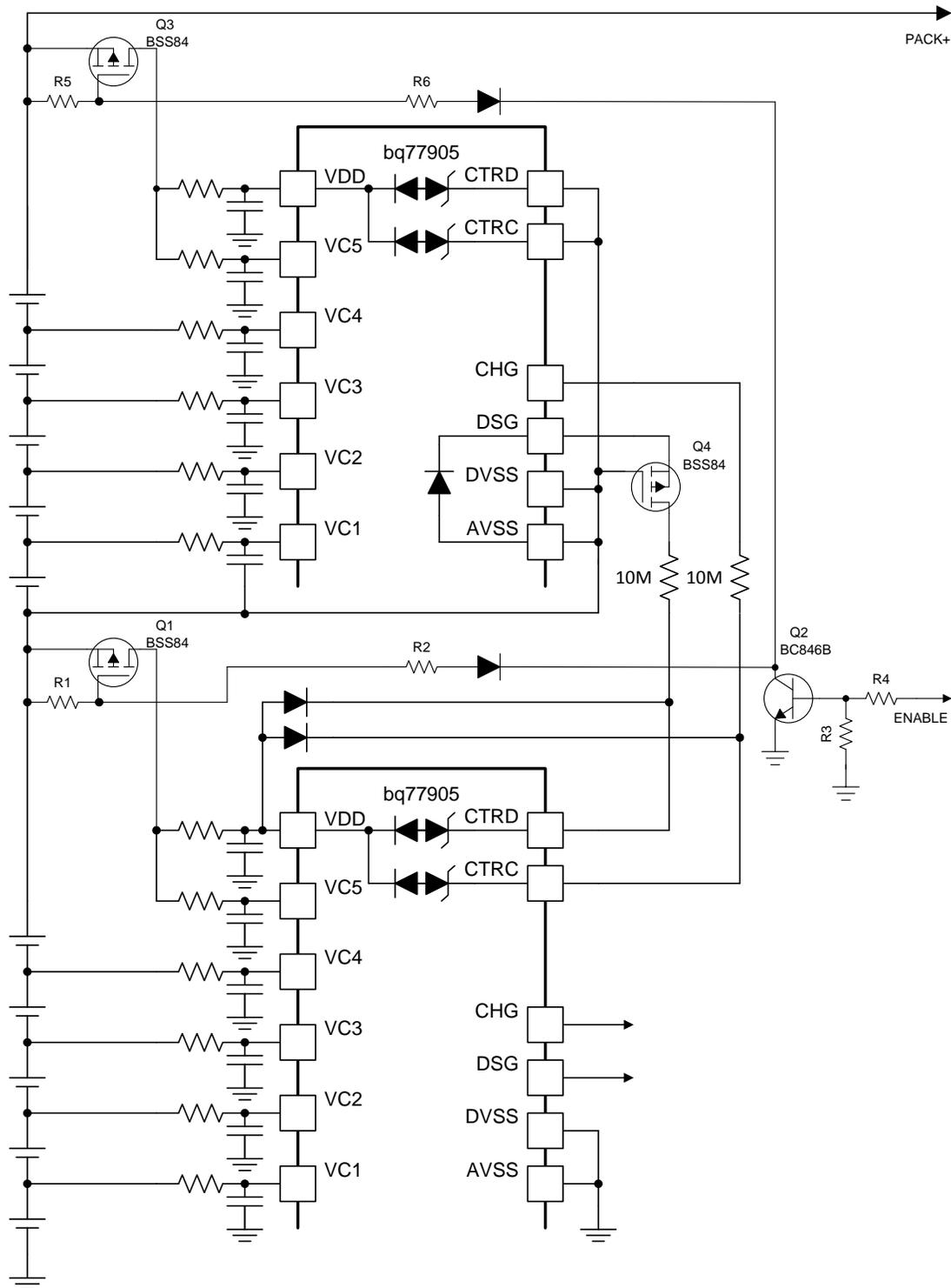
Figure 8 shows a circuit proposal to allow shutdown of stacked devices avoiding the leakage into CTRC and CTRD. A specification concern may exist for some user's since the maximum  $V_{CTR(DIS)}$  for the stacking input is 0.7 V while the maximum  $V_{(FETOFF)}$  is 0.5 V. This apparently provides little margin, however CHG is not held at the maximum and is allowed to fall below VSS. The designer should satisfy themselves the circuit will work in their application before implementing this design.



Copyright © 2017, Texas Instruments Incorporated

Figure 8. Stacked Device Shutdown Circuit

Figure 9 shows a test circuit which implements switches for both upper and lower devices and the proposal to prevent pullup through the CTRC and CTRD pins. The pack is enabled when ENABLE is connected to PACK+. R5 and R6 provide a load on the entire battery while R1 and R2 load only the lower cells. A compensating load could be added from Q3 drain to the upper VSS, but was not implemented in this circuit. Other switch configurations could be implemented, use appropriate transient protection for a system design.



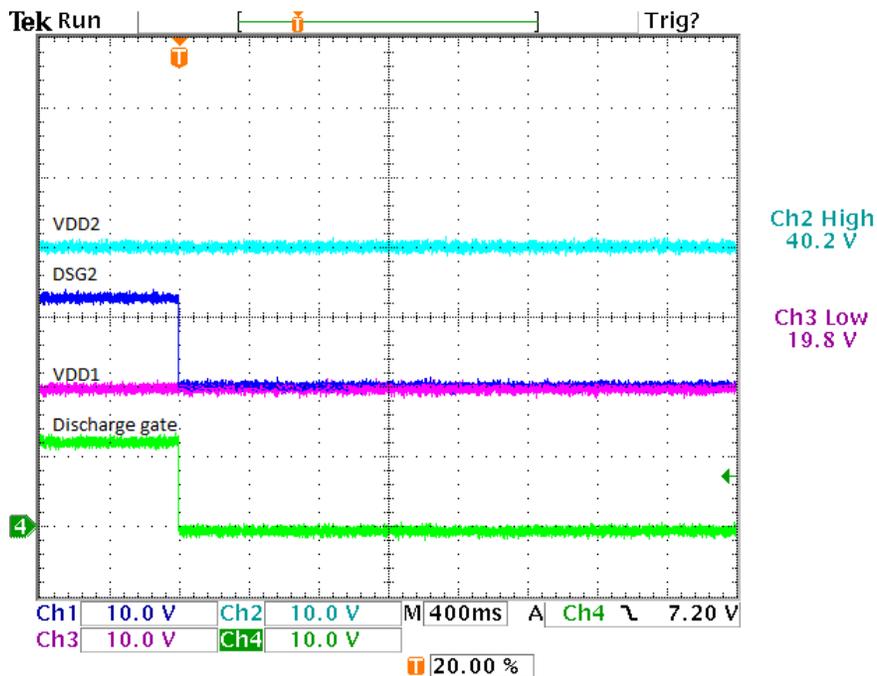
Copyright © 2017, Texas Instruments Incorporated

Figure 9. Stacked Switch Example Test Circuit

The circuit was tested with the component values shown in Table 3. With the circuit enabled, the circuit operates as expected. Figure 10 shows the operation of the FET controls in response to an overtemperature on the top device. When the upper device CHG and DSG are off, CTRC and CTRD of the lower device are held near the VDD level and the lower DSG and CHG turn off.

**Table 3. Stacked Switch Circuit Component Values**

Reference Designator	Value ( $\Omega$ )
R1	510 k
R2	510 k
R3	5.1 k
R4	62 k
R5	510 k
R6	1.5 M
(diodes)	1N4148 type



**Figure 10. Overtemperature Fault on Top Device**

Figure 11 shows the response when ENABLE is disconnected from PACK+. Like the single device, the discharge gate voltage drops as VDD1 falls. The upper device VDD falls to the cell 5 level. VDD1, the lower device VDD falls toward VSS. Without the leakage into CTRC and CTRD, VDD1 continues to fall slowly after the device enters shutdown. The load on the bottom 5 cells which cause voltage variation of VDD1 shown in Figure 7 is not present with this circuit.

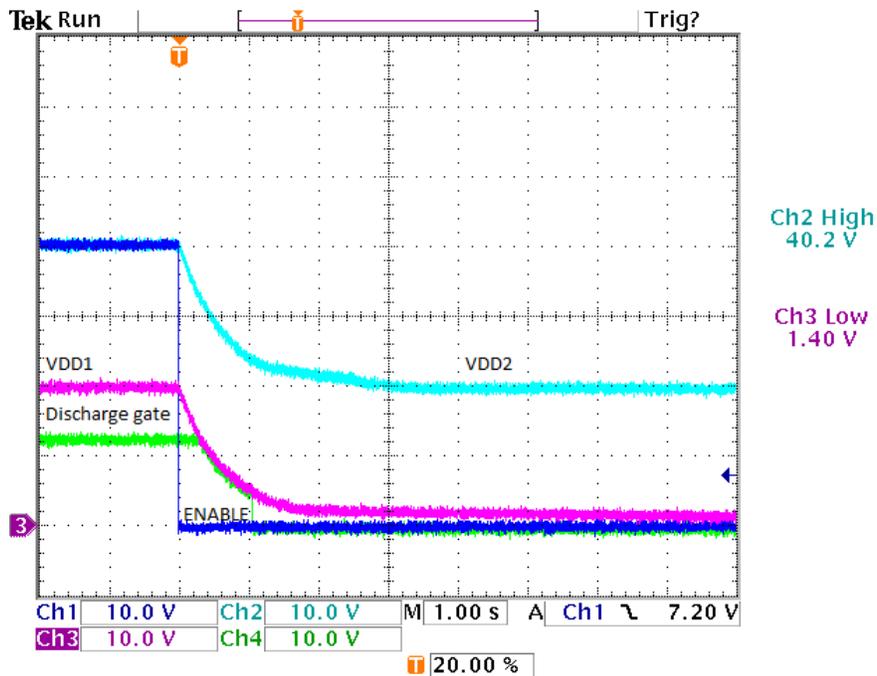


Figure 11. Stacked Devices Turn Off Using Test Circuit

#### 4 References

For additional information, refer to the following documents available at [www.ti.com](http://www.ti.com).

- Texas Instruments, [bq77905, bq77904 3-5S Ultra Low-Power Voltage, Current, Temperature, and Open Wire Stackable Lithium-ion Battery Protector Data Sheet](#)
- Texas Instruments, [bq77905 3-5S Low-Power Protector Evaluation Module User's Guide](#)
- Texas Instruments, ([bq77905 20S Cell Stacking Configuration Application Report](#))

## IMPORTANT NOTICE FOR TI DESIGN INFORMATION AND RESOURCES

Texas Instruments Incorporated ("TI") technical, application or other design advice, services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using any particular TI Resource in any way, you (individually or, if you are acting on behalf of a company, your company) agree to use it solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources.

You understand and agree that you remain responsible for using your independent analysis, evaluation and judgment in designing your applications and that you have full and exclusive responsibility to assure the safety of your applications and compliance of your applications (and of all TI products used in or for your applications) with all applicable regulations, laws and other applicable requirements. You represent that, with respect to your applications, you have all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. You agree that prior to using or distributing any applications that include TI products, you will thoroughly test such applications and the functionality of such TI products as used in such applications. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

You are authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING TI RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY YOU AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

You agree to fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of your non-compliance with the terms and provisions of this Notice.

This Notice applies to TI Resources. Additional terms apply to the use and purchase of certain types of materials, TI products and services. These include; without limitation, TI's standard terms for semiconductor products (<http://www.ti.com/sc/docs/stdterms.htm>), [evaluation modules](#), and [samples](http://www.ti.com/sc/docs/sampterm.htm) (<http://www.ti.com/sc/docs/sampterm.htm>).

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2017, Texas Instruments Incorporated