Application Report
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Magnetic Immune SMPS for Single-Phase LPRF Smart Meter

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ABSTRACT

This application note includes details to design a 12 V at 120 mA, 5 V at 100 mA, and 7.5 V at 40 mA output power supply using the UCC28880 with a 700-V integrated MOSFET from TI.

This design shows the high power density and simplicity that is possible because of the high level of integration while still providing exceptional performance. The document contains the power supply specification, schematic, bill of materials, transformer design, printed circuit board, performance data, and component selection.

Contents

List of Figures

List of Tables

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1 Electrical Requirements

Table 1 lists the electrical requirements.

Table 1. Electrical Requirements

	Description	MIN	TYP	MAX	Unit
$V_{IN(RMS)}$	Input voltage	90	240	480	VAC
F_{line}	Frequency	47	50	64	Hz
OUTPUT					
V_{OUT1}	Output voltage 1	0	5	5.02	V
I_{OUT1}	Output current 1	8		100	mA
V_{OUT2}	Output voltage 2	0	12	14	V
I_{OUT2}	Output current 2	5		120	mA
V_{OUT3}	Output voltage 3	0	7.5	8	V
I_{OUT3}	Output current 3	0		40	mA
P_{OUT}	Total output power (90 V to 480 V)	0	2.25	2.5	W

2 Schematic

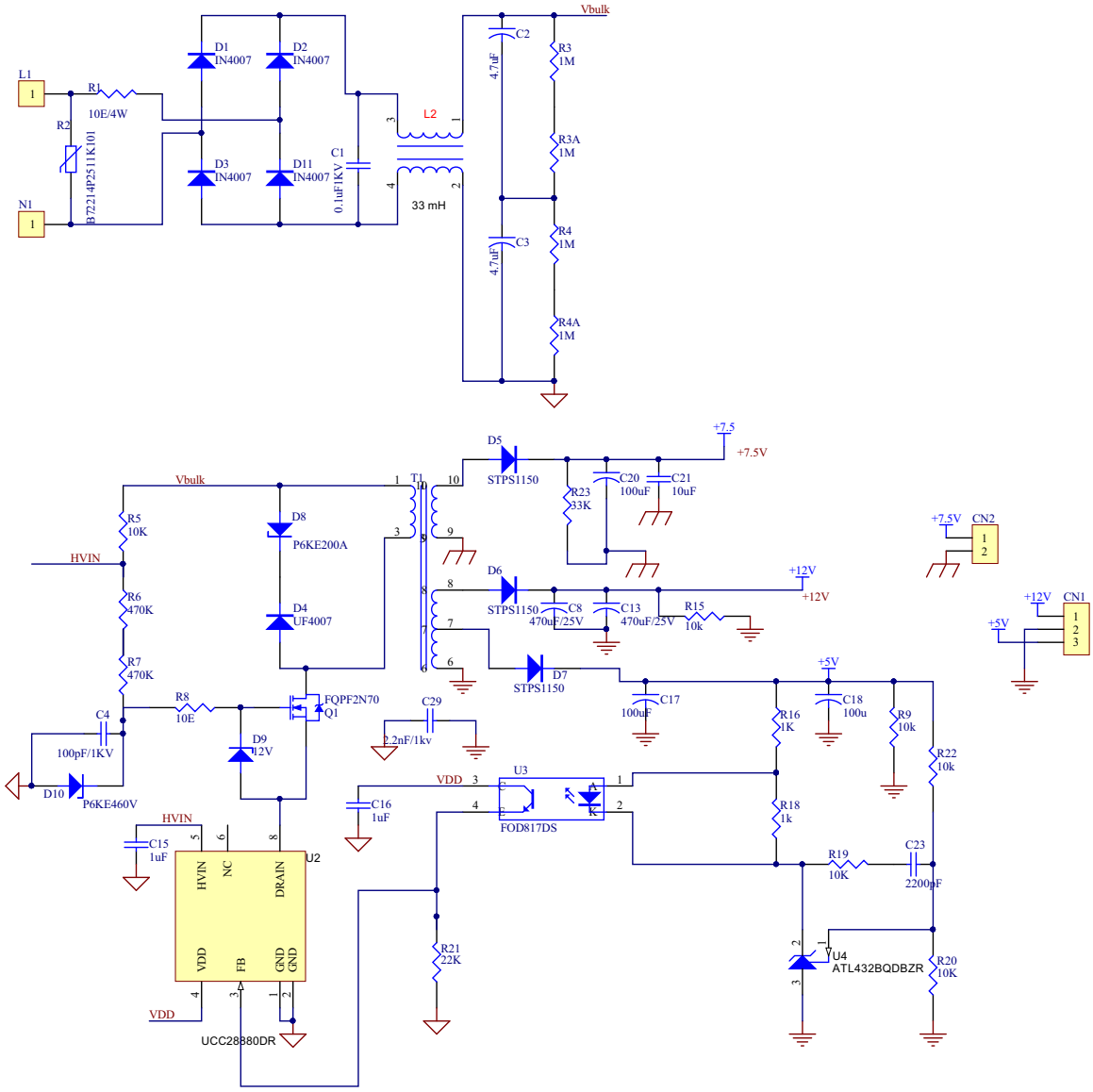

Figure 1. UCC28880 Schematic

3 Component Selection and Design Explanation

3.1 MOV (R2)

A 510-VAC MOV is used at the input. A 3-phase input in India can go as high as 500-VAC in rural areas. As a result, the input of the MOV is rated up to 510-VAC (B72214P2511K101 is the part used for MOV).

The MOV is used to pass the IEC 61000-4-5 specification. Users must rate the MOV such that it has a standoff voltage equal to voltage that can be continuous expected at the input of the circuit. Any voltage transient above this rating shall be clamped by this MOV.

3.2 Input Filter (L2 and C1)

A CMC of 33 mH is used in this design, and the leakage inductance of the CMC is around 1%. The leakage inductance of this CMC acts as a differential filter along with C1. This introduces an inductance of 0.33 mH to the input circuit. C1 is used in this design to act as an LC filter to attenuate differential noise. This LC combination helps to meet conducted emissions standard CISPR 14.

3.3 Series Fuse (R1)

A failure of the input circuitry can result in a complete short of the AC main supply, which might result in fire hazard and damage to the board beyond repair. This design uses a 10-Ω fusible resistor. The fusible resistor has two purposes: in case of a short circuit of the input MOSFET, the input resistor fuses and breaks the circuit, preventing any further damage. The resistor also limits the input current to the circuit in case of transient or inrush current peak.

The maximum peak current at the primary side is approximately 200 mA, hence a 10-Ω resistor will have a maximum peak heating of 0.4 W. This design uses a 2-W, fusible, 10-Ω resistor in the circuit.

3.4 Input Bulk Capacitor (C2 and C3)

After the full bridge rectification, the AC is rectified into pulsating DC. The peak of this pulsating DC can go up to V_{RMS} × 1.414 . Figure 2 shows the waveforms of the input pulsating DC.

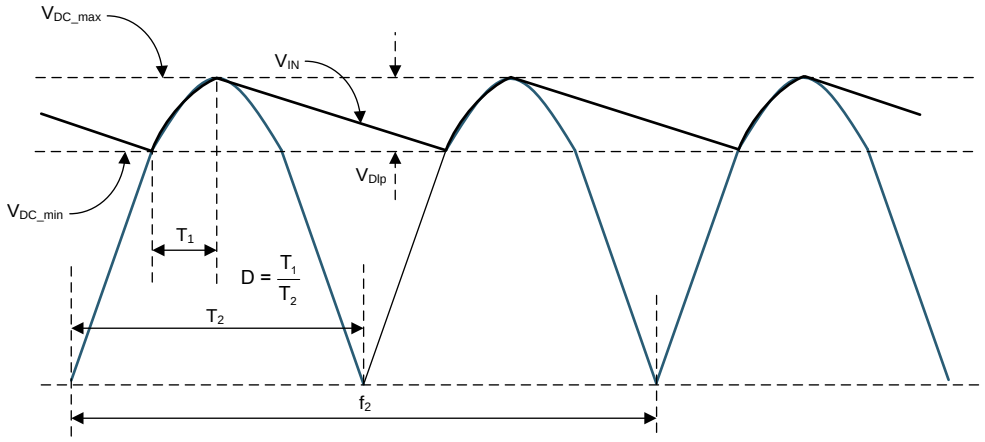

Figure 2. AC Rectified Waveform

Bulk capacitors are attached at Vbulk node to provide the peak current during the ON time of the MOSFET. Also, these bulk capacitors act as filters for the pulsating DC coming from the full bridge rectifier, enabling the primary of the circuit to set up near DC voltage.

Because the input AC voltage (input to the circuit) is rated up to 480-VAC RMS, the Vbulk voltage can go up to 480 × 1.414 = 680 V. As a result, the capacitors connected on these nodes must be rated for up to 800 to 900 V, considering the derating with temperature and time.

Because a single capacitor with such a high voltage rating is of high form factor, this design uses two series capacitor of equal value such that the voltage stress on each of them becomes half.

Every watt of power on the output requires approximately 1 µF to 2 µF on the Vbulk. The output power rating is 2.25 W, so a 2.2-µF capacitor is required on the Vbulk. Use 2 × 4.7 µF of 450 V on the input; this results in a net capacitance of around 2.35 µF capable of handling DC voltages up to 900 V.

3.5 MOSFET Voltage Rating (Q1)

The voltage stress in a flyback configuration on the primary MOSFET = V_{BULK} + V_{OUT} × Np / Ns + overshoot (due to parasitics).

[NP = number of turns primary; NS = number of turns secondary]

There are two ways to snub the overshoot in the primary side MOSFET:

- Zener + diode
- RC + diode

This design uses a less efficient, more cost-optimized approach of using a Zener clamp (D8 and D4).

Now with Zener clamp being used the Peak voltage stress on the MOSFET shall be equal to V_{BULK} + $V_{zenerclamp}$.

However, care must be taken so:

Zener clamp voltage > (Output voltage × Np / Ns) (1)

Failure to follow Equation 1 results in loss of power transfer during the off time.

In this case, the output is 5 V and the turns ratio is 15. As a result, the Zener clamp voltage must be at least greater than 75 V.

Assuming a 100-V Zener clamp is used, input stress voltage on the MOSFET is:

480 × 1.414 + 137 = 820 V (2)

(The 100-V clamping voltage of the Zener clamp can go as high as 137 V, hence using 137 V in Equation 2.)

Now the UCC28880 has only a 700-V MOSFET integrated in it, so this design uses a cascoded MOSFET based architecture. In a cascoded MOSFET architecture there are two MOSFETs in the series path of the primary side (see Figure 3).

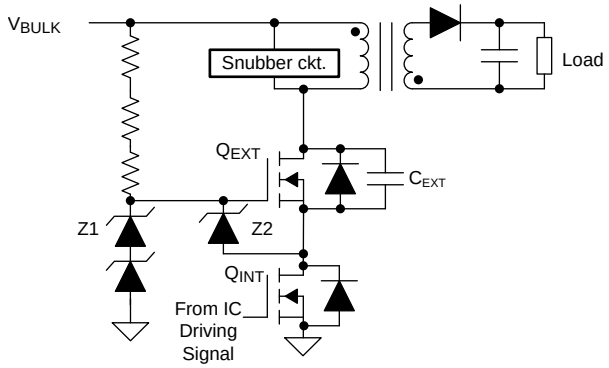

Figure 3. Cascode Architecture

At bulk voltages below the Z1 voltages the C_{EXT} is always diode connected, meaning that it is always on as its gate is tied to the drain. Hence, the MOSFET is diode shorted and will always have a voltage on the source = V_{BULK} – Vth (provided V_{BULK} < Z1).

As soon as the V_{BULK} goes above the Z1 clamp voltage, the gate of this MOSFET gets clamped to Z1 voltage, ensuring that under no condition shall the source be allowed to go above V_{Z1} – Vth. Hence, the MOSFET acts like an LDO (source follower) at V_{BULK} > V_{Z1} voltage. Any additional voltage on V_{BULK} beyond V_{Z1} is dropped across the external MOSFET.

The UCC28880 has a 700-V MOSFET, hence users must ensure that the MOSFET inside the UCC28880 is not exposed to a voltage of more than 700 V at any condition.

A Zener of 480-V (P6KE480A [D10]) is used. From the data sheet, users can see the P6KE480A can go to a maximum of up to 658 V. Hence, the source of the external MOSFET can go up to a maximum of 655 V. (The threshold voltage of the external MOSFET is taken as 3 V here.)

Now any additional voltage of the drain of the external MOSFET above 655 V is dropped across the upper external MOSFET (Q1).

Based on Equation 2, the maximum stress can go up to 820 V. Theoretically, a 200-V MOSFET is required.

As the voltage across the external MOSFET can go up to 820 V – 655 V = 165 V.

MOSFETs are very inexpensive in the voltage range of 700 V, so a 700-V MOSFET was chosen (FQPF2N70: Q_{EXT}).

Now with a 700-V MOSFET the design of the Snubber is more relaxed because the net voltage handling capability of the cascaded configuration = 700 V + 700 V = 1400 V .

P6KE200 (D8) was used for the snubber because there is now more margin.

With a 200-V Zener used in the snubber, the net voltage on the cascoded MOSFET can go as high as 480 × 1.414 + 274 = 950 V (a 200-V Zener can clamp at a voltage as high as 274 V).

Because an external MOSFET with a voltage rating of 700 V was used, there is a sufficient margin to accommodate the increases in voltage stress level on the primary MOSFET.

The maximum stress on external MOSFET = 950 V – 480 V = 470 V, which much below its rating.

The maximum stress on the UCC28880 internal MOSFET = clamping voltage of Z1 = 658 V.

The above optimization helps to decrease the losses at the snubber, which improves efficiency.

3.6 Secondary Diodes (D5, D6, D7)

The reverse voltage stress on the secondary side diode = V_{IN_MAX} × Ns / Np + V_{OUT}

V_{IN_MAX} = 480 × 1.414 = 680 V

Hence the reverse peak voltage on the secondary diode = 680 / 15 + 5 ≈ 60 V. A 150-V, 1-A Schottky diode was used (STPS1150). This is the highest stress on the O/P side, hence rating a diode to this can be sufficient and the same diode can be used on all other rails.

Schottky diodes are used for lower power losses on the diode.

3.7 Secondary Side Regulation

ATL432 (U4) was used as an error amplifier to transfer the feedback signal through an opto from the secondary side to primary side.

Because the wireless module is likely to be powered directly from the 5-V supply, good load regulation on this rail is required. Hence a secondary side regulation (SSR) based controller is recommended.

The opto coupler U3 (FOD817) used is 5 kV_{RMS} isolated.

In Table 4 and Table 5, users can see the voltage variation due to load is less than a couple of mV from no load to full load .

3.8 Output Capacitor (C17 and C18)

The output capacitors are designed to handle the transient load and the reduce the ripple voltage. As a DCM operation with less than 50% duty cycle there is no right half plane zero, hence the initial transient load is provided by the output capacitors before the loop bandwidth kicks in to provide the additional current.

There are a number of important factors when specifying the output capacitors:

- Capacitance value
- Ripple current
- Low ESR
- Temperature of operation (85°C or 105°C)
- Lifetime
- Voltage rating

3.9 Transformer (T1) Specification Sheet and Calculations

3.9.1 Step 1: Calculate the Turns Ratio

$$V_{IN\_MIN} = 90\ VAC \times 1.414 = 128\ VDC \quad (3)$$

Assuming the maximum duty cycle to be 45%:

$$T_{ON} / T_{OFF} = 0.45 / 0.55 \quad (4)$$

$$V_{MIN} \times T_{ON} = Np / Ns \times (V_{OUT} + V_f) \times T_{OFF}$$

(Applying Volt-Second) (5)

Because the 5-V rail will be regulated, V_{OUT} = 5 V, and Np / Ns = 19.

However, a turns ratio of 15 is used because this helps reduce the maximum voltage stress on the primary switching MOSFET.

NOTE: Using a lower Nps than ideal may result in deeper DCM operation at maximum load and may result in lower efficiency. The UCC28880 might not reach its maximum allowable duty cycle and will always be working in deep DCM.

3.9.2 Step 2: Choose the Core and Core Size

The chosen core size is EE20 for the power requirement of 2.5 W. In this case a much smaller core size can be used. However, an Iron Powdered core, which is mainly available in EE20 size, was used.

The meter power supply in India must be immune to magnetic tamper; as a test of this condition, metering manufacturers usually install a hall effect sensor to detect magnetic tamper. However, just detection of magnetic tamper is not sufficient. The power supply must withstand and deliver the rated output under an influence of 500-mT permanent magnet. The powdered iron core has an operating flux of 800 mT to 1.2 mT (this proves to be important in case of magnetic field intervention).

The permeabilty B_{SAT} and the L of an inductor drops as soon as a magnet is brought in proximity. A typical ferrite core with a B_{SAT} value of 0.3 T shall saturate in this condition when a 500-mT magnet is brought close to the core. However, a powdered iron core with a B_{SAT} value of 1.2 T is able to sustain despite the magnet in its vicinity because 0.8 T(B_{SAT} of powdered iron core) – 0.5 T (the flux density of magnet) is still is able to result in an available operating flux of 0.3 T, saving the core from getting saturated.

A KE20-52A core was used. Users can find the data sheet at KDM. The AL value of this core is 73. With this AL in mind, the number of turns was chosen in accordance with the required inductance value (see Equation 6).

$$AL = nH / (turns^2)$$

- see Equation 9 to calculate L (6)

3.9.3 Transformer Design Calculation

The peak current flowing through the MOSFET is limited internally to 170 mA at 25°C and the maximum switching frequency allowed for the UCC28880 is 52 kHz, these constraints help to decide the value of the inductor.

For a P_{OUT} = 2.315 W, first calculate the required I_{PEAK} on the primary side:

$$P_{IN} = P_{OUT} / \text{Efficiency} = 2.9 \text{ W} \quad (7)$$

Because the device is operated in DCM with a 50% duty cycle as the maximum, the input peak can be calculated using .

$$I_{PEAK} = 2 \times P_{IN\_MAX} / (V_{DC\_MIN} \times D_{MAX})$$

$$(2 \times 2.9) / (128 \times 0.4) = 0.113 \text{ A} \quad (8)$$

where

- 80% efficiency is assumed

A peak of 0.113 A is approximately enough peak current, which is available at *UCC28880 700-V, 100-mA Low Quiescent Current Off-Line Converter*.

An inductor with at least 260 mA of allowed peak current at the least on time is required.

The on time is least at the highest switching frequency, 75 kHz (maximum limit).

$$V = L \times di / dt$$

$$L = V_{DC\_MIN} \times D_{MAX} / (I_{PEAK} \times Fsw)$$

$$L = 2.9 \text{ mH} \quad (9)$$

The L value found in Equation 9 is the maximum allowed L for the UCC28880 to be in discontinuous mode of operation.

An L of approximately 2.4 mH is chosen to make sure the winding fits in an EE20 core transformer (the most popular core in the metering industry).

4 Transformer Construction Details

Table 2. Core and Bobbin Details

Core Type	Core Material	Bobbin	Isolation Voltage	Quantity	Primary Inductance
KE20-26 (EE 20)	Iron powdered core	10 pin (horizontal)	3000 VAC	1	2400 µH ±5%

Table 3. Winding Details

Winding	Number of Turns	Wire Gauge	Start Pin	End Pin	Inductance
W1	90	33 AWG	3	2	
W3	12	30 AWG	7	6	
W4	18	30 AWG	8	7	
W2	90	33 AWG	2	1	
W5	18	32 AWG	10	9	

4.1 Insulation Requirements

The primary inductance shall be 2400 µH ±5% (between Pin 3 and Pin 1).

- Insulation voltage: between [W1, W2] and [W3, W4] → 1000 V for one minute.
- Insulation voltage: between [W1, W2 (shorted together)] and W5 → 3000 VAC for one minute.
- Insulation voltage: between [W3, W4 and W5] → 3000 VAC for one minute.

5 Winding Procedure

1. Start with half primary 90 turns (W1) starting at Pin 3 and end at Pin 2.
2. Supplementary insulation.
3. Secondary 1 (W3) 12 turns spreading uniformly across bobbin width, start at Pin 7 and end at Pin 6.
4. Basic insulation.
5. Secondary 2 (W4) 18 turns spreading uniformly across bobbin width, start at Pin 8 and end at Pin 7
6. Basic insulation.
7. Wind rest of half primary 90 turns (W2) start at Pin 2 and end at Pin 1.
8. Reinforced insulation.
9. Wind bias (W5) 18 turns starting at Pin 10 and ending at Pin 9 in one layer spreading uniformly across the bobbin.
10. Reinforced insulation.
11. Put core and measure the primary inductance between Pin 1 and Pin 3.
12. Vacuum impregnate with varnish

6 Load Efficiency, Line Regulation, and Thermal Performance

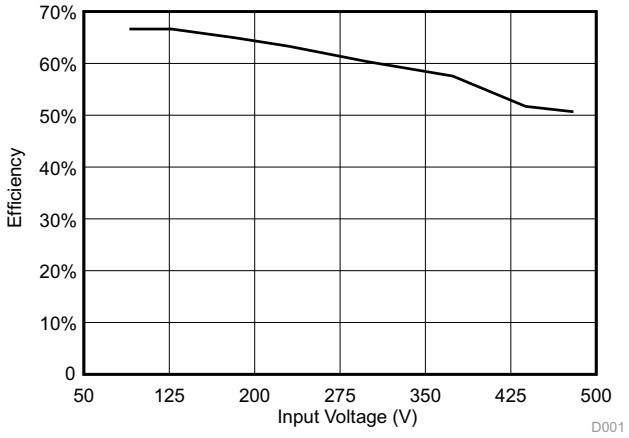

Figure 4. Full Load Efficiency vs Line Voltage

Table 4. Line Regulation (Full Load)

AC Input Voltage (V)	DC Vbulk (V)	O/P Volt at 12 V	I_{OUT} at 12 V in Amps	O/P Volt at 5 V in Volts	I_{OUT} at 5 V in Amps	Output Voltage on 7.5 V	Rload on 7.5 V in Ohms
90.5	128	13.3	0.128	4.95	0.1	8	200
127.3	180	13.3	0.128	4.94	0.1	8	200
183.9	260	13.3	0.128	4.94	0.1	8	200
232.0	328	13.3	0.128	4.94	0.1	7.9	200
300.6	425	13.2	0.128	4.93	0.1	7.9	200
374.8	530	13.2	0.128	4.93	0.1	7.9	200
438.5	620	13.2	0.128	4.93	0.1	7.9	200
480.9	680	13.1	0.128	4.92	0.1	7.9	200

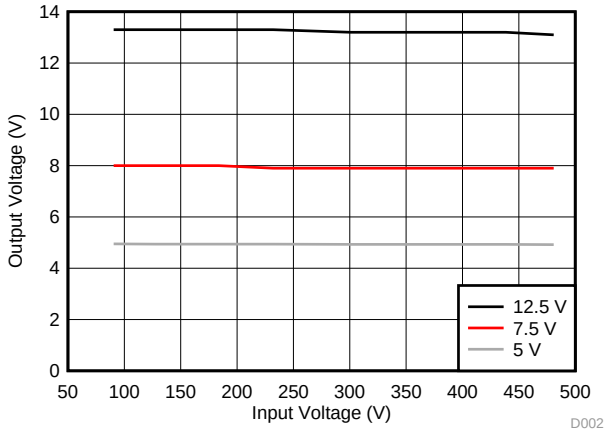

Figure 5. Line Regulation (Full Load)

Table 5. Full Load on 5 V and 5 mA on 12.5 V (Line Regulation)

AC Input Voltage (V)	Vbulk DC (V)	Output Voltage 12 V	I_{OUT} on 12 V in Amps	Output Voltage (5 V)	I_{OUT} at 5 V in Amps	Output Voltage on 7.5 V	Rload on 7.5 V in Ohms
90.5	128	14.4	0.005	4.95	0.1	8	200
127.3	180	14.4	0.005	4.94	0.1	8	200
183.9	260	14.5	0.005	4.94	0.1	8	200
232.0	328	14.5	0.005	4.94	0.1	7.9	200
300.6	425	14.5	0.005	4.93	0.1	7.9	200
374.8	530	14.5	0.005	4.93	0.1	7.9	200
438.5	620	14.5	0.005	4.93	0.1	7.9	200
480.9	680	14.5	0.005	4.92	0.1	7.9	200

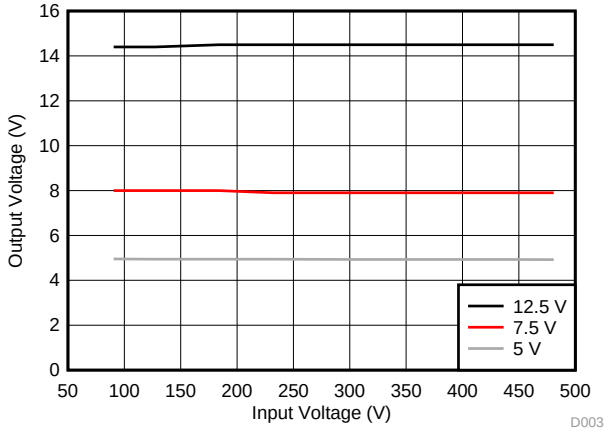

Figure 6. Full Load on 5 V and 5 mA on 12.5 V (Line Regulation)

Table 6. No Load on 5 V and 5 mA on 12.5 V (Line Regulation)

AC Input Voltage (V)	DC Vbulk (V)	Output Voltage 12 V	I_{OUT} on 12 V in Amps	Output Voltage on 5 V	I_{OUT} at 5 V in Amps	Output Voltage (7.5 V)	Rload on 7.8 in Ohms
90.5	128	10.1	0.005	4.95	0	6	200
127.3	180	9.4	0.005	4.94	0	5.6	200
183.9	260	9.1	0.005	4.94	0	5.3	200

Table 6. No Load on 5 V and 5 mA on 12.5 V (Line Regulation) (continued)

AC Input Voltage (V)	DC Vbulk (V)	Output Voltage 12 V	I_{OUT} on 12 V in Amps	Output Voltage on 5 V	I_{OUT} at 5 V in Amps	Output Voltage (7.5 V)	Rload on 7.8 in Ohms
232.0	328	8.9	0.005	4.94	0	5.2	200
300.6	425	8.6	0.005	4.93	0	5.1	200
374.8	530	8.5	0.005	4.93	0	4.9	200
438.5	620	8.2	0.005	4.93	0	4.7	200
480.9	680	8	0.005	4.92	0	4.5	200

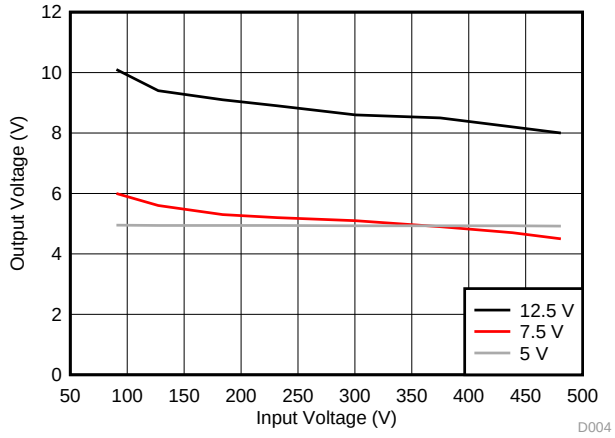

Figure 7. No Load on 5 V and 5 mA on 12.5 V (Line Regulation)

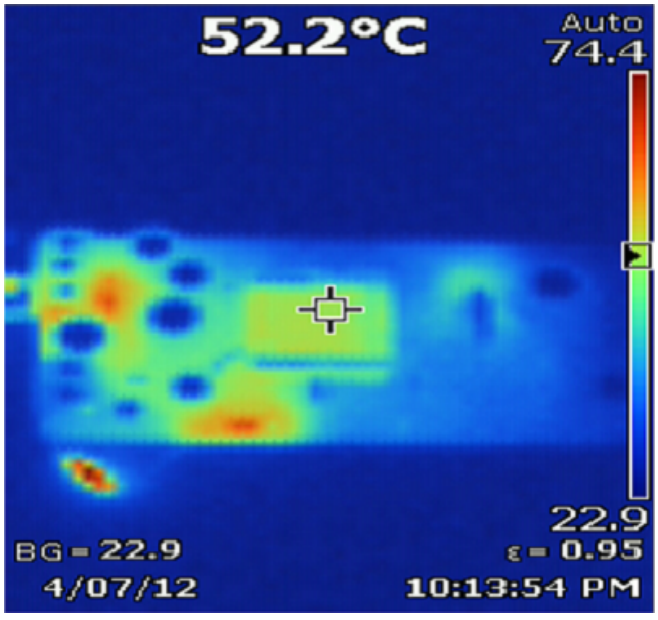

Figure 8. Thermal Performance: 240-VAC Full Load (Top)

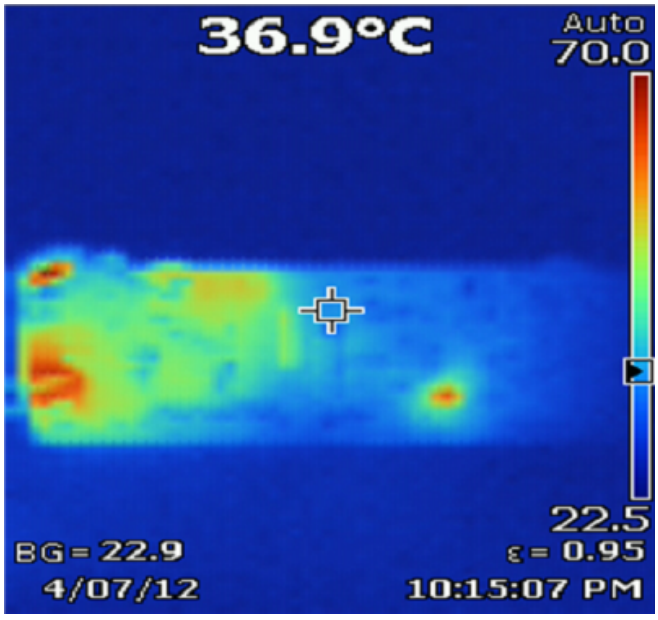

Figure 9. Thermal Performance: 240-VAC Full Load (Bottom)

7 Layout

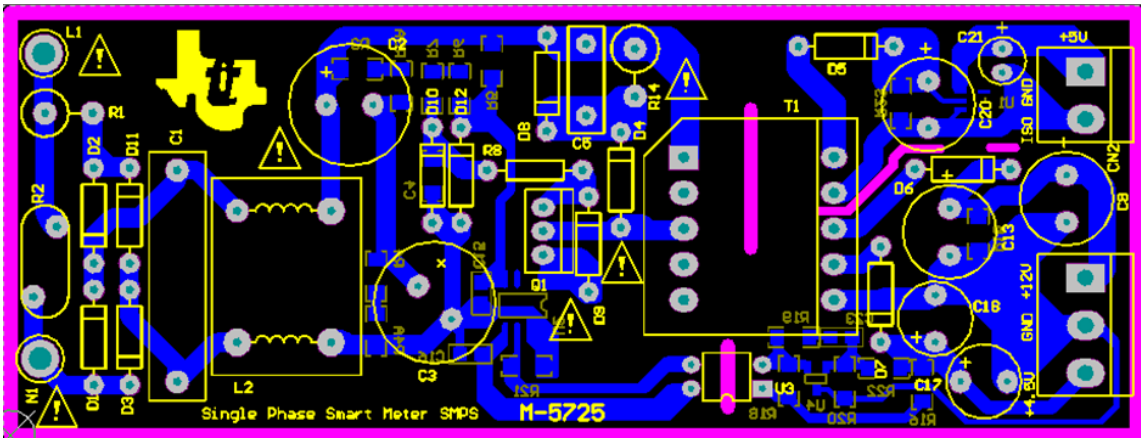

Figure 10. Layout (1 of 3)

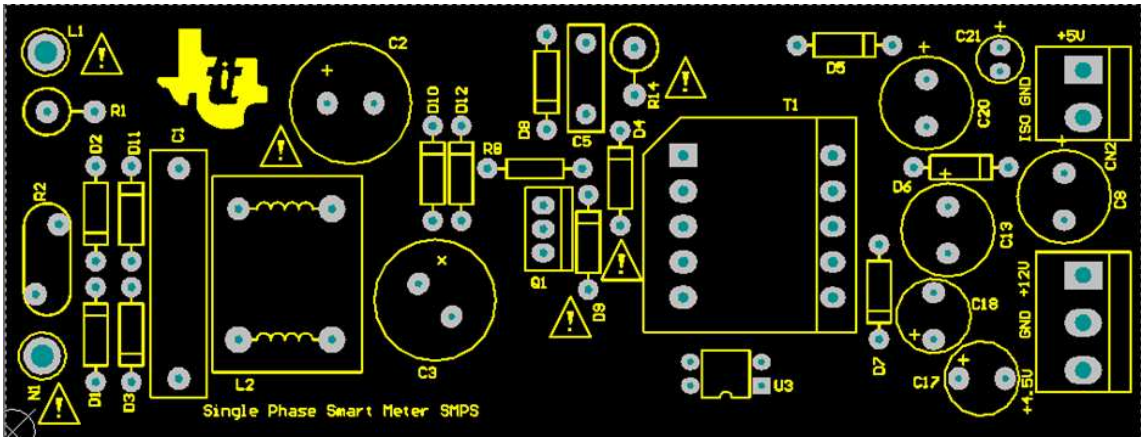

Figure 11. Layout (2 of 3)

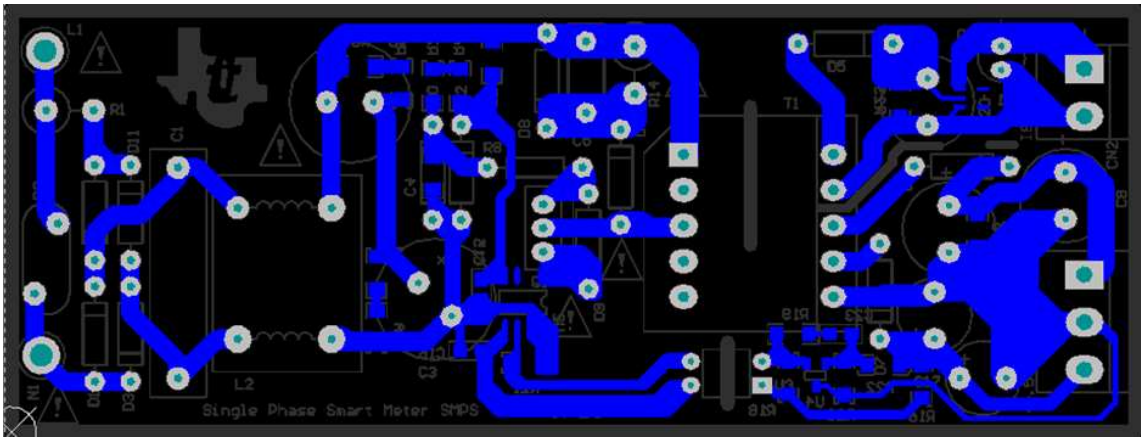

Figure 12. Layout (3 of 3)

8 Transient Loading

1-kΩ resistor added on 12 V and 5 V each; No load = 1 kΩ on 12 V and 5 V; Violet = 5 V (output); Green = 12 V (output); Yellow = transient drive waveform

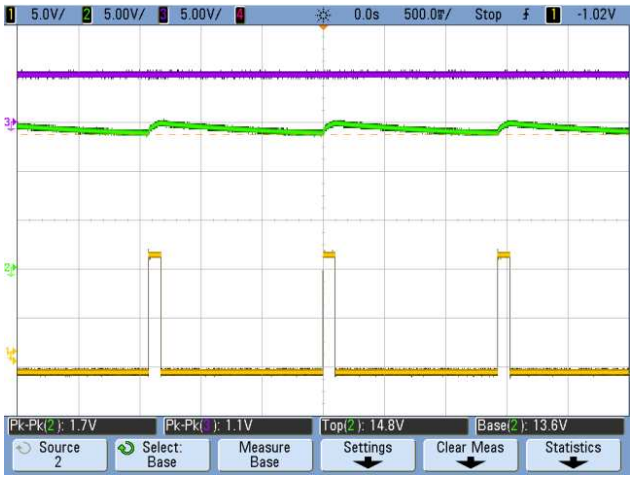

Figure 13. 90 VAC: No Load on 12-V Output, 5-V Load Transient

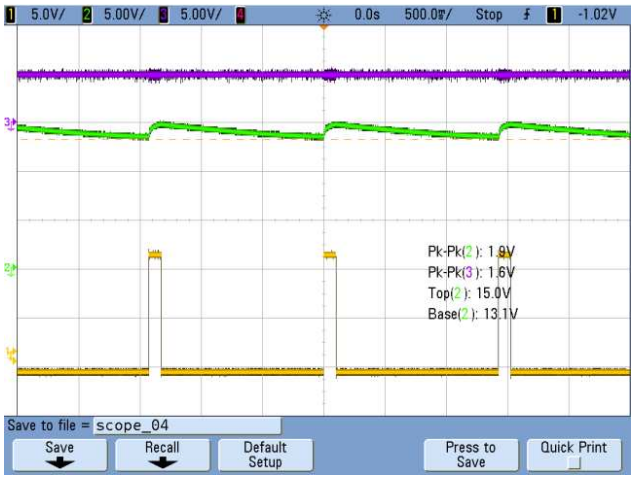

Figure 14. 480 VAC: No Load on 12 V, 5-V Load Transient

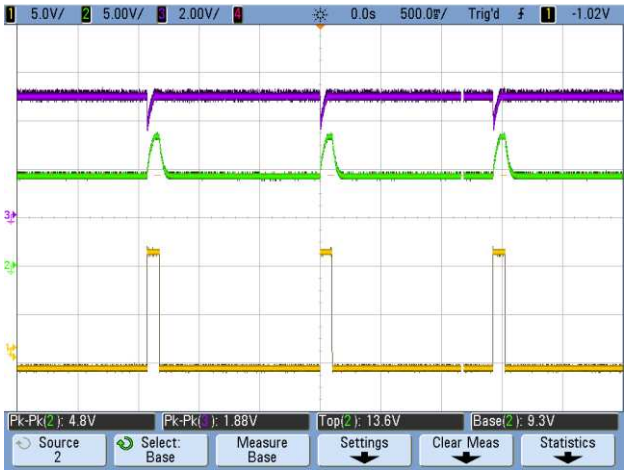

Figure 15. 90 VAC: Full Load on 12-V Output, 5-V Load Transient

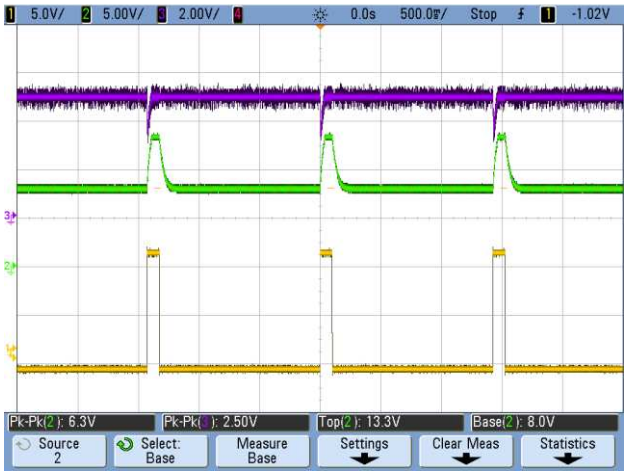

Figure 16. 480 VAC: Full Load on 12-V Output, 5-V Load Transient

1-kΩ resistor added on 12 V and 5 V each; No load = 1 kΩ on 12 V and 5 V; Violet = 5 V (output); Green = 12 V (output); Yellow = transient drive waveform

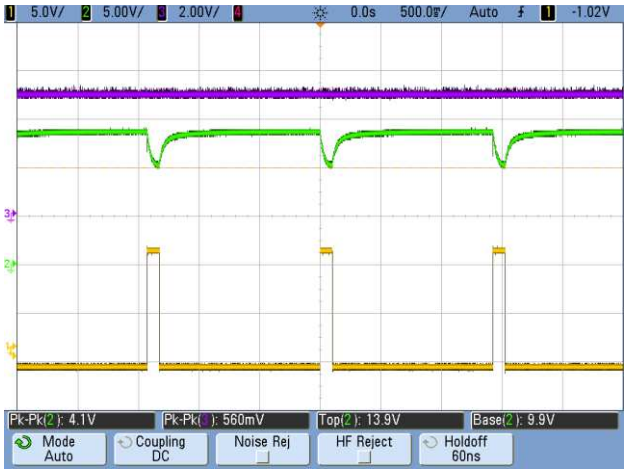

Figure 17. 90 VAC: No Load on 5-V Output, 12-V Load Transient

Figure 18. 480 VAC: No Load on 5-V Output, 12-V Load Transient

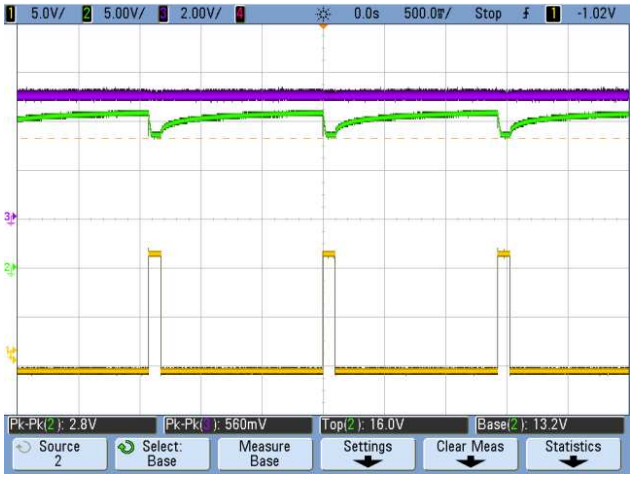

Figure 19. 90 VAC: Full Load on 5-V Output, 12-V Load Transient

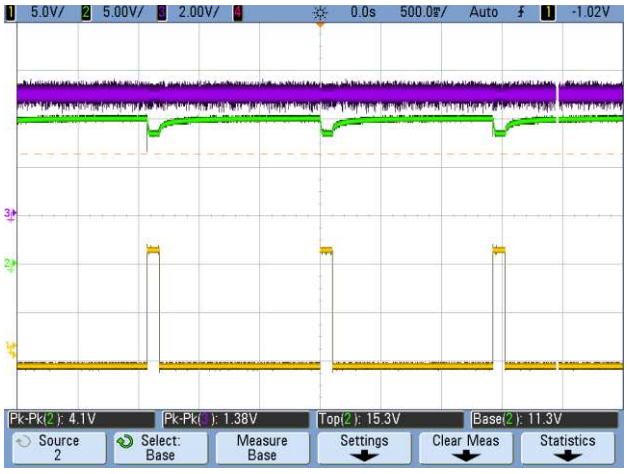

Figure 20. 480 VAC: Full Load at 5 V, 12-V Load Transient

9 Output Voltage During Start Up

Violet = 7.5 V (output); Yellow = 5 V (output); Green = 12 V (output)

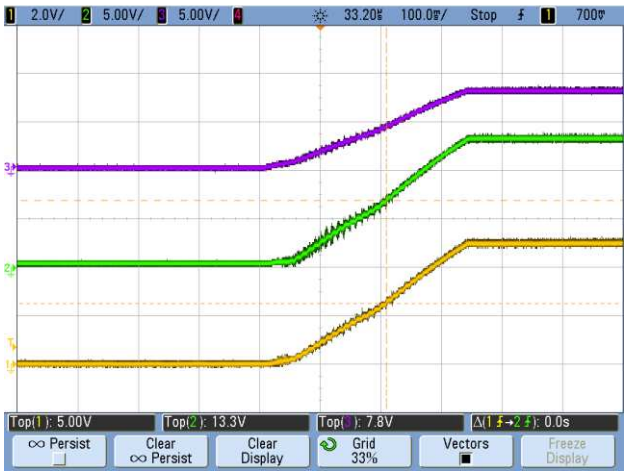

Figure 21. 90 VAC: Full Load Start Up

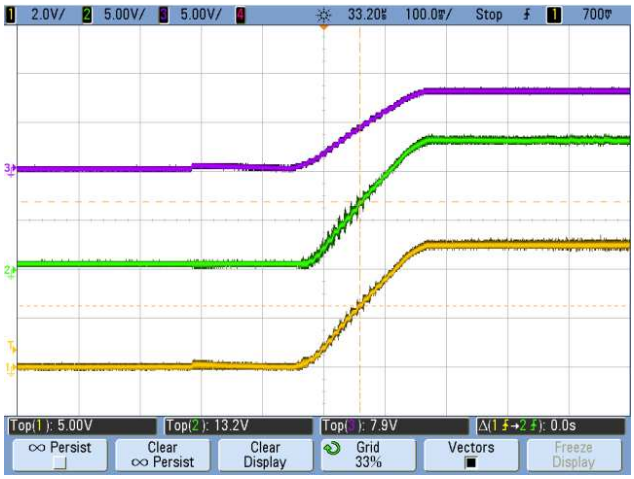

Figure 22. 230 VAC: Full Load Start Up

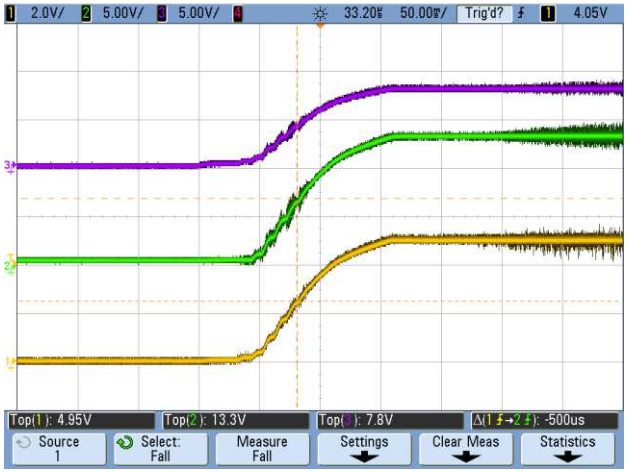

Figure 23. 480 VAC: Full Load Start Up

10 Switch Node Waveforms

Figure 24. 90-VAC Input: 90 No Load (Wide)

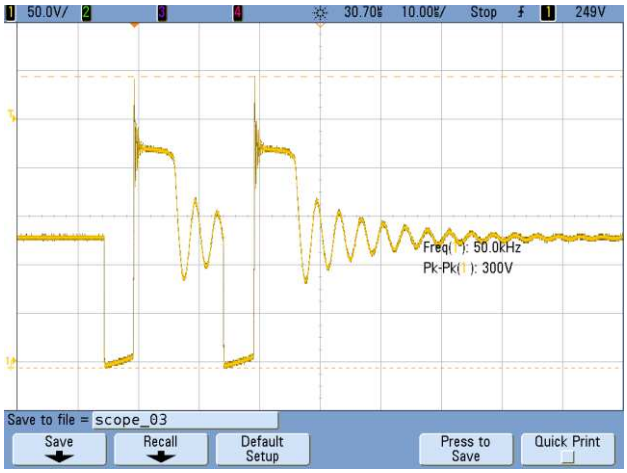

Figure 25. 90-VAC Input: 90 No Load (Zoom)

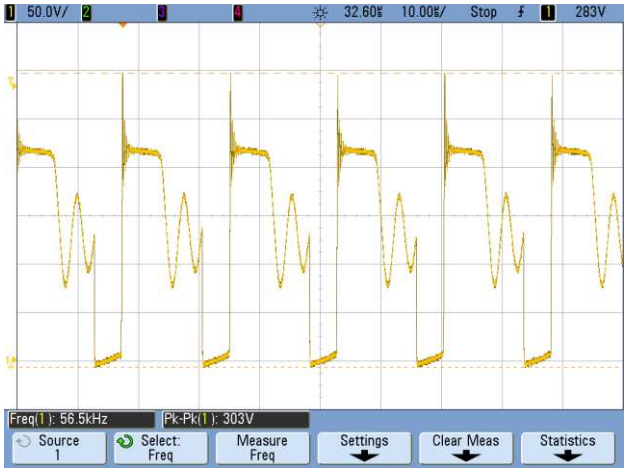

Figure 26. 90-VAC Input: 90 Full Load (Zoom)

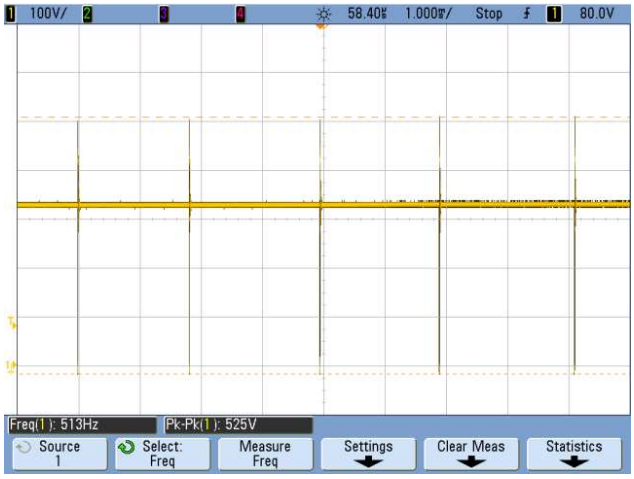

Figure 27. 240-VAC Input: 230 No Load (Wide)

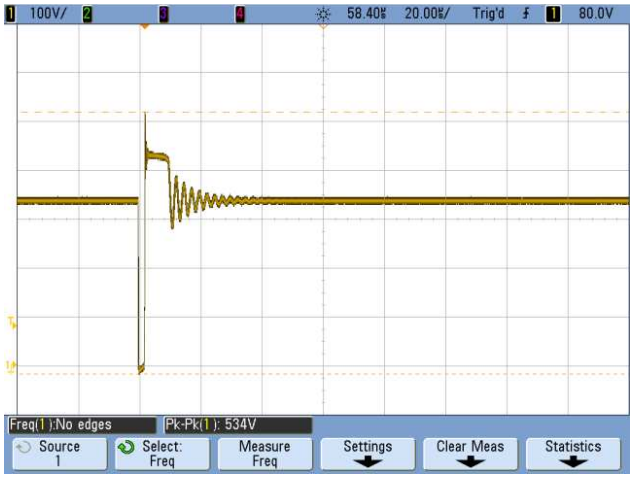

Figure 28. 240-VAC Input: 230 No Load (Zoom)

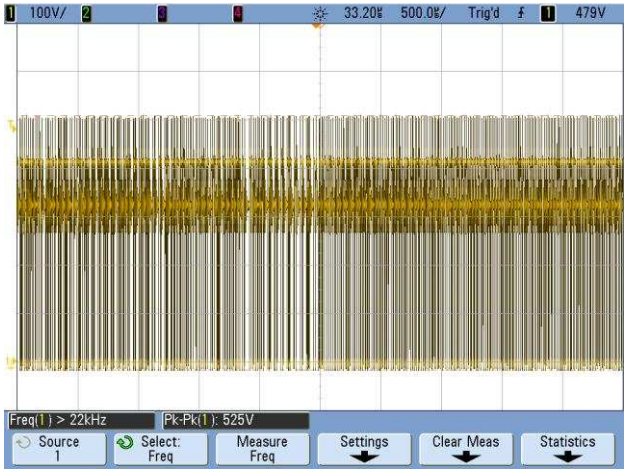

Figure 29. 240-VAC Input: 230 Full Load (Wide)

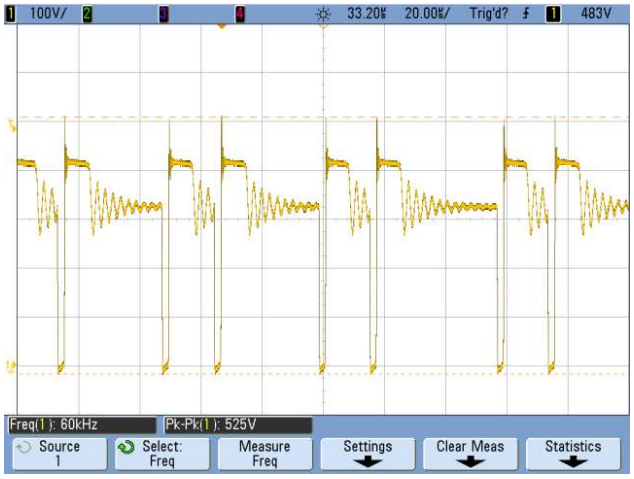

Figure 30. 240-VAC Input: 230 Full Load (Zoom)

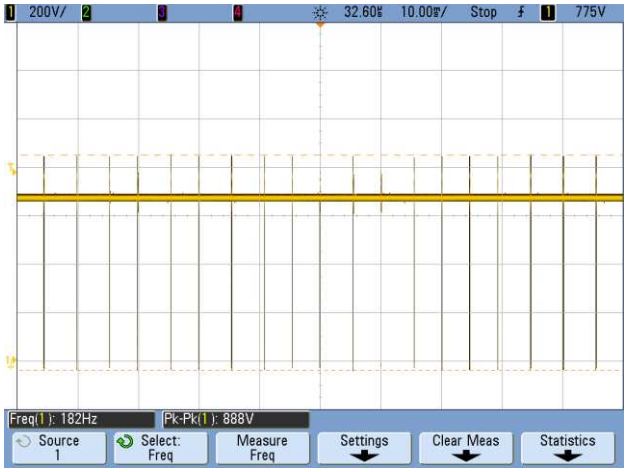

Figure 31. 480-VAC Input: 480 No Load (Wide)

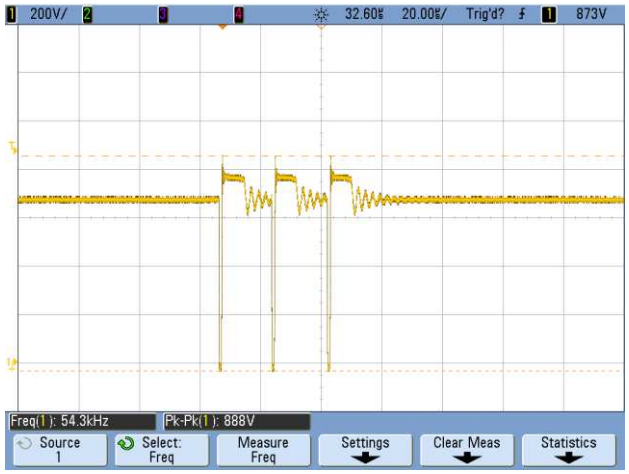

Figure 32. 480-VAC Input: 480 No Load (Zoom)

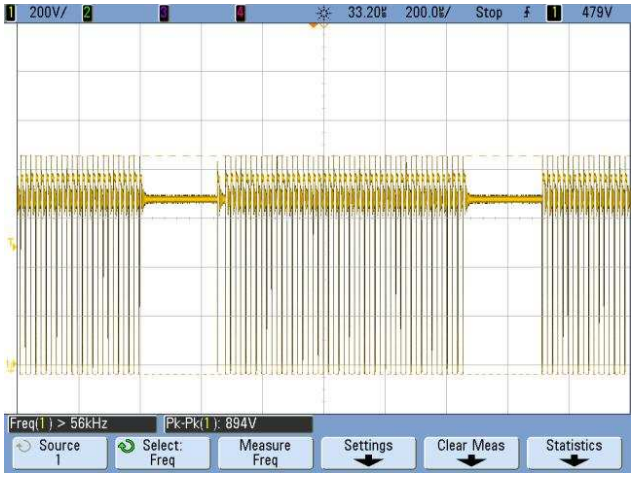

Figure 33. 480-VAC Input: 480 Full Load (Wide)

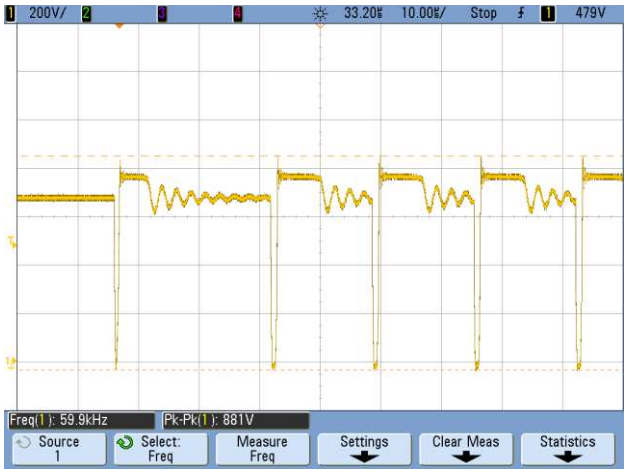

Figure 34. 480-VAC Input: 480 Full Load (Zoom)

11 Output Ripple Waveforms

Green = 12 V (output); Yellow = 5 V (output)

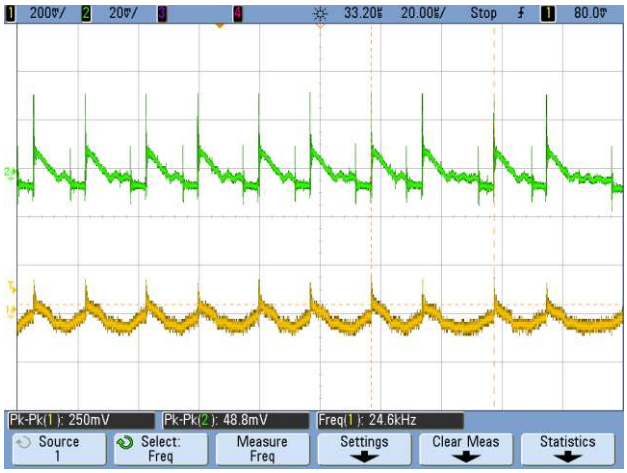

Figure 35. 90-V Full Load Output Ripple

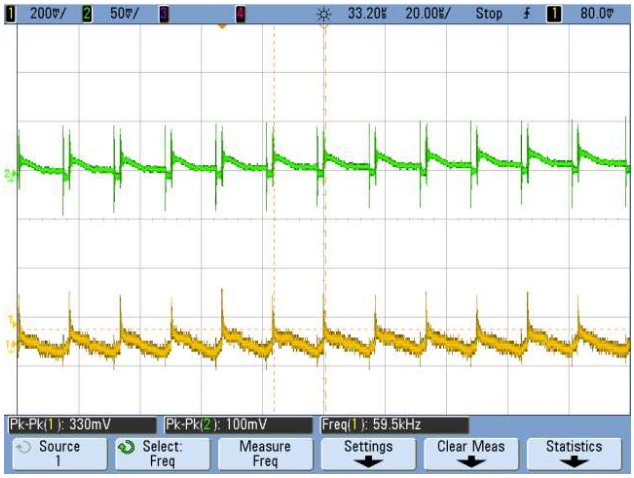

Figure 36. 230-V Full Load Output Ripple

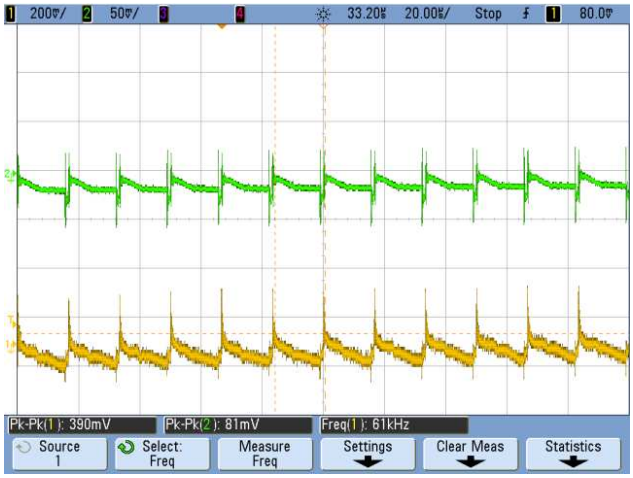

Figure 37. 480-V Full Load Output Ripple

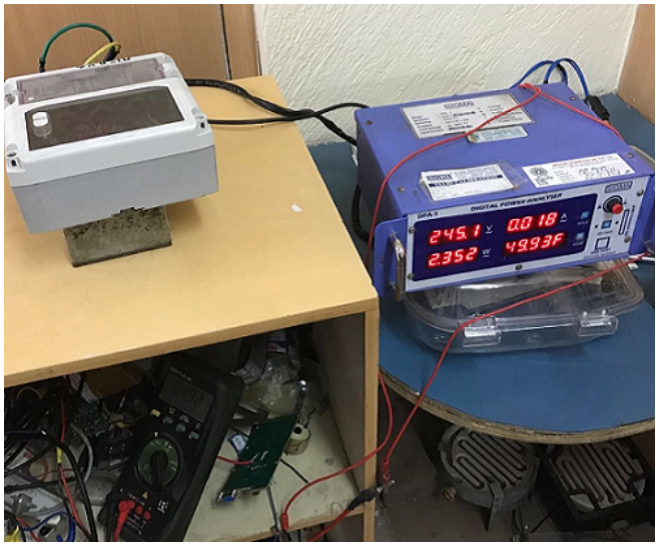

Figure 38. Magnet Immunity (1 of 6)

Figure 39. Magnet Immunity (2 of 6)

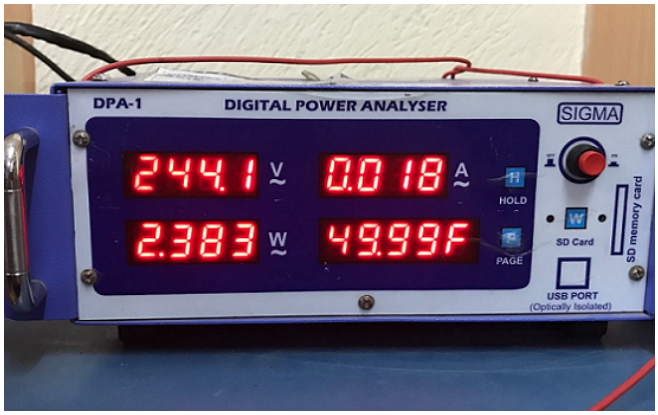

Figure 40. Magnet Immunity (3 of 6)

Figure 41. Magnet Immunity (4 of 6)

Figure 42. Magnet Immunity (5 of 6)

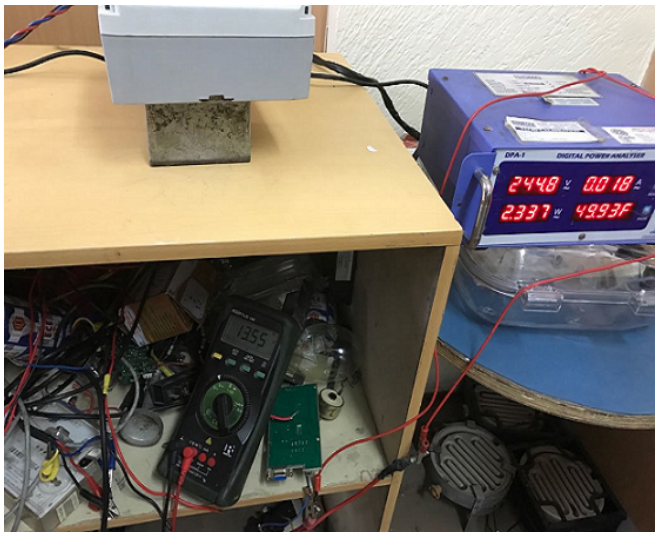

Figure 43. Magnet Immunity (6 of 6)

Figure 44. Conducted EMI Results

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Date	Revision	Description
February 2018	*	Initial Release

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