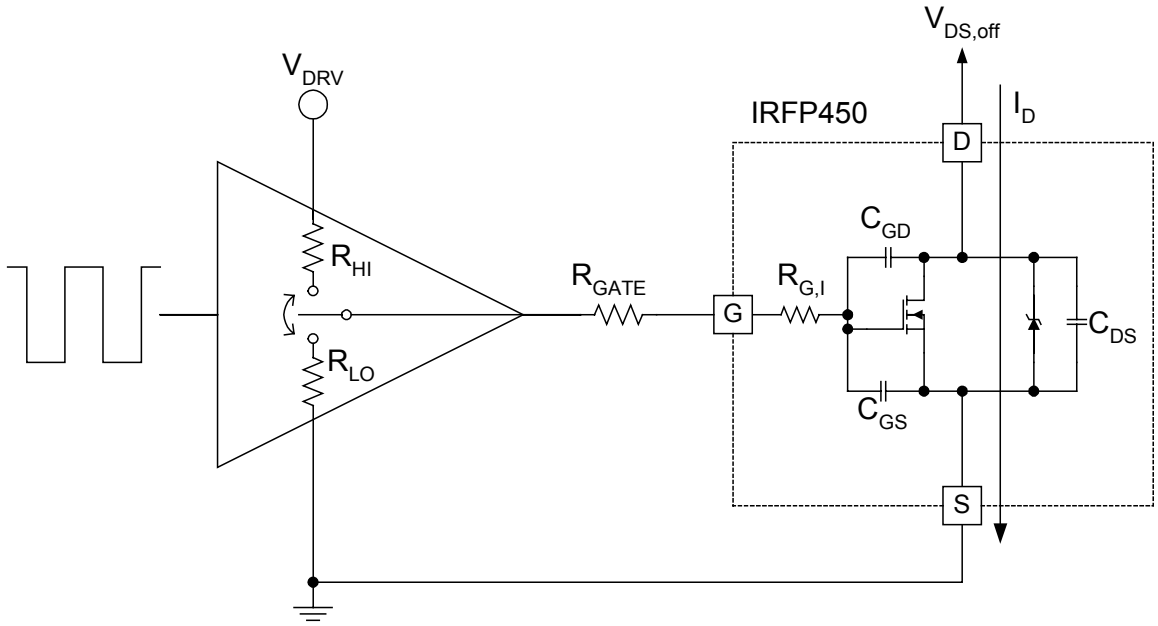
APPENDIX A

Estimating MOSFET Parameters from the Data Sheet
(Equivalent Capacitances, Gate Charge, Gate Threshold Voltage,
Miller Plateau Voltage, Internal Gate Resistance, Maximum Dv/Dt)

In this example, the equivalent C_{GS}, C_{GD}, and C_{DS} capacitances, total gate charge, the gate threshold voltage and Miller plateau voltage, approximate internal gate resistance, and dv/dt limits of an IRFP450 MOSFET will be calculated. A representative diagram of the device in a ground referenced gate drive application is pictured below.



The following application information are given to carry out the necessary calculations:

$V_{DS,OFF}$=380V	the nominal drain-to-source off state voltage of the device.
I_D=5A	the maximum drain current at full load.
T_J=100°C	the operating junction temperature.
V_{DRV}=13V	the amplitude of the gate drive waveform.
R_{GATE}=5Ω	the external gate resistance.
R_{LO}=R_{HI}=5Ω	the output resistances of the gate driver circuit.

A1. Capacitances

The data sheet of the IRFP450 gives the following capacitance values:

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C_{iss}	Input Capacitance	—	2600	—	pF	V_{GS}=0V
C_{oss}	Output Capacitance	—	720	—		V_{DS}= 25V
C_{rss}	Reverse Transfer Capacitance	—	340	—		f=1.0MHz See Figure 5

Using these values as a starting point, the average capacitances for the actual application can be estimated as:

Equations:

$$C_{RSS,ave} = 2 \cdot C_{RSS,spec} \cdot \sqrt{\frac{V_{DS,spec}}{V_{DS,off}}}$$

$$C_{OSS,ave} = 2 \cdot C_{OSS,spec} \cdot \sqrt{\frac{V_{DS,spec}}{V_{DS,off}}}$$

Numerical Example:

$$C_{RSS,ave} = 2 \cdot 340pF \cdot \sqrt{\frac{25V}{380V}} = 174pF$$

$$C_{OSS,ave} = 2 \cdot 720pF \cdot \sqrt{\frac{25V}{380V}} = 369pF$$

The physical capacitor values can be obtained from the basic relationships:

$$C_{GD} = C_{RSS,ave} \qquad C_{GD} = 174pF$$

$$C_{GS} = C_{ISS} - C_{RSS} \qquad C_{GS} = 2600pF - 340pF = 2260pF$$

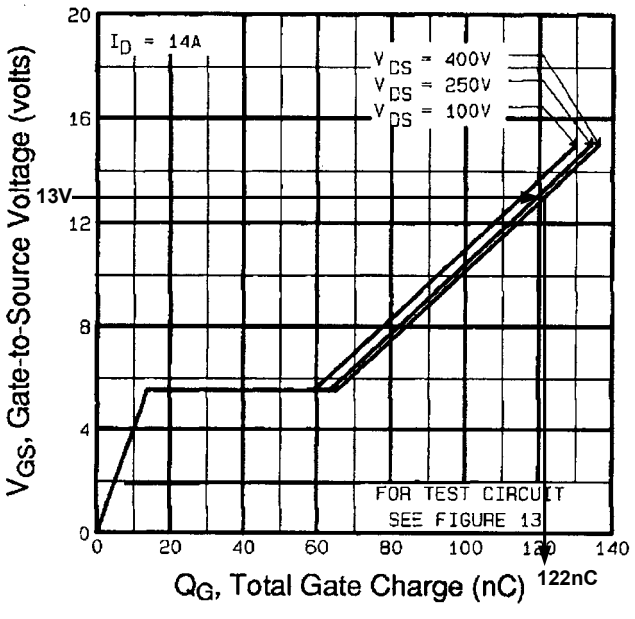
$$C_{DS} = C_{OSS,ave} - C_{RSS,ave} \qquad C_{DS} = 369pF - 174pF = 195pF$$

Notice that C_{GS} is calculated from the original data sheet values. Within one equation, it is important to use capacitor values which are measured under the same test conditions. Also keep in mind that C_{GS} is constant, it is not voltage dependent. On the other hand, C_{GD} and C_{DS} capacitors are strongly non-linear and voltage dependent. Their highest value is at or near 0V and rapidly decreasing as the voltage increases across the gate-to-drain and drain-to-source terminals respectively.

A2. Gate charge

The worst case gate charge numbers for a particular gate drive amplitude, drain current level, and drain off state voltage are given in the IRFP450 data sheet.

Q_g	Total Gate Charge	—	—	150	nC	I_D=14A
Q_{gs}	Gate-to-Source Charge	—	—	20		V_{DS}=400V
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	80		V_{GS}=10V See Fig. 6 and 13 ④



Correcting for a different gate drive amplitude is simple using the typical Total Gate Charge curve as illustrated on the left.

Starting from the 13V gate-to-source voltage on the left hand side, find the corresponding drain-to-source voltage curve (interpolate if not given exactly), then read the total gate charge value on the horizontal axes.

If a more accurate value is required, the different gate charge components must be determined individually. The gate-to-source charge can be estimated from the curve on the left, only the correct Miller plateau level must be known. The Miller charge can be calculated from the $C_{RSS,AVE}$ value obtained in A1. Finally, the over drive charge component – raising the gate-to-source voltage from the Miller plateau to the final amplitude – should be estimated from the graph on the left again.

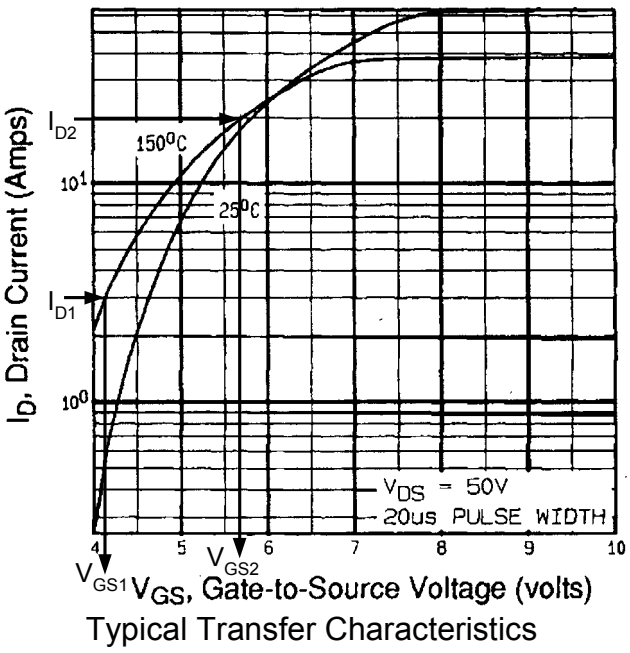
A3. Gate threshold and Miller plateau voltages

As it was already shown in A2, and will be demonstrated later, several MOSFET switching characteristic are influenced by the actual value of the gate threshold and Miller plateau voltages. In order to calculate the Miller plateau voltage, one possibility would be to use the gate-to-source threshold voltage (V_{TH}) and transconductance (g_{fs}) of the MOSFET as listed in the data sheet.

$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	V_{DS}=V_{GS}, I_D= 250μA
g_{fs}	Forward Transconductance	9.3	—	—	S	V_{DS}=50V, I_D=8.4A ④

Unfortunately, the threshold is not very well defined and the listed g_{fs} is a small signal quantity. A more accurate method to obtain the actual V_{TH} and Miller plateau voltages is to use the Typical Transfer Characteristics curves of the data sheet.

From the same temperature curve, pick two easy to read points and note the corresponding drain currents and gate-to-source voltages. Select the drain current values to correspond to vertical grid lines of the graph, that way the currents can be read accurately. Then follow the intersections to the horizontal axes and read the gate-to-source voltages. Starting with the drain currents will result in higher accuracy because the gate-to-source voltage is on a linear scale as opposed to the logarithmic scale in drain current. It is easier to estimate Vgs1 and Vgs2 on the linear scale therefore the potential errors are much smaller.



Typical Transfer Characteristics

For this example, using the 150°C curve:

$I_{D1} = 3A$

$V_{GS1} = 4.13V$

$I_{D2} = 20A$

$V_{GS2} = 5.67V$

The gate threshold and Miller Plateau voltages can be calculated as:

$$I_{D1} = K \cdot (V_{GS1} - V_{TH})^2$$

$$I_{D2} = K \cdot (V_{GS2} - V_{TH})^2$$

$$V_{TH} = \frac{V_{GS1} \cdot \sqrt{I_{D2}} - V_{GS2} \cdot \sqrt{I_{D1}}}{\sqrt{I_{D2}} - \sqrt{I_{D1}}} \qquad V_{TH} = \frac{4.13V \cdot \sqrt{20A} - 5.67V \cdot \sqrt{3A}}{\sqrt{20A} - \sqrt{3A}} = 3.157V$$

$$K = \frac{I_{D1}}{(V_{GS1} - V_{TH})^2} \qquad K = \frac{3A}{(4.13V - 3.157V)^2} = 3.169$$

$$V_{GS,Miller} = V_{TH} + \sqrt{\frac{I_{LOAD}}{K}} \qquad V_{GS,Miller} = 3.157V + \sqrt{\frac{5A}{3.169}} = 4.413V$$

These values correspond to 150°C junction temperature, because the 150°C curve from the Typical Transfer Characteristics was used. Due to the substantial temperature coefficient of the threshold voltage, the results have to be corrected for the 100°C operating junction temperature in this application. The gate threshold voltage and the Miller plateau voltage level must be adjusted by:

$$\Delta V_{ADJ} = (T_J - 150°C) \cdot TC \qquad \Delta V_{ADJ} = (100°C - 150°C) \cdot \left(-0.007 \frac{V}{°C}\right) = +0.35V$$

A4. Internal gate resistance

Another interesting parameter is the internal gate mesh resistance ($R_{G,I}$), which is not defined in the data sheet. This resistance is an equivalent value of a distributed resistor network connecting the gates of the individual MOSFET transistor cells in the device. Consequently, the gate signal distribution within a device looks and behaves very similar to a transmission line. This results in different switching times of the individual MOSFET cells within a device depending on the cells distance from the bound pad of the gate connection.

The most reliable method to determine $R_{G,I}$ is to measure it with an impedance bridge. The measurement is identical to the ESR measurement of capacitors which is routinely carried out in the lab. For this measurement the source and drain terminals of the MOSFET are shorted together. The impedance analyzer should be set to R_S-C_S or if it is available R_S-C_S-L_S equivalent circuit to yield the component values of the equivalent gate resistor, $R_{G,I}$, the MOSFET's input capacitance, C_{ISS} and the series parasitic inductance of the device, all connected in series.

For this example, the equivalent component values of an IRFP450 were measured by an HP4194 impedance analyzer. The internal gate resistance of the device was determined as $R_{G,I}$=1.6Ω. The equivalent inductance was measured at 12.9nH and the input capacitance was 5.85nF.

A5. dv/dt limit

MOSFET transistors are susceptible to dv/dt induced turn-on only when their drain-to-source voltage rises rapidly. Fundamentally, the turn-on is caused by the current flowing through the gate-drain capacitor of the device and generating a positive gate-to-source voltage. When the amplitude of this voltage exceeds the gate-to-source turn-on threshold of the device, the MOSFET starts to turn-on. There are three different scenarios to consider.

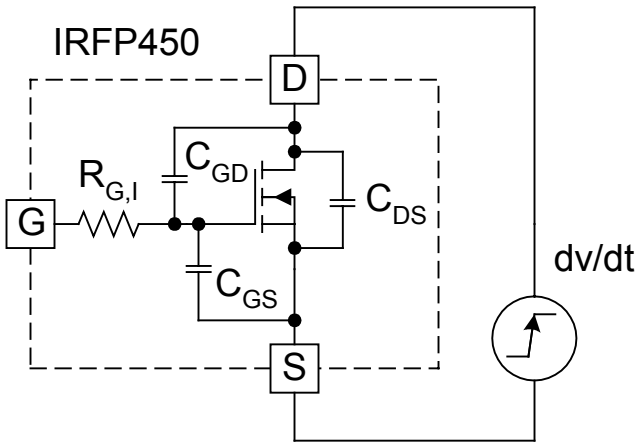
First, look at the capacitive divider formed by the C_{GD} and C_{GS} capacitors. Based on these capacitor values the gate-to-source voltage can be calculated as:

$$V_{GS} = V_{DS} \cdot \frac{C_{GD}}{C_{GS} + C_{GD}}$$

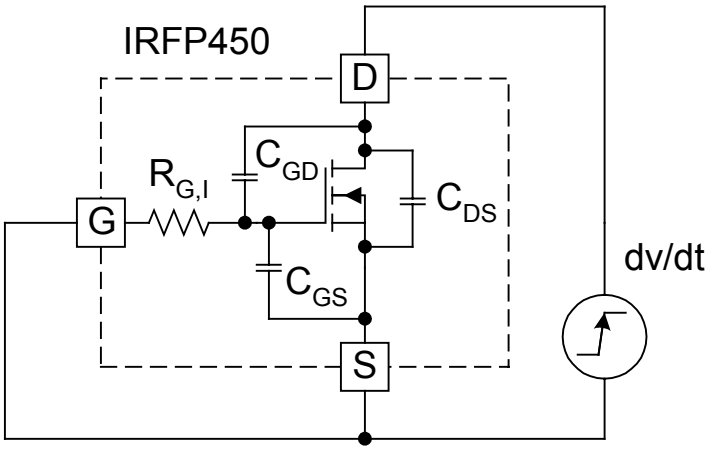
If $V_{GS}<V_{TH}$, the MOSFET stays off. The maximum drain-to-source voltage to ensure this can be estimated by:

$$V_{DS,MAX} \approx V_{TH} \cdot \frac{C_{GS} + C_{GD}}{C_{GD}}$$

This mechanism provides full protection against dv/dt induced turn-on in low voltage applications, independent of the internal gate resistor and the external drive impedances.



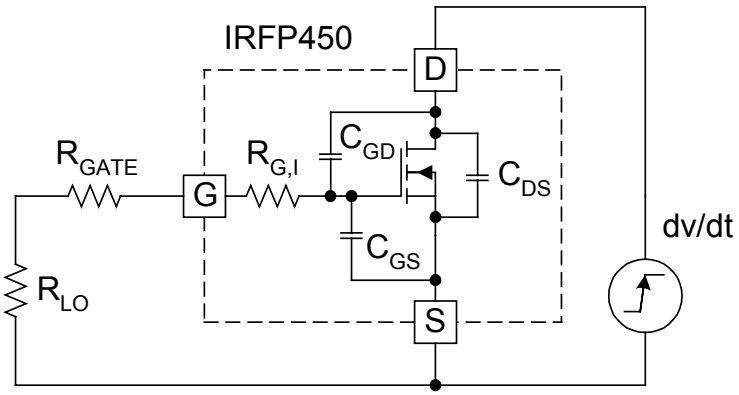
For higher voltage applications, it is desirable to determine the natural dv/dt limit of the MOSFET. This characteristic corresponds to the maximum dv/dt the device can withstand without turning on in an ideal situation where the external drive impedance is zero. This is signified by the shorted gate-source connection in the schematic diagram on the right.



The turn-on is initiated by the voltage drop across $R_{G,I}$ due to the charge current of C_{GD}. Accordingly, the natural dv/dt limit can be calculated by:

$$\left(\frac{dv}{dt}\right)_{N\text{-}LIMIT} = \frac{V_{TH}}{R_{G,I} \cdot C_{GD}}$$

This number is significant in evaluating the suitability of a device for a specific application where the turn-off dv/dt is forced by other components in the circuit. These applications include synchronous rectifiers, resonant mode and soft-switching power converters.



The third calculation describes the resulting dv/dt limit of the drain-to-source voltage waveform based on the parasitic components of the MOSFET device and the characteristics of the gate drive circuit. To avoid turn-on, the gate-to-source voltage must stay below the turn-on threshold voltage:

$$\left(\frac{dv}{dt}\right)_{LIMIT} = \frac{V_{TH}}{\left(R_{G,I} + R_{GATE} + R_{LO}\right) \cdot C_{GD}}$$

It is important to emphasize again that the threshold voltage of the MOSFET transistor changes significantly with temperature. Therefore, the effect of high junction temperature must be taken into effect. For the particular example using the IRFP450 type transistor at 100°C operating junction temperature the calculations yield the following limitations:

Case 1. No dv/dt induced turn-on takes place below the drain-to-source voltage of:

$$V_{DS,MAX} = \left(V_{TH} + \Delta V_{ADJ}\right) \cdot \frac{C_{GS} + C_{GD}}{C_{GD}} \qquad V_{DS,MAX} = \left(3.157V + 0.35V\right) \cdot \frac{2600pF}{340pF} = 26.82V$$

Case 2. The natural dv/dt limit of the IRFP450 is:

$$\left(\frac{dv}{dt}\right)_{N\text{-}LIMIT} = \frac{V_{TH} + \Delta V_{ADJ}}{R_{G,I} \cdot C_{GD}} \qquad \left(\frac{dv}{dt}\right)_{N\text{-}LIMIT} = \frac{3.157V + 0.35V}{1.6\Omega \cdot 340pF} = 6.4\frac{kV}{\mu s}$$

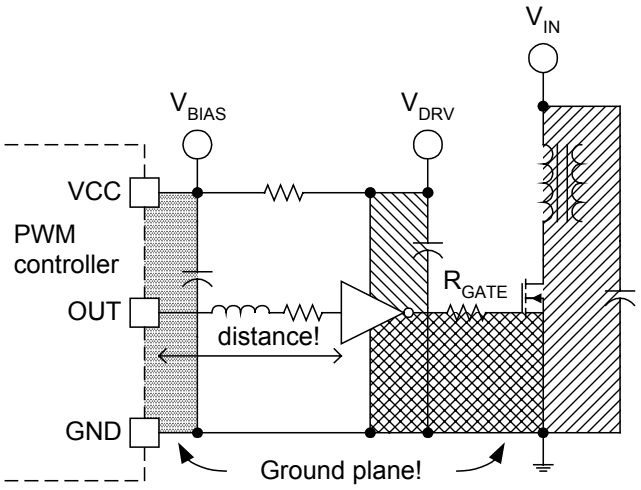
Case 3. The in-circuit dv/dt limit including the effect of the driver's output impedance is:

$$\left(\frac{dv}{dt}\right)_{LIMIT} = \frac{V_{TH} + \Delta V_{ADJ}}{\left(R_{G,I} + R_{GATE} + R_{LO}\right) \cdot C_{GD}} \qquad \left(\frac{dv}{dt}\right)_{LIMIT} = \frac{3.157V + 0.35V}{\left(1.6\Omega + 5\Omega + 5\Omega\right) \cdot 340pF} = 889\frac{V}{\mu s}$$

APPENDIX B

Calculating Driver Bypass Capacitor Value

MOSFET drivers must be operated from a low impedance voltage source to achieve high switching speed and reliable operation. To provide this virtual voltage source, the bias line of the drivers must be locally bypassed by very good quality, high frequency capacitors. In most applications this capacitance is realized by low impedance, high frequency, multilayer ceramic capacitors. Half of the success in bypassing can be ensured by the proper location of the bypass capacitors and the driver itself. Some of the most important rules of proper gate drive design are highlighted in the example below:



- The driver should be close to the device it is driving. Significant distance can be tolerated between the PWM controller and the MOSFET driver with careful layout design. Even though there is no high current between the output of the PWM IC and the input of the driver, relatively wide printed circuit board traces can reduce the parasitic interconnection inductance, thus providing lower loop impedance and better noise immunity.
- It is also important to separately bypass the individual noise sources, i.e. the power stage, the PWM controller and the driver both have their own respective bypass capacitors. The three shaded loop areas must be minimized.

During turn-on the gate current flows through the bypass capacitor of the driver, while during turn-off the high frequency bypass capacitor of the power stage must provide a path to charge the C_{GD} capacitor of the MOSFET.

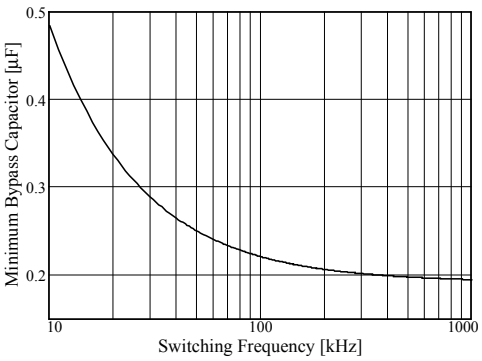
In this numerical example an IRFP350 MOSFET is driven by a Micrel MIC4423 driver. The driver's quiescent current $I_{Q,HI}$ with a high input, is 2.5mA. When the input is low the quiescent current is negligible. The switching frequency is 100kHz and the maximum duty ratio of the PWM signal is 0.7. The gate is driven by a 12V signal, and the off state voltage of the device is approximately 300V.

From these operating conditions the total gate charge can be estimated as 115nC. A 5% percent ripple voltage across the bypass capacitor is acceptable, and a 12V bias would allow 0.6V ripple voltage. The equation to calculate the minimum bypass capacitor value is:

$$C_{BYPASS} = \frac{I_{Q,HI} \cdot \frac{D_{MAX}}{f_{DRV}} + Q_G}{\Delta V}$$

$$C_{BYPASS} = \frac{2.5mA \cdot \frac{0.7}{100kHz} + 115nC}{0.6V} = 221nF$$

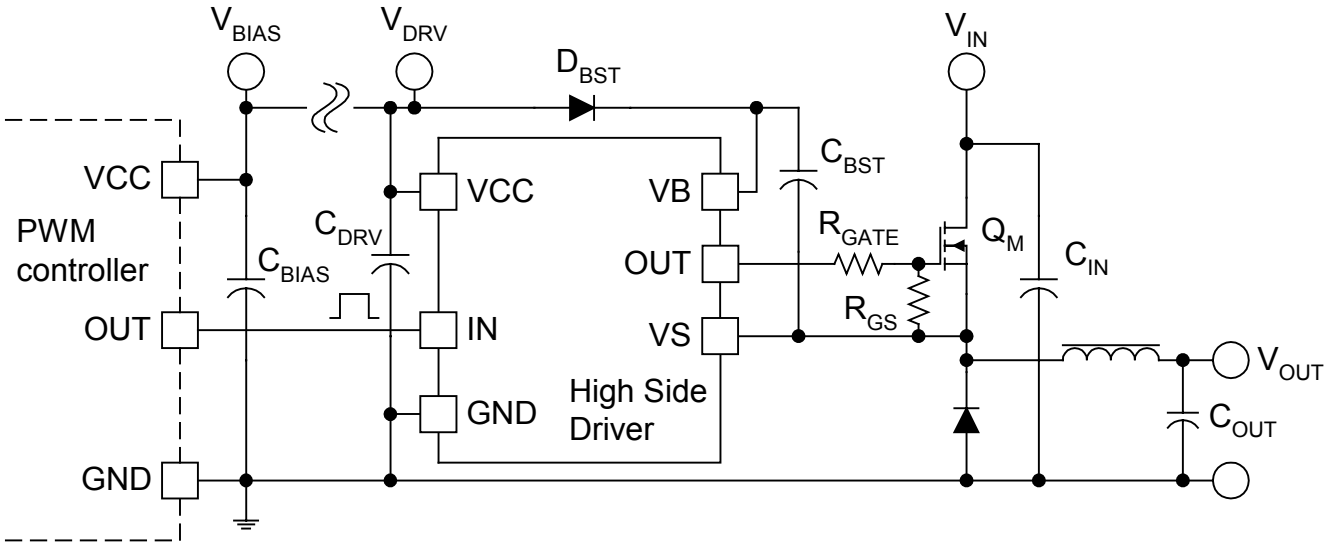
The effect of switching frequency on the bypass capacitor value is depicted in the figure on the right. At high frequency, the gate charge determines the minimum bypass capacitor, thus the curve approaches an asymptotic minimum value. At low operating frequencies the quiescent current of the driver commands the minimum capacitor size. Note that this ripple component depends on the duty ratio of the PWM signal. For this calculation, the worst case situation (D=0.7) was considered.



APPENDIX C

Bootstrap Bypass Capacitor Example

In this example an IR2125 high voltage integrated gate driver is employed to drive an IRF1310N transistor in a 48V input buck converter. The corresponding schematic diagram is given below.



Let's assume the following application parameters:

$V_{IN,MAX}$=65V	the maximum steady state input voltage.
V_{DRV}=12V	the bias voltage for the high side driver and the gate drive amplitude.
ΔV_{BST}=0.5V	the steady state ripple voltage across C_{BST}.
$\Delta V_{BST,MAX}$=3V	the maximum voltage droop across C_{BST} before the driver goes to under voltage lockout or the gate drive amplitude becomes insufficient.
f_{DRV}=100kHz	the switching frequency.
D_{MAX}=0.9	the maximum steady state duty ratio at minimum input voltage – the controller does not limit the maximum duty cycle in this example.
$t_{OFF,TR}$=400µs	transient off-time – at sudden removal of the load, the MOSFET stays off for this time interval.
$t_{ON,TR}$=200µs	transient on-time – at sudden increase of the load current, the controller keeps the MOSFET on for this time interval to build up the output inductor current.

The circuit components are characterized by:

Q_G=85nC	the total gate charge of the IRF1310 @ V_{DRV}=12V and V_{DS}=65V.
R_{GS}=5.1kΩ	the gate-to-source pull down resistor value.
I_R=10µA	leakage current of D_{BST} @ $V_{IN,MAX}$ and T_J=80°C.
V_F=0.6V	forward voltage drop of D_{BST} @ 0.1A and T_J =80°C.
I_{LK}=0.13mA	leakage current of the level shifter @ $V_{IN,MAX}$ and T_J =100°C.
I_{QBS}=1mA	quiescent current of the floating driver.

First, consider the steady state operation of the driver. Based on the ripple budget of 0.5V and the amount of charge consumed from the bootstrap capacitor, a minimum capacitance value can be established:

$$C_{BST,1} = \frac{\left(I_R + I_{LK} + I_{QBS} + \frac{V_{DRV} - V_F}{R_{GS}}\right) \cdot \frac{D_{MAX}}{f_{DRV}} + Q_G}{\Delta V_{BST}}$$

Substituting the numerical values yields the minimum bootstrap capacitor value for steady state operation:

$$C_{BST,1} = \frac{\left(10\mu A + 0.13mA + 1mA + \frac{12V - 0.6V}{5.1k\Omega}\right) \cdot \frac{0.9}{100kHz} + 85nC}{0.5V} = 231nF$$

For the transient conditions calculate the capacitor values based on the maximum voltage droop. When the switch has to stay off for an extended period of time, the output inductor current decays to zero and the source of the main switch settles at the output voltage. The bootstrap diode is reverse biased and the bootstrap capacitor has to keep the floating driver alive. Moreover, at the end of the idle period, C_{BST} still has to provide the gate charge to turn-on the MOSFET. Accordingly, the required capacitor value is:

$$C_{BST,2} = \frac{\left(I_R + I_{LK} + I_{QBS} + \frac{V_{DRV} - V_F}{R_{GS}}\right) \cdot t_{OFF,TR} + Q_G}{\Delta V_{BST,MAX}}$$

Using the actual application parameters:

$$C_{BST,2} = \frac{\left(10\mu A + 0.13mA + 1mA + \frac{12V - 0.6V}{5.1k\Omega}\right) \cdot 400\mu s + 85nC}{3V} = 478nF$$

The last calculation is carried out to check whether the switch can be turned on continuously for the desired 200 microseconds transient on time. The long on period will be followed by a guaranteed off-time when the bootstrap capacitor can be replenished. The bootstrap capacitor must hold enough energy to support the quiescent and leakage currents only as indicated in the expression below:

$$C_{BST,3} = \frac{\left(I_R + I_{LK} + I_{QBS} + \frac{V_{DRV} - V_F}{R_{GS}}\right) \cdot t_{ON,TR}}{\Delta V_{BST,MAX}}$$

With the given numerical values:

$$C_{BST,3} = \frac{\left(10\mu A + 0.13mA + 1mA + \frac{12V - 0.6V}{5.1k\Omega}\right) \cdot 200\mu s}{3V} = 225nF$$

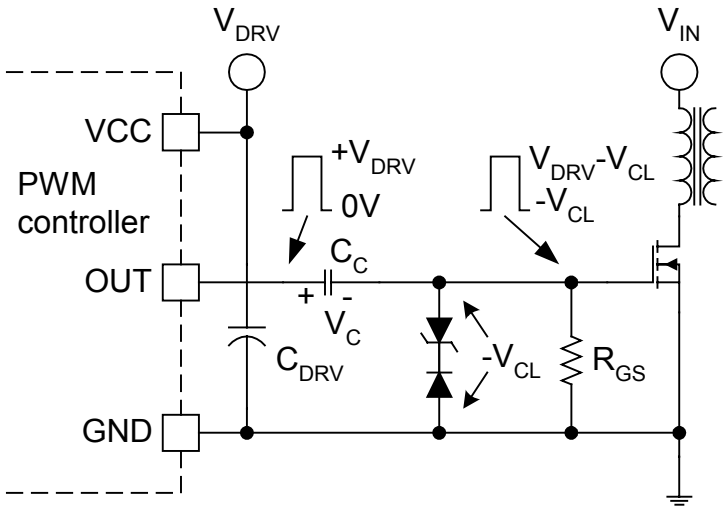
To fulfill all three requirements, the highest capacitor value (C_{BST}=470nF) should be selected.

The high side driver IC must be bypassed not only by the bootstrap capacitor, but also by another ground referenced capacitor as indicated in the schematic diagram. C_{DRV} provides the high peak charge current to replenish the energy taken from C_{BST} during the preceding on-time of the main MOSFET. If $C_{DRV} >> C_{BST}$, the bootstrap capacitor can be recharged to the full V_{DRV} level. Usually, C_{DRV} is an order of magnitude larger capacitance than C_{BST}. When selecting the value of the low side bypass capacitor, primarily the steady state operation should be considered. Accordingly, $C_{DRV} \approx 10 \cdot C_{BST,1}$, which requires C_{DRV} = 2.2µF.

APPENDIX D

Coupling Capacitor and Transient Settling Time Calculation

In this example the coupling capacitor and gate-to-source resistor value of an AC coupled gate drive circuit will be calculated. The design goal is to provide a 3V negative bias for the MOSFET during its off time. The application circuit is shown below:



The following application information is given:

dV_{IN}/dt=200V/ms	the maximum dv/dt of the input voltage during power up, limited by the combined effect of the inrush current limiting circuit and the input energy storage capacitor.
$C_{GD,0}$=1nF	the maximum gate-to-drain capacitance of the MOSFET read from the data sheet at 0V drain-to-source voltage (worst case start-up condition).
V_{TH}=2.7V	the gate-to-source turn-on threshold @ $T_{A,MAX}$.
V_{DRV}=15V	the supply voltage of the PWM controller, i.e. the gate driver's bias voltage.
f_{DRV}=100kHz	the switching frequency.
D_{MAX}=0.8	maximum duty ratio, limited by the PWM controller to reset the transformer.
V_{CL}=3V	the negative bias amplitude.
ΔV_C=1.5V	maximum allowable ripple of the coupling capacitor.
Q_G=80nC	total gate charge of the MOSFET .
τ=100µs	transient time constant for the coupling capacitor voltage (V_C). This is the start-up time constant as well to establish the initial value of V_C.

The design starts by determining the maximum value of the gate pull down resistor. During power-up, R_{GS} must be low enough to keep the MOSFET off. When the voltage rises across the drain-source terminal, the C_{GD} capacitor is charged and a current proportional to dV_{IN}/dt flows through R_{GS}. The MOSFET stays off if the voltage drop across R_{GS} remains below the gate threshold. Therefore, the maximum allowable R_{GS} value is:

$$R_{GS,MAX} = \frac{V_{TH}}{C_{GD,0} \cdot \frac{dV_{IN}}{dt}}$$

$$R_{GS,MAX} = \frac{2.7V}{1nF \cdot 200000\frac{V}{s}} = 13.5k\Omega$$

The next step is to find the common solution for the required time constant and ripple voltage. The two equations are:

$$\tau = C_C \cdot R_{GS}$$

$$C_C = \frac{Q_G \cdot \tau \cdot f_{DRV}}{\Delta V_C \cdot \tau \cdot f_{DRV} - V_{DRV} \cdot D + V_C(D) \cdot D}$$

where $V_C(D)$ is the coupling capacitor voltage as a function of the duty ratio. The second equation can be evaluated right away since all parameters are defined. In general, $V_C(D)=D \cdot V_{DRV}$ if the clamp circuit is not used, and the expression has a local maximum at D=0.5, which gives the minimum coupling capacitor value. In this application, the coupling capacitor voltage is limited to 3V by the zener clamp. Thus for D>0.2, the coupling capacitor voltage is constant, and V_C=3V. Consequently, the maximum value of the second equation is not at D=0.5, but rather at the maximum duty cycle, D_{MAX}.
Before calculating C_C, another important limitation should be pointed out. In order to arrive at a meaningful positive capacitor value, the denominator of the second equation must be positive which sets a limit on the transient time constant. This limit is:

$$\tau_{MIN} = \frac{D \cdot (V_{DRV} - V_C(D))}{\Delta V_C \cdot f_{DRV}}$$

This function has a maximum value at D=0.5 if the clamp circuit is not used. With the clamp circuit, $D=D_{MAX}$ will define the fastest possible transient response of the coupling capacitor voltage. Substituting the application parameters and using the appropriate equation for the clamp case yields the following values:

$$\tau_{MIN} = \frac{D_{MAX} \cdot (V_{DRV} - V_{CL})}{\Delta V_C \cdot f_{DRV}} \qquad \tau_{MIN} = \frac{0.8 \cdot (15V - 3V)}{1.5V \cdot 100kHz} = 64\mu s$$

$$C_C = \frac{Q_G \cdot \tau \cdot f_{DRV}}{\Delta V_C \cdot \tau \cdot f_{DRV} - D_{MAX} \cdot (V_{DRV} - V_{CL})} \qquad C_C = \frac{80nC \cdot 100\mu s \cdot 100kHz}{1.5V \cdot 100\mu s \cdot 100kHz - 0.8 \cdot (15V - 3V)} = 148nF$$

$$R_{GS} = \frac{\tau}{C_C} \qquad R_{GS} = \frac{100\mu s}{148nF} = 675\Omega$$

These results are acceptable because $\tau_{MIN}<\tau$ and $R_{GS,MAX}>R_{GS}$, therefore all conditions are met. The worst case power dissipation of R_{GS} is 173mW at the maximum duty ratio of 0.8. If this value is not acceptable, selecting a longer time constant will increase the pull down resistor value. At the same time the power dissipation and the coupling capacitor value will decrease.

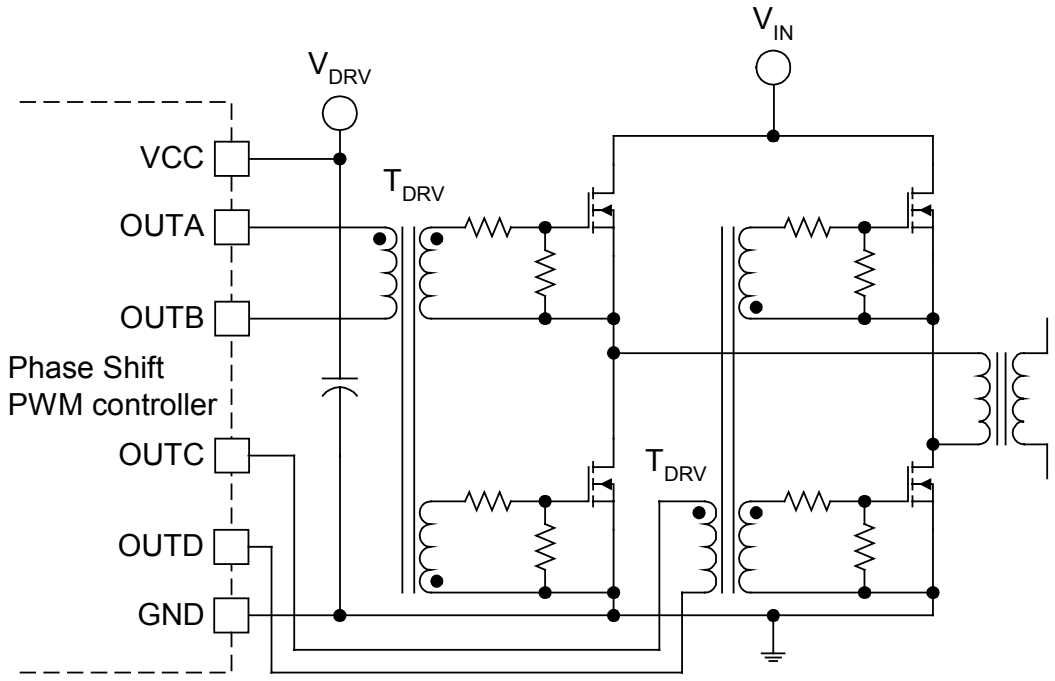
The last calculation is to compute the bypass capacitor value. Assuming a maximum of 1V ripple on the bias rail (ΔV_{DRV}=1V) the following minimum bypass capacitance value will result:

$$C_{DRV} = \frac{Q_G}{\Delta V_{DRV}} + \frac{V_{DRV} - V_{CL}}{\Delta V_{DRV} \cdot R_{GS} \cdot f_{DRV}} \cdot D_{MAX} \qquad C_{DRV} = \frac{80nC}{1V} + \frac{15V - 3V}{1V \cdot 675\Omega \cdot 100kHz} \cdot 0.8 = 222nF$$

APPENDIX E

Gate Drive Transformer Design Example

The gate drive transformers for a phase shifted full-bridge converter will be designed according to the schematic diagram below:



In this example, the PWM controller has four high current output drivers on-board. The gate drive transformer design is based on the following application information:

f_{CLOCK}=400kHz	the clock frequency.
f_{DRV}=200kHz	the operating frequency of the gate drive transformers.
D_{MAX}=0.5	maximum duty ratio of the gate drive transformer.
V_{DRV}=15V	the bias voltage of the controller, which is also used to power the output drivers.

The first task is to choose the core size. A seasoned designer can pick the right core for the first try based on previous experience. But even then, like all magnetics problem solving, the gate drive transformer design might require a couple of iterations. For this application a Ferroxcube RM5/I core was selected with no airgap. The preferred choice of material is 3C94 because it has the highest permeability and lowest loss at 200kHz from the available selection.

Ae=24.8mm^2	effective cross section area of the core.
Ve=574mm^3	effective volume of the core.
B_{SAT}=0.35T	saturation flux density of the ferrite material @ 100°C.
A_L=2μH/turns^2	equivalent inductance per turns square.
B_{PEAK}=0.1T	peak flux density in steady state operation. Remember, that during transient operation the transformer's flux can walk due to uneven duty cycles. Usually, a 3:1 margin is desirable.
ΔB=0.2T	peak-to-peak flux density in steady state operation.

Check the core loss under these conditions from the data sheet.

P_V=200kW/m^3 effective volumetric power dissipation of 3C94 @ B_{PEAK}=0.1T and 200kHz. (it is more meaningful to convert to 0.2mW/mm^3.)

$$P_{CORE} = P_V \cdot V_e \qquad P_{CORE} = 0.2\frac{mW}{mm^3} \cdot 574mm^3 = 115mW$$

The power dissipation of the RM5/I core is 115mW which is acceptable. Next, calculate the primary number of turns according to:

$$N_P = \frac{V_{DRV} \cdot D_{MAX}}{\Delta B \cdot A_e \cdot f_{DRV}} \qquad N_P = \frac{15V \cdot 0.5}{0.2T \cdot 24.8mm^2 \cdot 200kHz} = 7.56 \text{ turns}$$

The next higher full turn is selected, N_P=8 turns. Since voltage scaling is not required in this gate drive transformer, the two secondary windings have 8 turns as well. In order to minimize leakage inductance and AC winding resistance, each winding should occupy a single layer only. The following data is needed to execute the winding design:

W_W=4.7mm the winding width from the data sheet of the coil former.
MLT=24.9mm the average length of turn also from the coil former data sheet.

Considering that at the termination N+1 wires are side by side, the corresponding wire diameter is:

$$d_W = \frac{W_W}{N_P + 1} \qquad d_W = \frac{4.7mm}{9} = 0.52mm = 20.5mils$$

The closest smaller diameter wire size according to the American Wire Gauge table is #25 and its characteristic data is:

d_W=0.0199mils heavy built (double isolated) nominal diameter. (0.0199mils=0.506mm)
ρ_W=32.37Ω/1000ft. normalized wire resistance. (32.37Ω/1000ft =0.1062mΩ/mm)

The DC winding resistance is:

$$R_{W,DC} = N_P \cdot MLT \cdot \rho_W \qquad R_{W,DC} = 8 \cdot 24.9mm \cdot 0.1062\frac{m\Omega}{mm} = 21.2m\Omega$$

Next, check the AC resistance based on Dowell's curves according to the following steps:

$$D_{PEN} = \frac{7.6}{\sqrt{f_{DRV}}} \qquad D_{PEN} = \frac{7.6}{\sqrt{200000}} = 0.017cm$$

$$Q = \frac{0.83 \cdot d_W}{D_{PEN}} \qquad Q = \frac{0.83 \cdot 0.506mm}{0.17mm} = 2.47$$

Entering Dowell's graph at Q=2.5, the single layer curve gives an R_{AC}/R_{DC}=3 ratio, thus the AC resistance of the winding is R_{AC}=3·21.2mΩ=63.6mΩ, which is quite acceptable.

The last step is to calculate the magnetizing inductance and current values:

$$L_M = A_L \cdot N^2 \qquad L_M = 2\frac{\mu H}{turns^2} \cdot 8^2 = 128\mu H$$

$$I_{M,P} = \frac{\Delta I_M}{2} = \frac{1}{2} \cdot \frac{V_{DRV} \cdot D_{MAX}}{L_M \cdot f_{DRV}} \qquad I_{M,P} = \frac{1}{2} \cdot \frac{15V \cdot 0.5}{128\mu H \cdot 200kHz} = 146mA$$

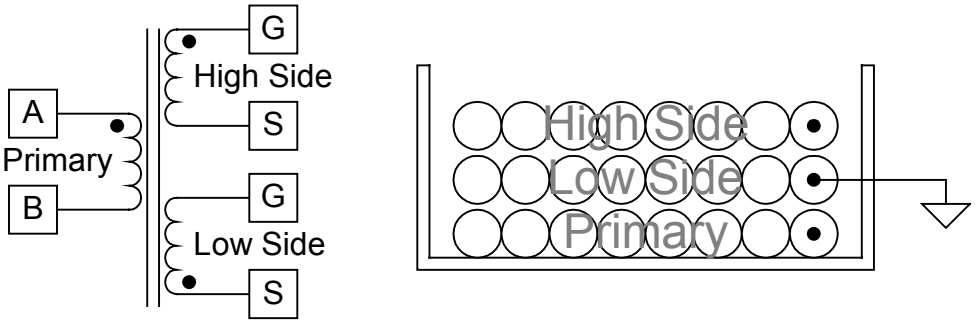
$$I_{M,RMS} = I_{M,P} \cdot \sqrt{\frac{D_{MAX}}{3}} \qquad I_{M,RMS} = 146mA \cdot \sqrt{\frac{0.5}{3}} = 60mA$$

Based on the RMS value of the magnetizing current, the wire loss is:

$$P_W = I_{M,RMS}^2 \cdot R_{AC} \qquad P_W = (60mA)^2 \cdot 63.6m\Omega = 0.2mW$$

This result demonstrates that power dissipation in the winding is not an issue in the gate drive transformer. The high magnetizing inductance and low winding resistance are the most critical design parameters to achieve low droop in the gate drive waveform. Also notice that copper loss is based purely on AC resistance, because in an **ideal, steady state** operation there is no DC current in the windings.

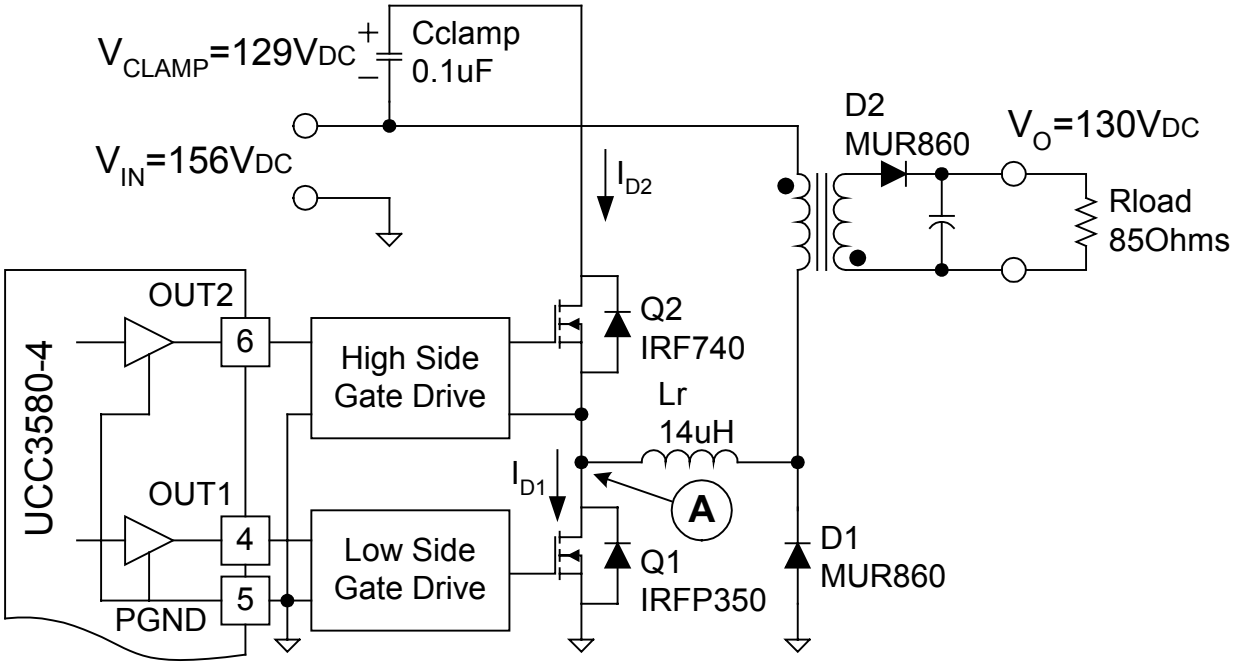
Finally, the winding arrangement of the transformer is shown below. The primary is near the center post, then the low side, and the high side windings. All windings are in a single layer. The low side winding is utilized as a natural shield against parasitic capacitive currents between signal ground and the floating circuitry.



APPENDIX F

A Step by Step Design Example of a Ground Referenced and a Floating High Side Gate Driver for an Active Clamp Flyback Converter

The gate drive design process begins AFTER the power stage is designed and the power components are selected. The simplified final schematic diagram of the active clamp flyback converter is shown below.



The relevant operating parameters are:

$V_{DS1,off}=V_{DS2,off}=285V$	the off state drain-to-source voltage of Q1 and Q2. Both transistors are switching between ground (0V) and $V_{IN}+V_{CLAMP}$.
$I_{D1}=2.7A$	the peak drain current of Q1 at turn-off.
$T_J=100°C$	the operating junction temperature of the devices.
$L_R=14uH$	the resonant inductor of the active clamp flyback power stage.

The specified driver output impedances and gate drive parameters of the UCC3580-4 are:

OUT1	**OUT2**
$V_{DRV}=15V$	$V_{DRV}=15V$
$D_{MAX1}=0.7$	$D_{MAX2}=0.95$
$f_{DRV}=250kHz$	$f_{DRV}=250kHz$
$R_{HI1}=20\Omega$	$R_{HI2}=33\Omega$
$R_{LO1}=10\Omega$	$R_{LO2}=33\Omega$

The estimated MOSFET parameters according to the operating junction temperature and based on the methods demonstrated in the previous Appendix's are:

IRFP350

Q_{G1}=135nC
C_{GD1}=148pF
C_{OSS1}=391pF
$R_{G1,I}$=1.2Ω
V_{TH1}=3.2V
$V_{GS1,Miller}$=4.2V

IRF740

Q_{G2}=60nC
C_{GD2}=71pF
C_{OSS2}=195pF
$R_{G2,I}$=1.63Ω
V_{TH2}=3.5V
$V_{GS2,Miller}$=4.8V

Next, establish the dv/dt of the external resonant circuit and the dv/dt of the devices. At node A, the resonant inductor, L_R, charges and discharges the effective node capacitance. The inductor current barely changes during the short switching action, therefore it can be looked at as a DC current source. The node capacitance and the resulting dv/dt of the power stage are:

$$C_R = C_{OSS1} + C_{OSS2} \qquad C_R = 391pF + 195pF = 586pF$$

$$\frac{dv}{dt}_{RES} \approx \frac{I_{D1}}{C_R} \qquad \frac{dv}{dt}_{RES} \approx \frac{2.7A}{586pF} = 4.6\frac{kV}{\mu s}$$

The turn-on dv/dt of the MOSFET and the dv/dt_{LIMIT} to prevent dv/dt induced turn-on assuming R_{GATE}=0Ω are:

$$\frac{dv}{dt}_{ON} = \frac{V_{DRV} - V_{GS,Miller}}{(R_{G,I} + R_{HI}) \cdot C_{GD}}$$

$$\frac{dv}{dt}_{Q1,ON} = \frac{15V - 4.2V}{(1.2\Omega + 20\Omega) \cdot 148pF} = 3.4\frac{kV}{\mu s}$$

$$\frac{dv}{dt}_{Q2,ON} = \frac{15V - 4.8V}{(1.63\Omega + 33\Omega) \cdot 71pF} = 4.15\frac{kV}{\mu s}$$

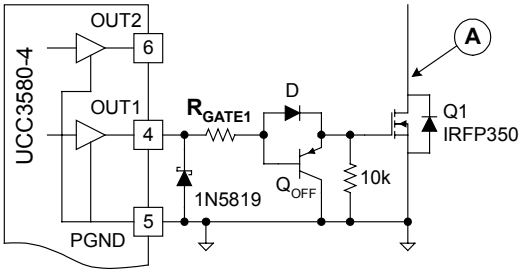
$$\frac{dv}{dt}_{LIMIT} = \frac{V_{TH}}{(R_{G,I} + R_{LO}) \cdot C_{GD}}$$

$$\frac{dv}{dt}_{Q1,LIMIT} = \frac{3.2V}{(1.2\Omega + 10\Omega) \cdot 148pF} = 1.93\frac{kV}{\mu s}$$

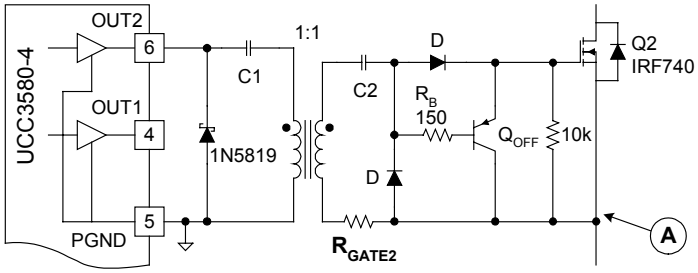
$$\frac{dv}{dt}_{Q2,LIMIT} = \frac{3.5V}{(1.63\Omega + 33\Omega) \cdot 71pF} = 1.42\frac{kV}{\mu s}$$

Since the resonant dv/dt is higher than the dv/dt_{LIMIT} calculated for both Q1 and Q2 transistors, a turn-off speed-up circuit must be used in both drive circuits. The selected low side and high side gate drive circuits are presented below:

IRFP350 (Low Side Drive)



IRF740 (High Side Drive)



Now, the dv/dt_{LIMIT} numbers must be re-calculated assuming that the drivers' output impedance is shunted out. Also, pay attention to the 0.7V voltage drop across the pn junction of the Q_{OFF} transistors.

$$\frac{dv}{dt}_{Q1,LIMIT} = \frac{3.2V - 0.7V}{1.2\Omega \cdot 148pF} = 14\frac{kV}{\mu s} \qquad \frac{dv}{dt}_{Q2,LIMIT} = \frac{3.5V - 0.7V}{1.63\Omega \cdot 71pF} = 24\frac{kV}{\mu s}$$

The next step is to calculate the gate resistor values. The gate resistor sets the turn-on dv/dt of the device which must be lower than the dv/dt_{LIMIT}. Slowing down the turn-on dv/dt might be beneficial to reduce EMI and to decrease reverse recovery problems in the rectifier diodes. For this design the turn-on dv/dt of both transistors is limited below 2.3kV/us. This value was selected to be half of the resonant dv/dt calculated before under full load conditions. Accordingly:

$$\frac{dv}{dt}_{ON} = \frac{V_{DRV} - V_{GS,Miller}}{\left(R_{HI} + R_{GATE} + R_{G,I}\right)\cdot C_{GD}} \qquad \rightarrow \qquad R_{GATE} = \frac{V_{DRV} - V_{GS,Miller}}{\frac{dv}{dt}_{ON}\cdot C_{GD}} - \left(R_{HI} + R_{G,I}\right)$$

and

$$R_{GATE1} = \frac{15V - 4.2V}{2.3\frac{kV}{\mu s}\cdot 148pF} - \left(20\Omega + 1.2\Omega\right) = 10.5\Omega \qquad R_{GATE2} = \frac{15V - 4.8V}{2.3\frac{kV}{\mu s}\cdot 71pF} - \left(33\Omega + 1.6\Omega\right) = 27\Omega$$

At this point the low side driver is fully defined. The procedure continues with the gate drive transformer design. The details of this calculation are omitted here. A step by step example is given in Appendix E. The gate drive transformer's relevant characteristics for further calculations are:

L_M=100uH	the magnetizing inductance of the transformer.
$I_{M,P}$=75mA	the maximum peak value of the magnetizing current at D=0.5.

There are two coupling capacitors in the high side driver circuitry, and their values are calculated next. Assume ΔV_{C1}=0.65V and ΔV_{C2}=0.65V. The sum of these two ripple components will be present at the gate of Q2 (ΔV_{GATE}=1.3V).

$$C_{C2} = \frac{Q_{G2}}{\Delta V_{C2}} + \frac{\left(V_{DRV} - V_{D,FW}\right)\cdot D_{MAX}}{\Delta V_{C2}\cdot R_{GS}\cdot f_{DRV}} \qquad C_{C2} = \frac{60nC}{0.65V} + \frac{\left(15V - 0.7V\right)\cdot 0.95}{0.65V\cdot 10k\Omega\cdot 250kHz} = 100nF$$

$$C_{C1} = \frac{Q_{G2}}{\Delta V_{C1}} + \frac{\left(V_{DRV} - V_{D,FW}\right)\cdot D}{\Delta V_{C1}\cdot R_{GS}\cdot f_{DRV}} + \frac{V_{DRV}\cdot\left(D^2 - D^3\right)}{\Delta V_{C1}\cdot 4\cdot L_M\cdot f_{DRV}^2}$$

where D=0.68, corresponding to the maximum of the C_{C1} equation above.

$$C_{C1} = \frac{60nC}{0.65V} + \frac{\left(15V - 0.7V\right)\cdot 0.68}{0.65V\cdot 10k\Omega\cdot 250kHz} + \frac{15V\cdot\left(0.68^2 - 0.68^3\right)}{0.65V\cdot 4\cdot 100\mu H\cdot\left(250kHz\right)^2} = 235nF$$

Verify the start-up time constant of the AC coupling network:

$$\tau = \frac{2\cdot\pi\cdot f_{DRV}\cdot L_M\cdot R_{GS}\cdot C_{C1}}{2\cdot\pi\cdot f_{DRV}\cdot L_M + R_{GS}} \qquad \tau = \frac{2\cdot\pi\cdot 250kHz\cdot 100\mu H\cdot 10k\Omega\cdot 235nF}{2\cdot\pi\cdot 250kHz\cdot 100\mu H + 10k\Omega} = 36\mu s$$

Check the gate power loss and the power dissipation of the UCC3850 output drivers:

$$P_{GATE} = V_{DRV}\cdot\left(Q_{G1} + Q_{G2}\right)\cdot f_{DRV} \qquad P_{GATE} = 15V\cdot\left(135nC + 60nC\right)\cdot 250kHz = 731mW$$

$$P_{OUT1} = \frac{1}{2}\cdot\frac{R_{HI1}}{R_{HI1} + R_{GATE1} + R_{G1,I}}\cdot Q_{G1}\cdot V_{DRV}\cdot f_{DRV} \qquad P_{OUT1} = \frac{0.5\cdot 20\Omega\cdot 135nC\cdot 15V\cdot 250kHz}{20\Omega + 10\Omega + 1.2\Omega}\cdot = 162mW$$

$$P_{OUT2} = \frac{1}{2}\cdot\frac{R_{HI2}}{R_{HI2} + R_{GATE2} + R_{G2,I}}\cdot Q_{G2}\cdot V_{DRV}\cdot f_{DRV} + \frac{I_{M,P}^2}{3}\cdot R_{HI2}$$

$$P_{OUT2} = \frac{0.5 \cdot 33\Omega \cdot 60nC \cdot 15V \cdot 250kHz}{33\Omega + 27\Omega + 1.2\Omega} + \frac{(75mA)^2}{3} \cdot 33\Omega = 122mW$$

The UCC3580 dissipates 284mW of the total 731mW gate drive power loss.

Lastly, the bypass capacitor value is calculated. The bypass capacitor supplies the gate charge for both MOSFETs, the currents through the two gate pull down resistors, R_{GS1} and R_{GS2}, and the magnetizing current of the gate drive transformer. Its value can be estimated by:

$$C_{DRV} \approx \frac{Q_{G1} + Q_{G2}}{\Delta V_{DRV}} + \frac{V_{DRV} \cdot D_{MAX1}}{\Delta V_{DRV} \cdot R_{GS1} \cdot f_{DRV}} + \frac{(V_{DRV} - V_{D,FW}) \cdot D_{MAX1}}{\Delta V_{DRV} \cdot R_{GS2} \cdot f_{DRV}} + \frac{V_{DRV} \cdot (D_{MAX1}^2 - D_{MAX1}^3)}{\Delta V_{DRV} \cdot 4 \cdot L_M \cdot f_{DRV}^2}$$

$$C_{DRV} \approx \frac{135nC + 60nC}{1V} + \frac{15V \cdot 0.7}{1V \cdot 10k\Omega \cdot 250kHz} + \frac{(15V\text{-}0.7V) \cdot 0.7}{1V \cdot 10k\Omega \cdot 250kHz} + \frac{15V \cdot (0.7^2 - 0.7^3)}{1V \cdot 4 \cdot 100\mu H \cdot (250kHz)^2} = 291nF$$

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