

Power Supply Design Seminar

Buck Converter Design Basics

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This entry-level topic provides a practical introduction to the design of synchronous buck converters, which are widely used in DC-DC voltage step-down applications. After covering the basics of the buck switching topology and how it achieves output voltage regulation, the white paper provides a step-by-step example to illustrate the design principles and procedure for a $48V_{IN}$-to-$5V_{OUT}$ buck converter implementation. The example covers design parameters, component selection, control-loop compensation, board layout, hardware testing, and experimental results. Using a design calculator helps to streamline and expedite the design effort. The target audience of this topic includes those with little or no power electronics design experience.

Introduction

Buck-converter integrated circuits (ICs) with integrated switches enable high levels of power density and conversion efficiency. They are ubiquitous in end equipment for industrial, automotive, and enterprise applications. In this paper, we will discuss the operating principles of the synchronous buck topology, review the steady-state waveforms, and provide an overview of commonly used control techniques. Outlining several design goals, we provide insight into the design and realization of a buck converter for a typical USB-C application operating from a 48V automotive battery supply and providing a regulated 5V output at 8A rated load. We will touch upon opportunities for optimization, including reduction of conducted and radiated emissions, better thermal performance, and smaller solution size. The principles covered generally extend to buck regulator applications, such as those at higher current levels using a buck controller (with discrete power MOSFETs), or possibly lower currents using a buck module (with integrated power MOSFETs, controller, and inductor).

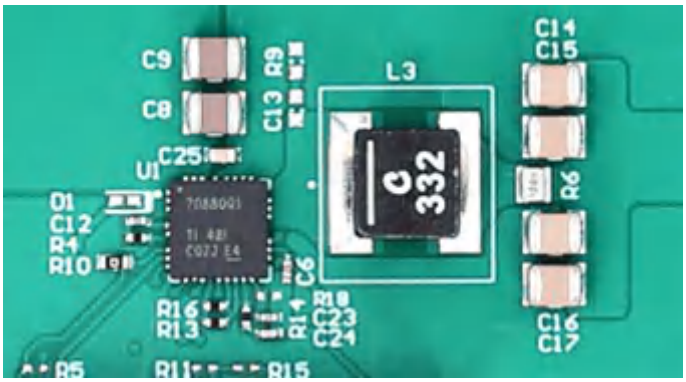


Figure 1. *An example of a buck converter.*

Buck Converter Basics

Design Goals for Power Converters

A common design goal for power converters is to regulate the output voltage. In some applications like LED (light emitting diode) lighting the primary goal may be to regulate the output current, but in most applications the goal is to control the output voltage. A typical output voltage specification would allow ±3% to ±5% deviation in the output voltage under all conditions (for example, load transients) and a steady-state regulation target of ±1%.

There are other common design goals beyond output regulation. These may include high conversion efficiency, low power loss, thermal performance (also considering airflow and heat sinking), small size, low cost, low output voltage ripple and noise, low EMI (electromagnetic interference), high performance (fast response), reliability, and robustness. It

is important to understand the design priorities and make engineering tradeoffs accordingly. For example, some design decisions may result in higher efficiency but slower transient performance. Other design decisions may reduce cost but result in more power loss and thermal challenges.

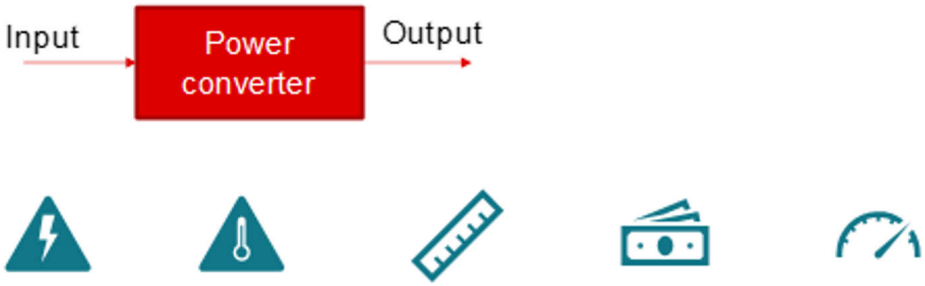


Figure 2. *Considering design goals for a buck converter.*

Linear vs. Switching Regulators

There are two main types of step-down regulators: linear regulators and switching regulators. Linear regulators (also called low-dropout regulators or LDOs), have a series pass element (for example, a MOSFET) between the input and the output (shown in **Figure 3** (a)). The pass element controls the flow of current from the input to the output to regulate the output voltage. Linear regulators are simple, low cost, and low noise. The main drawback of linear regulators is that they can generate a lot of power loss (heat), especially when there is a large voltage conversion ratio and/or large output current.

Switching regulators take a different approach. As the name suggests, they incorporate switches that turn on and off (**Figure 3** (b)). Switching regulators also include passive components like inductors and capacitors for energy storage and filtering. There are numerous converter topologies that can be formed depending on the arrangement of switches and passive components. These topologies include buck (step down), boost (step up), buck-boost (step up or down), and many more.

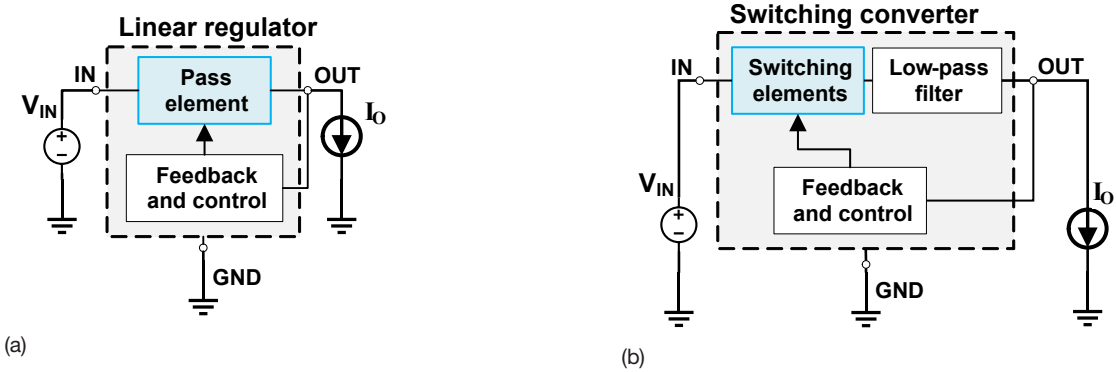


Figure 3. *Simplified blocks diagram of an LDO (a) and a switching regulator (b).*

Switching Regulator Components

An example switching regulator is shown in **Figure 4**. The switches are often MOSFETs but can be diodes, IGBTs, or other semiconductor devices. Gate drive circuits are used to turn the switches on or off. The passive components in this

example include input and output capacitors as well as an inductor. In some topologies transformers are used as well. The control loop can be implemented using an analog or digital control scheme. Controllers include many useful features and typically include the ability to sense voltage, current, and temperature.

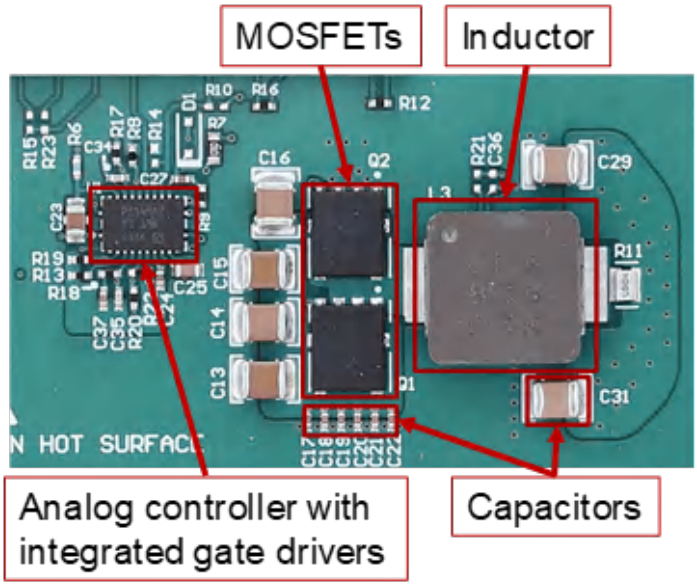


Figure 4. *Components in an example switching regulator, including power MOSFETs, an inductor, input and output capacitors, and an analog controller with integrated drivers.*

Buck Converter Overview

The buck converter is one of the most widely used switching converter topologies. A simplified schematic is shown in **Figure 5**. The high side switch labeled Q_1 and the low side switch is labeled Q_2. The buck topology shown is called a "synchronous" buck because the low side switch Q_2 is a controllable MOSFET versus a "nonsynchronous" buck which would have a diode in place of Q_2. The node between the two switches labeled V_{SW} is the switch node. An inductor L is connected between the switch node and the output voltage V_O. Input capacitors (C_{IN}) and output capacitors (C_O) are connected at the input and output.

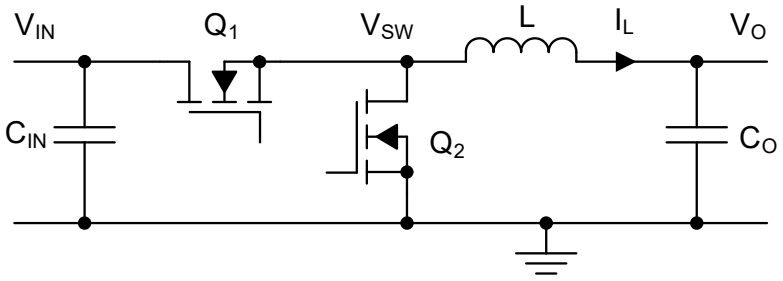


Figure 5. *Circuit schematic of a synchronous buck topology.*

Steady-State Operation

The basic switch states and simplified waveforms are shown in **Figure 6** for a buck converter operating in continuous conduction mode. The switches Q_1 and Q_2 turn ON and OFF in a complementary fashion. When Q_1 is ON, Q_2 is OFF, and when Q_2 is ON, Q_1 is OFF. The switches turn ON and OFF in repeating cycles. The switch node V_{SW} is connected

to V_{IN} when switch Q_1 is ON and the switch node is connected to 0V (often referred to as "ground") when switch Q_2 is ON. The output voltage V_O is lower than the input voltage as intended. There is also a "dead time" included in practical switching circuits (not shown in the diagram) that describes a short period of time when both switches are OFF to enable smooth commutation between the two main switch states.

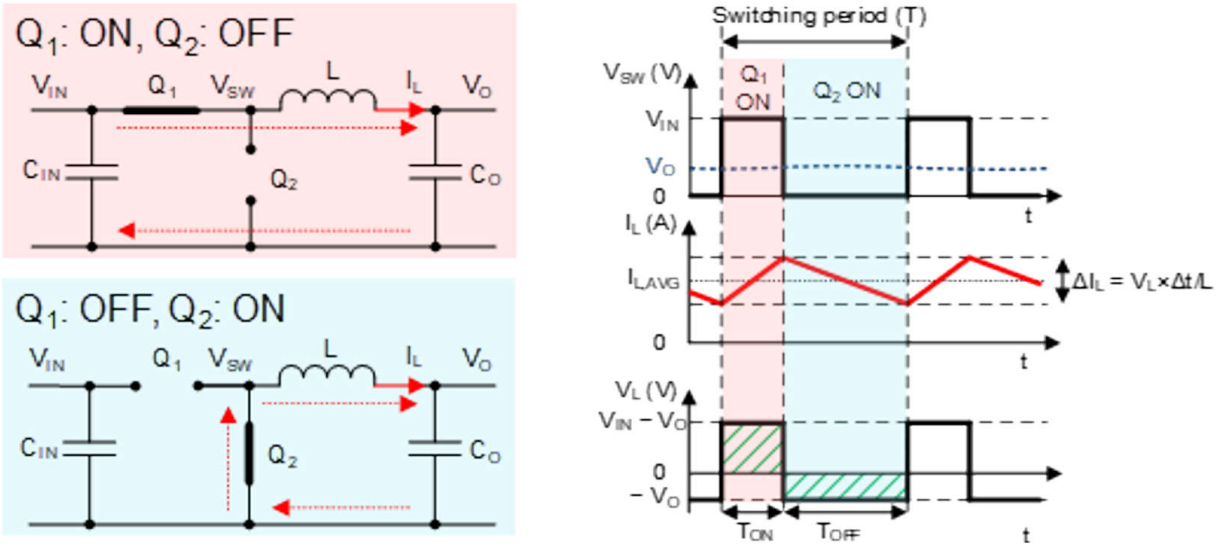


Figure 6. *Operating modes and key waveforms of a buck converter during steady-state operation.*

The inductor current I_L can be approximated by straight lines that increase when Q_1 is ON and decrease when Q_2 is ON. The reason this occurs can be explained by examining the voltage across the inductor drawn as V_L. The inductor voltage is positive when Q_1 is ON and Q_2 is OFF. The inductor voltage is negative when Q_1 is OFF and Q_2 is ON. The input and output voltage ripple is relatively small in comparison to the nominal output voltage, and those voltages are assumed to be constant.

During steady state, the average inductor current will remain constant because the current level at the beginning and end of the cycle are equal. This is the result of the principle of volt-second balance. The inductor voltage multiplied by the time of each portion of the cycle are equal. The equivalent principle for capacitors in steady state is called charge balance.

Effect of Pulse-Width Modulation (PWM)

A simple way to control the operation of a buck converter is to adjust the switch on-times. The high side switch on time can be adjusted to control the conversion ratio of the converter and to regulate the output voltage. This technique is called pulse width modulation (PWM). If the converter's input voltage goes up or down, the switch node pulse width is modulated to maintain output regulation as shown in **Figure 7**. The duty cycle D represents the portion of the switching period that the control switch (the high side switch in a buck converter) is ON. The duty cycle (also called duty ratio) is a number between 0 and 100%. For a buck converter, the voltage conversion ratio $V_O/V_{IN} = D$.

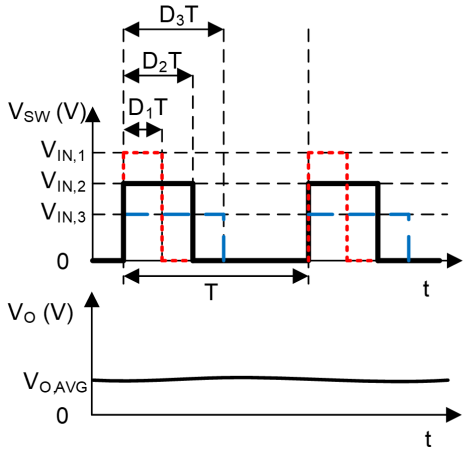


Figure 7. *Effect of duty cycle adjustment by PWM to regulate the output voltage given changes in the input voltage.*

Overview of Control Techniques

Feedback control regulates the output in the presence of changes in the input voltage, output current, temperature, and so forth. Various closed-loop control schemes are used in buck converters. Some common control schemes include voltage mode, current mode, and hysteretic (for example, constant on-time). There are advantages and disadvantages of each control scheme, and a detailed discussion is beyond the scope of this paper. Look at the references at the end of this paper for links to additional resources.

The general structure of a control loop is shown in **Figure 8**. The output voltage is typically measured and passed through a feedback network. This scaled and potentially filtered output voltage measurement is compared to a reference voltage by an error amplifier. The error signal is adjusted by compensation and a control voltage V_C is generated. The control voltage is provided to a pulse width modulator that generates the switch on-time signals. Gate drivers turn the switches ON and OFF according to the desired on-times generated by the pulse width modulator. Measured current information may also be included in the control loop if a form of current mode control is implemented.

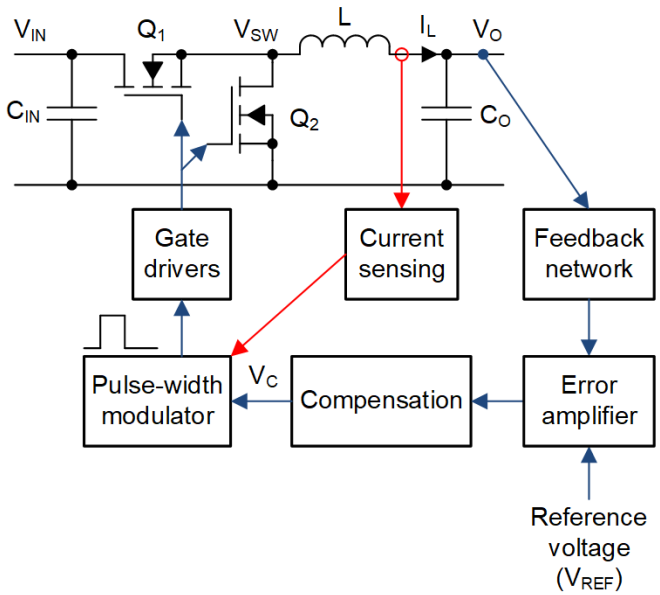


Figure 8. *Block diagram to showcase control techniques for output voltage regulation.*

The typical controller goals are to maximize control loop bandwidth while maintaining sufficient stability margins. The converter's response speed to dynamic changes in load current or other disturbances is directly related to its control loop bandwidth. Faster response leads to less output capacitance needed to maintain output voltage regulation within target limits. Pushing control loop bandwidth too high can result in lower stability margins or an unstable system. Generally, there is a tradeoff made as a result.

Buck Converter Design Example

Let's examine an example to explain the step-by-step process for buck converter design. Numerous potential applications could be considered, but this discussion will focus on generating a 5V intermediate supply rail from a nominal 48V input automotive battery. USB-C chargers in a car are one specific application where this power conversion is needed. The USB ports provide 5V (and other voltage levels) according to the USB-C power delivery standard. Many rear seats have access to multiple USB-C ports as shown in **Figure 9**.



Figure 9. *Rear seat USB-C ports – a typical buck converter application in automotive.*

Design Process Overview

The design process for a buck converter can be summarized as:

1. Understand power requirements
2. Select controller, converter, or module
3. Select switching frequency
4. Select inductor
5. Select capacitors
6. Select modes and features
7. Design control loop compensation
8. Layout circuit board
9. Build and test the design

These are the steps we will follow as we go through the design example for a buck converter. A simplified schematic for the example buck converter is shown in **Figure 10**. The components, features, and design decisions may vary depending on the application and buck solution selected. This may result in some modification of the design process.

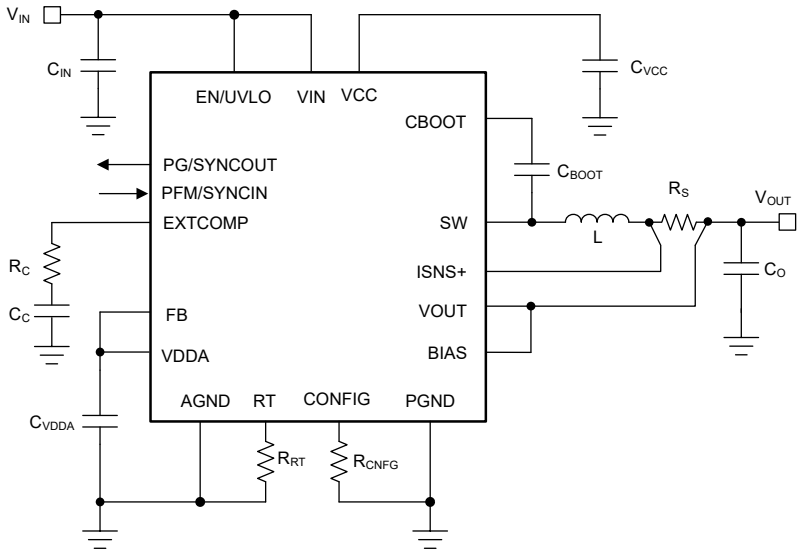


Figure 10. *Simplified schematic of the proposed buck converter with integrated MOSFETs.*

Understand the Power Requirements

The place to start is to understand what is needed in your application. It is important to collect parameters like the input voltage range, output voltage range, and output current, then record them as shown in **Table 1**. In this design example, the input voltage range is fairly large (from 24V to 70V) even though the typical input voltage is 48V. The converter design needs to account for this and be operational across the full input range. Similarly, the design needs to operate over the full temperature range. The typical output current is sometimes called thermal design current (TDC) as it guides the thermal design. The maximum output current is the maximum expected current during normal operation, and the overcurrent protection (OCP) level is higher than that.

Parameter	Min	Typ	Max	Units
Input voltage (V_{IN})	24	48	70	V
Output voltage (V_O), including transients	4.75	5	5.25	V
Output current (I_O)	0	5	8	A
Output overcurrent protection (I_{OCP})		10		A
Soft-start time (t_{SS})		3		ms
Ambient temperature	–40	25	85	°C

Table 1. *Power requirements for buck design example.*

There may be additional important specifications like output ripple, transient response, EMC, and so forth, that can be noted. Beyond the specifications, there are design priorities that impact design decisions. For example, should this design prioritize increasing efficiency or reducing size? Does the design have a cost target? How much flexibility is desired? It is helpful to rank your design priorities and make design tradeoffs and decisions accordingly.

Select a Controller, Converter, or Module Implementation

The next step is to select a buck controller, converter, or module to implement the design. A comparison of options is shown in **Figure 11**. Buck controllers integrate control, protection, interfacing, and various features. They often integrate the gate driver circuits as well. Buck controllers do not include the switches (for example, MOSFETs) or the inductor. Buck converter ICs integrate the control features, gate driver circuits, and the switches (for example, MOSFETs) but

do not include the inductor. The option with the most integration is modules which include the control, switches, and inductor. The converter and modules options may include a small amount of capacitance for input decoupling, bootstrap circuit, and so forth, but it is usually minimal.

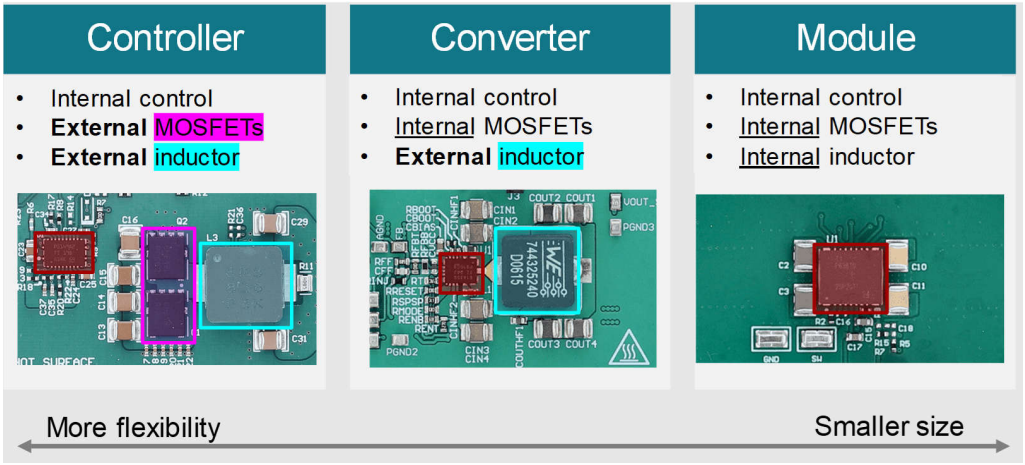


Figure 11. *Comparison of three possible implementations – controller, converter and module – with the IC highlighted in red.*

What are the tradeoffs in selecting one of these options? Controllers typically provide a lot of flexibility. The external MOSFETs can be independently changed when reusing the design for different voltage and current levels. This flexibility can be useful for design reuse. The downside is that controller-based solutions tend to be the largest. Conversely, module implementations are typically the most compact but may be less adaptable. Converter based solutions are somewhat in the middle providing a small solution but with some flexibility. Many converter families have pin-to-pin compatible parts with different current or voltage ratings that can help with scaling the design to be reused elsewhere. Parametric search tables on TI.com help with filtering out the various product offerings and can be used to find the right device for your needs.

Selected Device Overview

The LM70880-Q1 was selected for this design example. It is a synchronous buck converter IC with integrated MOSFETs, rated up to 80V input and 8A output. It has many useful features that can be pin programmed with a resistor or capacitor connected to one of the pins. This device uses a current-mode control scheme that can be compensated using external components or with the default compensation that is internal to the device. This buck converter can operate over the desired temperature range and is automotive qualified. For more details on the device, please see the **LM70880-Q1** product page. In the next several sections of the design example, we will select the components surrounding the IC as shown in **Figure 12**.

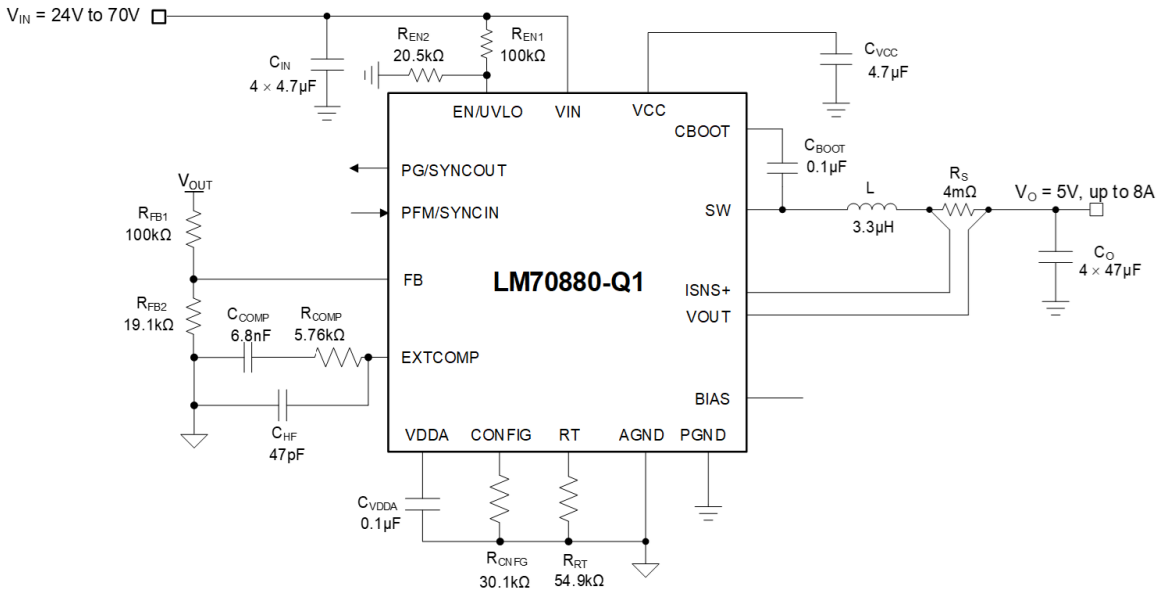


Figure 12. *Full schematic of the 80V, 8A buck converter using the LM70880-Q1.*

Choosing a Switching Frequency

The next design decision is to select the switching frequency, and there are tradeoffs to be made. An estimated efficiency comparison is shown in **Figure 13** for different switching frequencies. Lower switching frequency tends to result in higher conversion efficiency, less heat, and potentially lower EMI/noise. Higher switching frequencies typically result in smaller size, higher loop bandwidth, and potentially lower cost. Generally, select the highest switching frequency that achieves efficiency goals and meets thermal limits. In some automotive applications, the switching frequency is selected to stay out of the AM radio frequency band (540kHz to 1.6MHz) to help meet EMC requirements.

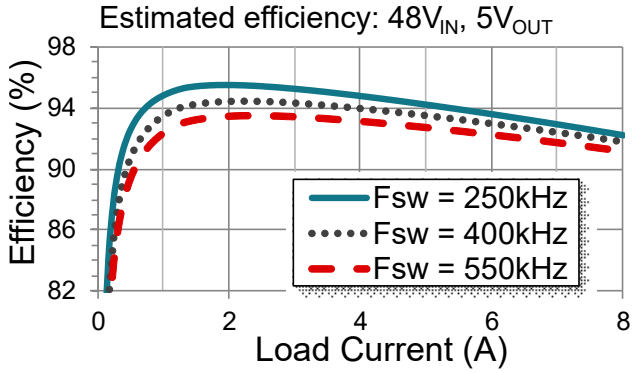


Figure 13. *Efficiency profile versus load with switching frequency as a parameter. VIN is fixed at 48V.*

For this design example, we select 400kHz as the switching frequency. To program this switching frequency, we estimate the R_{RT} resistor using the equation in the datasheet. The equation calculates 54.4kΩ for the resistance so we select the nearest standard resistor value of 54.9kΩ.

Select the Inductor

The next step is to choose an inductor. Inductors are usually the largest single component in a buck converter and have a large impact on efficiency and performance. The inductor current waveform is depicted in **Figure 14**.

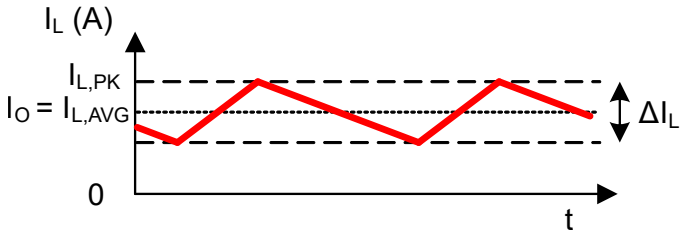


Figure 14. *Waveform of the inductor current waveform showing the triangular ripple amplitude.*

The first thing to estimate is the inductance value using **Equation 1**.

$$L = \frac{V_O}{\Delta I_L \times f_{SW}} \times \left(1 - \frac{V_O}{V_{IN}}\right) \quad (1)$$

where

- L is the inductance
- V_O is the output voltage
- V_{IN} is the input voltage
- ΔI_L is the peak-to-peak inductor current ripple
- f_{SW} is the switching frequency

Common practice is to choose an inductance value such that the inductor current ripple ΔI_L is between 20% and 45% of the full-load output current I_O. This provides a good tradeoff between core loss and winding loss in the inductor. While further adjustments to the value can be made to improve efficiency or transient performance, this is a good starting point. Based on **Equation 1**, the calculated value of inductance is 3.5µH; select 3.3µH since that is the nearest standard value for inductance.

Other important aspects to consider when selecting inductors are DC current rating, power loss, saturation current rating, and saturation profile (hard, soft). Select an inductor where the DC current rating is higher than the thermal design current and where the saturation current rating is higher than the overcurrent protection limit. Inductors with a soft saturating profile have a more gradual reduction in inductance above the saturation current rating compared to hard saturating inductors. The inductor power loss consists primarily of copper winding loss and core loss which can be estimated by **Equation 2** and **Equation 3** respectively.

$$P_{cu} \cong I_{L,RMS}^2 \times DCR \quad (2)$$

where

- $I_{L,RMS}$ is root-mean-square inductor current
- DCR is the inductor winding DC resistance

$$P_{core} \cong K_1 \times f_{SW}^{\alpha} \times \Delta B^{\beta} \quad (3)$$

where

- f_{SW} is the switching frequency

- ΔB is the peak-to-peak flux density
- K_1, α, β, are a constants related to the core material

While these equations are useful for gaining some basic insight into inductor power loss, you usually do not need to model the losses. Most inductor vendors have tools to estimate losses and compare inductors. It is recommended that you leverage these tools in your design and selection process.

Inductor selection can also impact current sensing and slope compensation needs of some buck converters. In this example design, the current-sense resistor R_S is selected to program the overcurrent protection limit I_{OCP} using **Equation 4**.

$$R_S = \frac{V_{CS(TH)}}{I_{OCP} + \frac{\Delta I_L}{2}} \quad (4)$$

where

- $V_{CS(TH)}$ is the current-sense threshold

A current-sense resistor value of 4.2mΩ is calculated from **Equation 4**. Select R_S to be 4mΩ.

Select Capacitors

The next step is to select capacitors. These may be input capacitors, output capacitors, or other capacitors.

Input Capacitors Selection

Input capacitors are selected to meet the input voltage ripple (ΔV_{IN}) needs and high frequency decoupling needs. The input current I_{IN}, input capacitor current I_{CIN}, and high side switch current I_{Q1} are highlighted in **Figure 15** (a). The simplified input capacitor current waveform is shown in **Figure 15** (b).

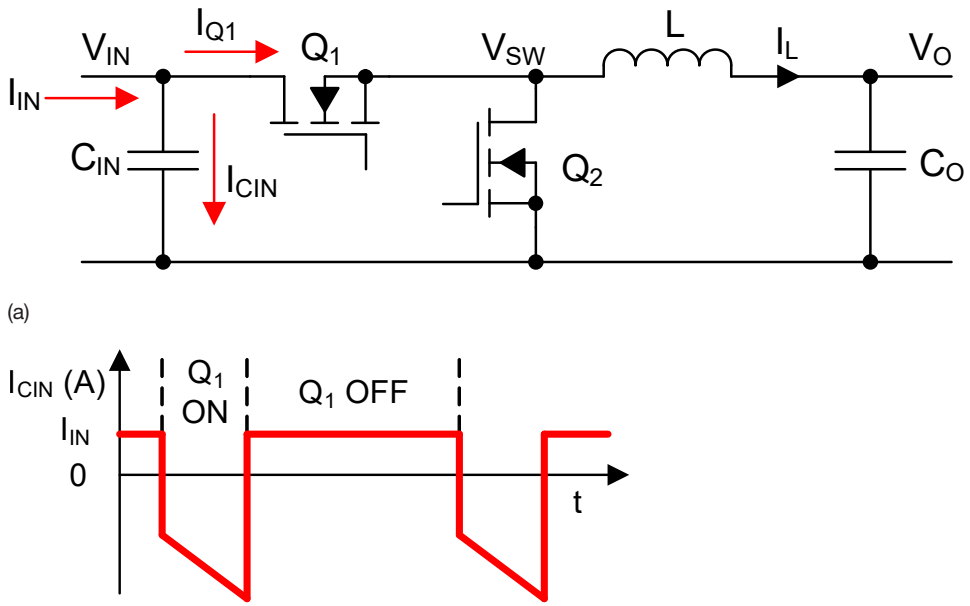


Figure 15. *Currents summing at the input in (a) and the input capacitor current waveform in (b).*

The input capacitance needed can be estimated using **Equation 5**.

$$C_{IN} > \frac{D \times (1 - D) \times I_O}{f_{SW} \times \Delta V_{IN}} \quad (5)$$

where

- C_{IN} is the input capacitance
- ΔV_{IN} is the input voltage ripple
- D is the duty ratio
- I_O is the output current
- f_{SW} is the switching frequency

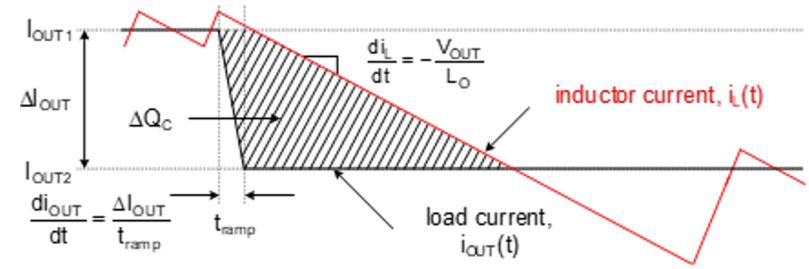
For this design example, we estimate C_{IN} using **Equation 5** to be 6.9µF. In practice, we need more capacitance. Ceramic capacitors commonly used as input capacitors have a reduction in effective capacitance as a DC voltage is applied to them. The capacitance derating with voltage can be as high as 80% reduction from the nominal capacitance. We also need to estimate the input capacitor RMS current to ensure the capacitors can support it. The RMS current can be estimated using **Equation 6** which is 3.25A in this example.

$$I_{CIN,\,RMS} \cong I_O \times \sqrt{D \times (1 - D)} \quad (6)$$

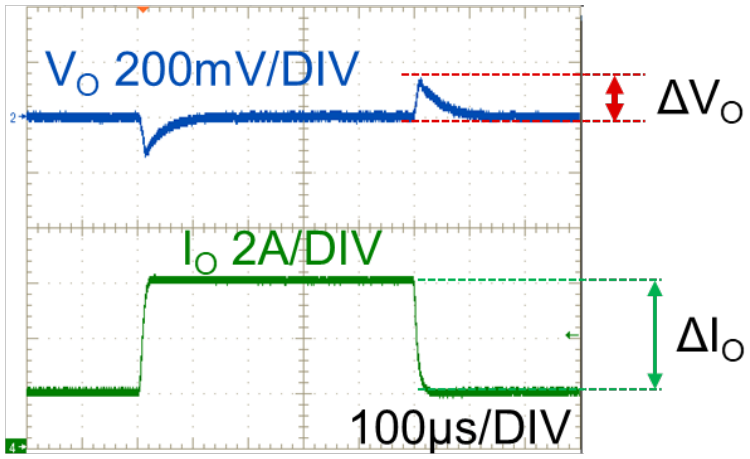
To meet the needs of this example, we select four, 4.7µF and one, 0.1µF capacitors in parallel. The 0.1µF capacitor is a small size, high frequency input decoupling capacitor that is placed as close to the converter input as possible.

Output Capacitors Selection

The output voltage ripple is quite low in steady state. Unless you have a noise sensitive rail that requires very low steady-state ripple, output capacitors are typically selected to meet output voltage limits during dynamic load current changes. The main reason for this is that the load current can change much faster than the inductor current can change as shown in **Figure 16** (a). During a load current transient, the output capacitor provides the difference in current between the output load current and the inductor current. As a result, the output voltage will overshoot or undershoot as shown in **Figure 16** (b).



(a)



(b)

Figure 16. *Currents summing at the input in (a) and the input capacitor current waveform in (b).*

The needed output capacitance can be estimated using **Equation 7**.

$$C_O \geq \frac{\Delta I_O}{2\pi f_C \Delta V_o} = \frac{4A}{2\pi(40kHz)(0.125V)} \quad (7)$$

where

- C_O is the output capacitance
- ΔV_O is the output voltage ripple (deviation) during a load step transient
- ΔI_O is the output load current transient
- f_C is the control loop bandwidth (crossover frequency)

If we assume a loop bandwidth f_C of 1/10th the switching frequency to start and a load step size of 4A, we estimate the needed output capacitance to be 127µF. As before, we should also consider capacitance derating with voltage. We decide to select four, 47µF ceramic capacitors as a result.

Other Capacitors Selection

For the rest of the capacitors used in the example design, we can follow the datasheet recommendations as shown in **Figure 17**. The VCC capacitor forms the bias supply for internal circuitry and gate drivers. The datasheet recommends an X7R ceramic capacitor between 4.7µF and 10µF. The bootstrap capacitor stores charge used to drive the high side

switch. The datasheet recommends a 47nF or higher capacitor. The VDDA capacitor is needed for an internal regulator decoupling; follow the datasheet guideline of 0.1µF.

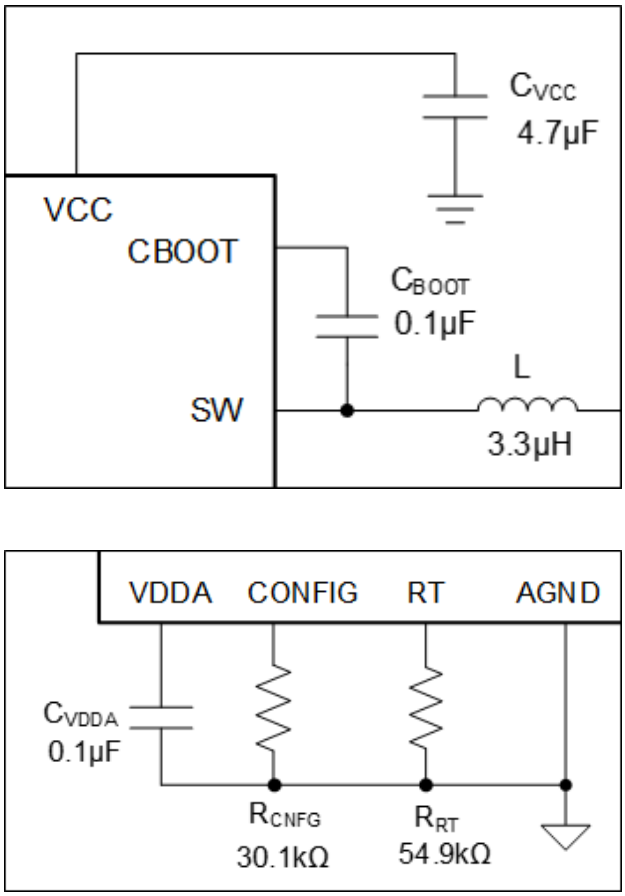


Figure 17. *The VCC and BOOT capacitors (a) and the VDDA capacitor (b) selection can follow datasheet recommendations.*

Select Modes and Features

Next, we will set the output voltage, turn-on and turn-off thresholds, and light-load mode.

Output Voltage Setpoint

The output voltage of buck converters is often set by selecting the external feedback divider resistors. The resistor divider provides a scaled down output voltage measurement that is compared to the internal reference voltage V_{REF} of error amplifier in the buck converter as shown in **Figure 18**. The error amplifier output (COMP) is the control voltage used by the pulse width modulator to set the buck converter switch on times and to regulate the output to the desired value.

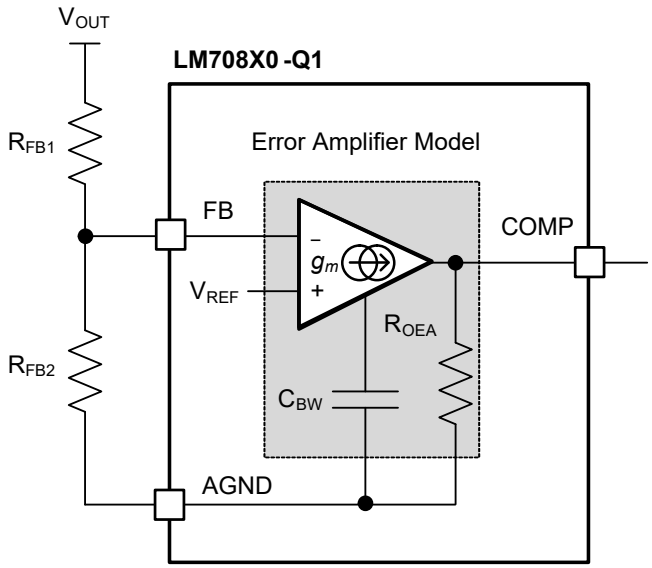


Figure 18. *Feedback resistor values set the output voltage.*

Let's first select the value of the top resistor R_{FB1} to be 100kΩ. This is typically the largest resistor value allowed in the automotive market without coating. Then we calculate the bottom resistor R_{FB2} value using **Equation 8**.

$$R_{FB2} = \frac{R_{FB1}}{\left(\frac{V_{OUT}}{V_{REF}} - 1\right)} \tag{8}$$

where

- V_{REF} is the internal reference voltage
- V_{OUT} is the output voltage

The calculated value is 19.05kΩ. Select the nearest E96 standard resistor value (1% tolerance) of 19.1kΩ.

Many buck converters can set the output voltage by configuring a pin of the device. **Table 2** shows the configuration options for the LM70880-Q1. Several common output voltages are programmable with one resistor or none. This saves a little size, reduces solution cost, and may improve output accuracy with some devices.

FB pin setting	Output voltage
Short to VDDA	3.3V
24.9kΩ to VDDA	5V
49.9kΩ to VDDA	12V
Resistor divider to V_{OUT}	0.8V to 55V

Table 2. *Setting the output voltage by configuring the FB pin of LM70880-Q1.*

Enable Turn ON/OFF

There are several options available for controlling the converter turn ON and OFF. Undervoltage lockout (UVLO) is a common feature that keeps the converter OFF (disabled) when the input voltage is below a certain level. The EN/UVLO pin can be actively pulled high or low (above or below the enable threshold voltage) by external circuits like a sequencer

or microcontroller. Another option is to connect a resistor divider from the input voltage node to the EN/UVLO pin to set input voltage levels at which the converter turns ON/OFF as shown in **Figure 19**.

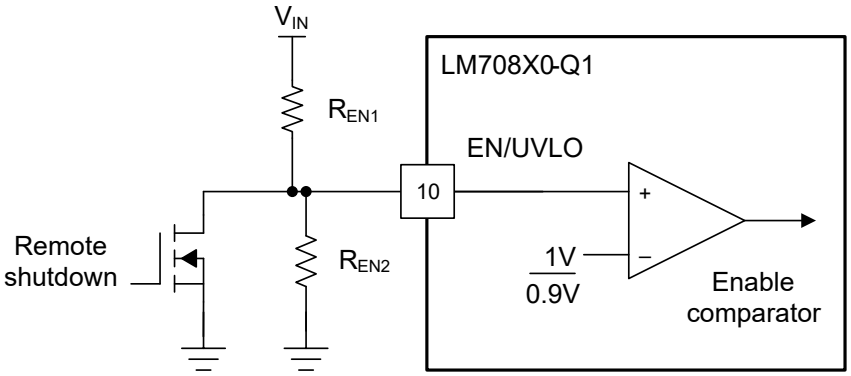


Figure 19. *A resistor divider from the input voltage can set the turn ON/OFF thresholds.*

To set the input voltage turn ON threshold, start by selecting the top resistor R_{EN1} to be 100kΩ. Next, calculate R_{EN2} using **Equation 9**.

$$R_{EN2} = \frac{R_{EN1}}{\left(\frac{V_{IN(on)}}{V_{EN\text{-}TH}} - 1\right)} \tag{9}$$

where

- $V_{IN(on)}$ is the desired input voltage turn ON threshold
- $V_{EN–TH}$ is the enable comparator rising threshold (1V)

In this example, the value for R_{EN2} is calculated to be 20.4kΩ based on a 5.9V input voltage turn ON threshold. Select the nearest E96 resistor value of 20.5kΩ for R_{EN2}. The corresponding input voltage turn OFF threshold is 5.3V.

Light-Load Mode Selection

Many buck converters can change their operating mode under light load conditions. Light load conditions occur when the output current is less than approximately 20% of the full load current. One approach is to operate the converter at a fixed switching frequency with forced pulse-width modulation (FPWM). This mode is essentially the same operation mode as during medium to full load where the high-side and low-side switches are turned on and off in a complementary fashion. Another approach called pulse frequency modulation (PFM) will reduce the switching frequency of the converter under light load conditions and introduces a time interval where neither switch is turned on. The benefit of PFM is shown in **Figure 20**; PFM greatly improves efficiency. These modes can be selected by programming the PFM/SYNCIN pin (connecting it to GND or VDDA pins).

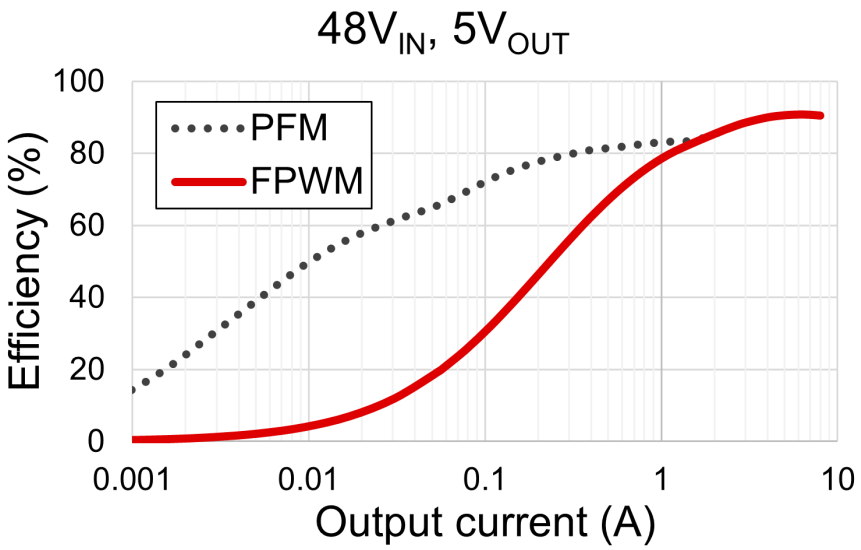


Figure 20. *Efficiency comparison of PFM and FPWM light load modes.*

Control Loop Compensation

Proper design of the control loop is important for stable converter operation. The feedback control loop is shown in **Figure 21** and some noteworthy transfer functions are plotted in a simplified format in **Figure 22**. The control-to-output transfer function (a) $\tilde{v}_{out}(s)/\tilde{v}_c(s)$ describes the behavior of the output of the converter based on the control voltage (V_C). The output-to-control transfer function (b) $\tilde{v}_c(s)/\tilde{v}'_{out}(s)$ describes the behavior of the feedback network, error amplifier, and compensation components. The overall loop gain (c) $\tilde{v}_{out}(s)/\tilde{v}'_{out}(s)$ is the product of the two transfer functions. The design objective is to set the compensation zero and poles to get the desired control loop response. Common design objectives would be to have a closed loop bandwidth (crossover frequency) of around 1/10th of the switching frequency (if the error amplifier can support it), phase margin greater than 45°, and gain margin of greater than 10dB.

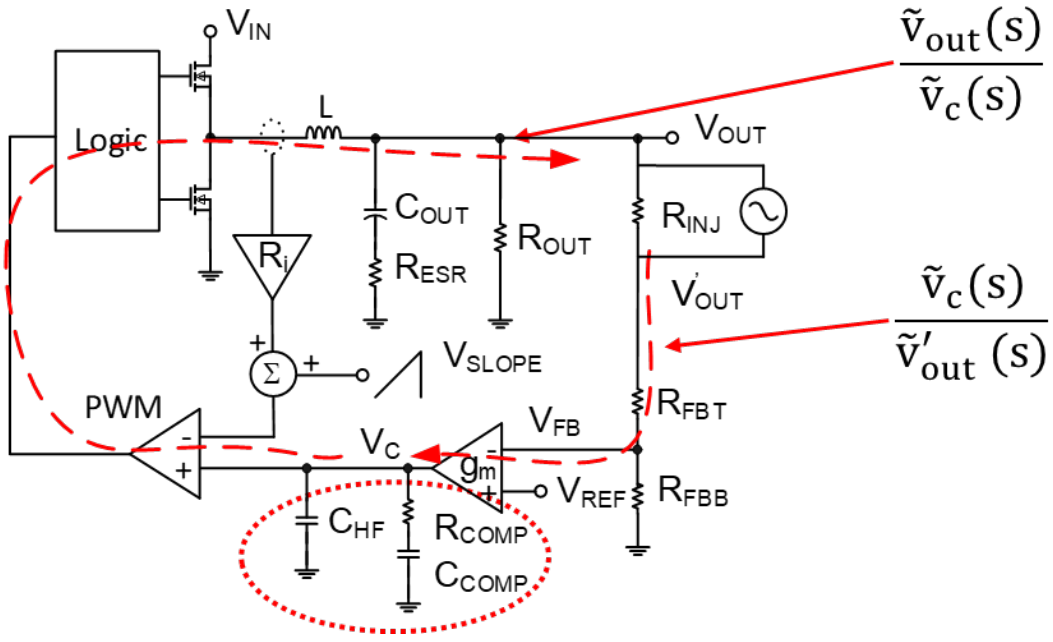


Figure 21. *Feedback control loop overview.*

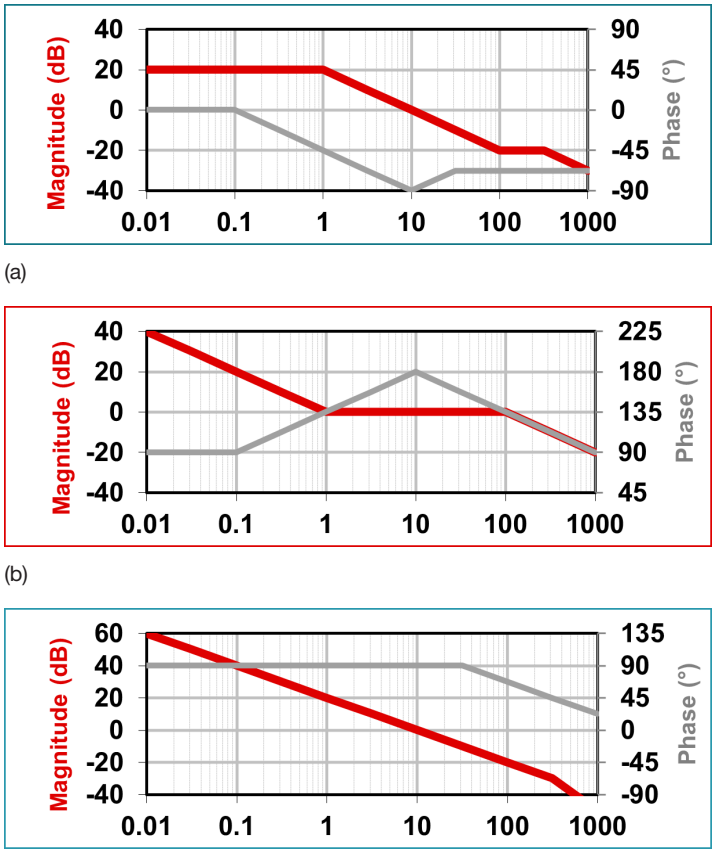


Figure 22. *Control loop transfer functions (a) $\tilde{v}_{out}(s)/\tilde{v}_c(s)$, (b) $\tilde{v}_c(s)/\tilde{v}'_{out}(s)$, and (c) $\tilde{v}_{out}(s)/\tilde{v}'_{out}(s)$.*

In this design example, we will select three compensation components (R_{COMP}, C_{COMP}, and C_{HF}) which are shown in **Figure 23**.

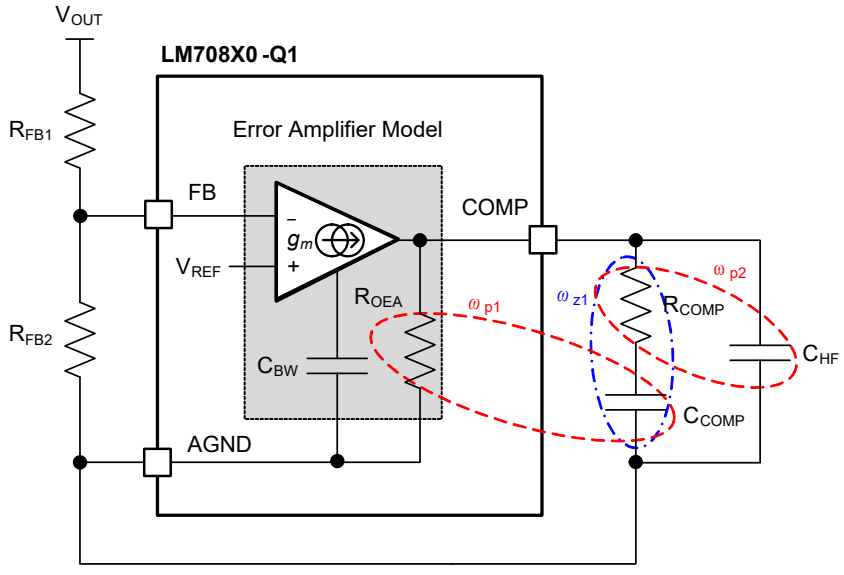


Figure 23. *Control loop compensation components.*

The R_{COMP} resistor sets the mid-band frequency gain and can be estimated using **Equation 10**.

$$R_{COMP} = 2\pi \times f_C \times \frac{V_{OUT}}{V_{REF}} \times \frac{R_S G_{CS}}{g_m} \times C_{OUT} \quad (10)$$

where

- f_C is the desired crossover frequency
- V_{OUT} is the output voltage
- V_{REF} is the internal reference voltage
- R_S is the current sense resistance
- G_{CS} is the current sense gain
- g_m is the transconductance error amplifier gain
- C_{OUT} is the output capacitance

The C_{COMP} capacitor is selected to place a zero in the transfer function at $1/10^{th}$ the crossover frequency or at the load pole. In this example, we choose $1/10^{th}$ of the crossover frequency and estimate the capacitance value using **Equation 11**.

$$C_{COMP} = \frac{10}{2\pi \times f_C \times R_{COMP}} \quad (11)$$

A high-frequency pole is created by C_{HF} to attenuate high-frequency noise. The location of the pole in this design example is at the frequency of the output capacitor ESR zero and can be selected using **Equation 12**.

$$C_{HF} = \frac{1}{2\pi \times f_{ESR} \times R_{COMP}} \quad (12)$$

Utilizing these equations, the selected compensation values are R_{COMP} = 5.76kΩ, C_{COMP} = 6.8nF, and C_{HF} = 55pF. While these design equations from the LM70880-Q1 datasheet are useful, it is recommended to use design tool calculators to simplify the component selection process when they are available. The selected values provide a good starting point for the control loop compensation but may need to be adjusted based on measured results and other optimizations of the design.

Circuit Board Layout

Now that the component selection is complete, let's turn our attention to one of the most important parts of effective converter design: circuit board layout! A schematic that is beautifully designed can be completely ruined by poor layout. One basic challenge is that ideal circuit components do not exist. There are parasitic elements to every component with some examples shown in **Figure 24**. These parasitics can result in noise, instability, ringing, power loss, electromagnetic interference (EMI), and other unwanted effects. Proper layout reduces the negative impact of parasitics.

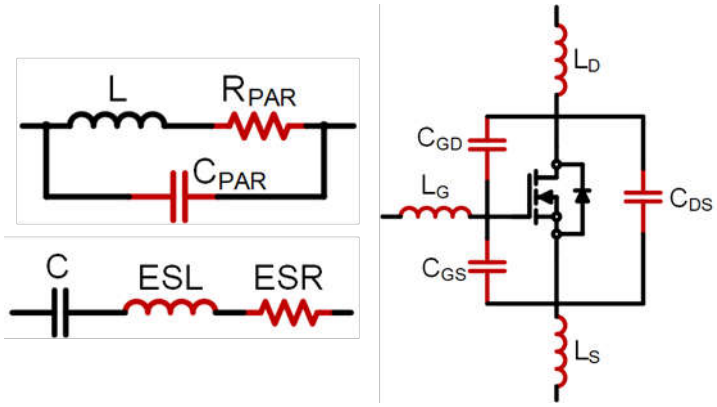


Figure 24. *Non-ideal parasitic elements in real circuit components must be accounted for in design and layout.*

There are layout recommendations and an example layout included in most datasheets. Please review them before making your layout. Some general points are illustrated in **Figure 25**. First, keep the high frequency power loop area small. This reduces parasitic inductance distributed around this high slew-rate current (high di/dt) loop which improves efficiency, reduces switch node ringing, and reduces EMI. Second, keep the switch node (and other high dv/dt nodes) area small to reduce capacitive noise coupling.

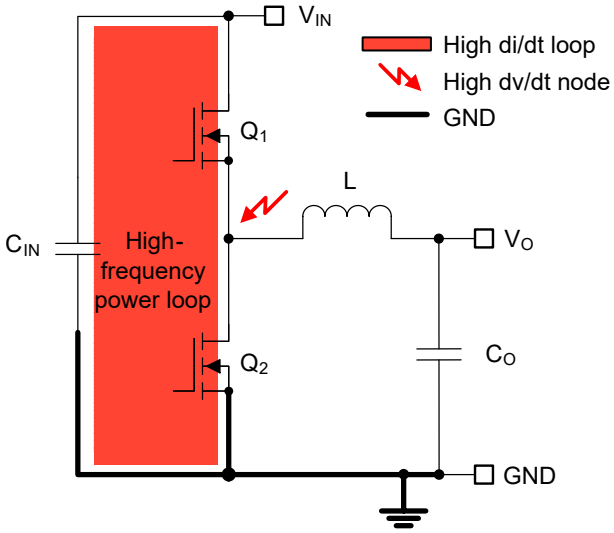


Figure 25. *Key considerations in buck converter layout.*

The example converter layout is shown in **Figure 26**. Notice how the input capacitors are placed right next to the VIN and PGND pins with a small, high frequency capacitor (C25) placed closest. The inductor is located near the SW pin and the area of the SW node is small. The C_{BOOT} capacitor is placed near the CBOOT pin. The feedback resistors are located close to the FB pin. Thermal vias are placed on the VIN and PGND pours to help dissipate heat. The AGND node is connected to the PGND node under the IC. The current sense trace is routed away from noise sources like the SW node.

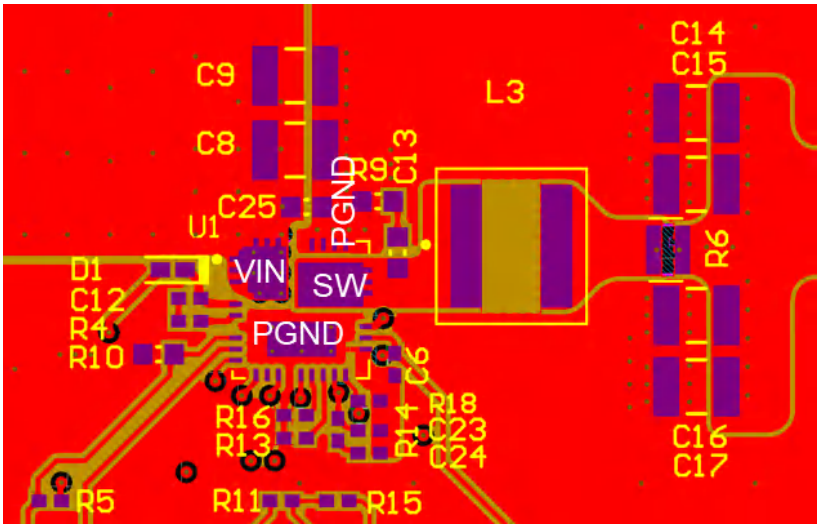


Figure 26. *Example buck converter layout.*

Experimental Validation

The next (and potentially final) step is to build and test the design. Based on the test results, additional refinement, corrections, and optimization of the design may be needed. Before beginning, it is helpful to outline a test plan you will use to evaluate the converter's performance. Some basic tests often conducted are measuring steady-state waveforms, efficiency, stability (for example, bode plot), load transient response, and thermal performance. Other common tests include measuring start-up waveforms, shutdown waveforms, fault response (for example, overcurrent protection), electromagnetic compatibility (EMC), output impedance, output noise spectrum, and no-load standby power. We will focus on a few basic tests in this design example.

Test: Steady-State Waveforms

One of the first functional tests is to measure the output voltage and switch node voltage under steady-state conditions. Steady state is when the converter is operating without any disturbances or changes to the input, output, or some other potential source of change. The intention is to see if the converter operates as expected. Is the output voltage smooth with the expected ripple? Is the switch node behavior consistent or is it operating erratically? These waveforms can be measured using voltage probes and an oscilloscope. Use a short ground lead directly across the measurement location to reduce noise pickup. The voltage probe tip is the positive terminal, and the voltage probe barrel is the negative terminal. **Figure 27** shows the expected steady-stage waveforms of the converter operating with 48V input and 8A output. The output voltage is measured with AC coupling in this case. The DC value can be measured with a multimeter.

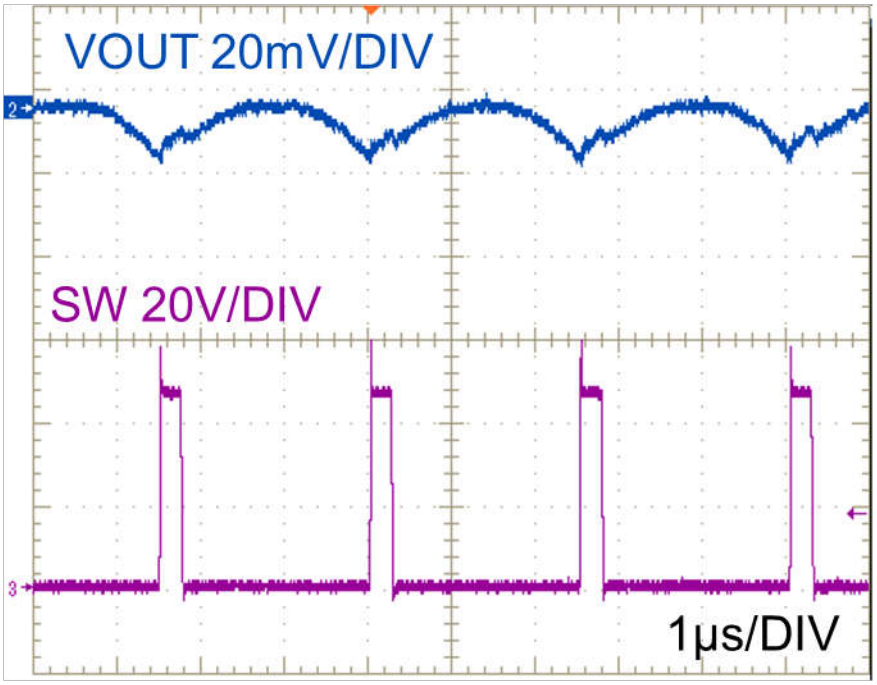


Figure 27. *Example output voltage and switch node steady-state waveforms of the buck converter with 48V input, 8A output.*

Test: Efficiency

Efficiency is a measure of the ratio of output power to input power. The efficiency data is collected by sweeping the output current and measuring the DC values of the input voltage, input current, output voltage, and output current at a particular input voltage. **Figure 28** shows some example results for three different input voltages while operating at room temperature. From the same dataset, the power loss results can also be calculated and plotted. Power loss ends up as heat that is generated and must be dissipated.

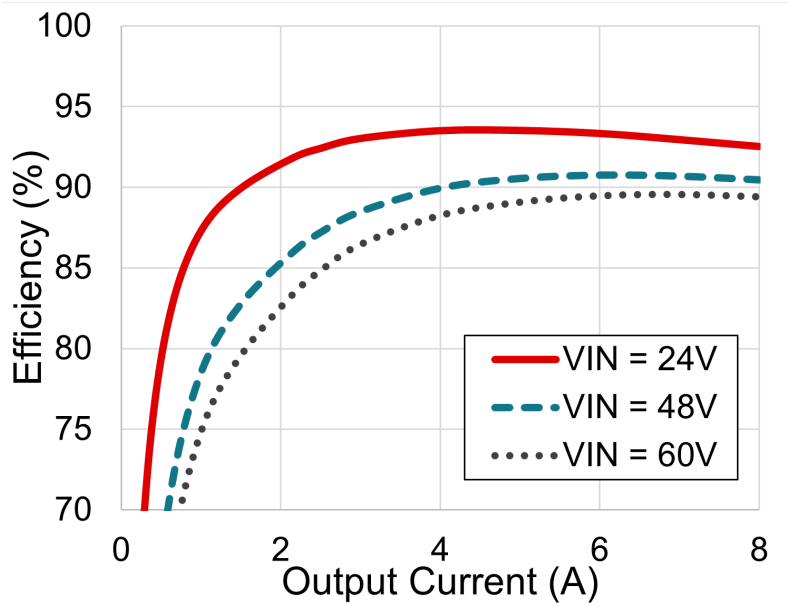


Figure 28. *Example measured efficiency of the buck converter with three different input voltages at room temperature.*

Test: Stability

A common approach to assessing stability of power converters is to measure the loop gain. A low amplitude, AC signal is typically injected into the feedback network to provide a small signal perturbation. The frequency of the injected AC signal is swept over the frequency range of interest and a bode plot is created, as shown in **Figure 29**. The bode plot displays the gain and phase relationship of the injected signal and the output voltage. When the gain curve crosses the 0dB line, this frequency is the crossover frequency (or bandwidth) of the converter's control loop. In this example it is 36kHz. The value of the phase curve at the crossover frequency is the phase margin, which is 66° in this example. Another noteworthy point is when the phase curve crosses 0 degrees; the gain at that frequency is the gain margin, which is –15dB in this example. Common guidelines are to ensure > 45° of phase margin and > 10dB (absolute value) of gain margin under all operating conditions to ensure a stable system. More information on bode plots, see the ***Considerations for Measuring Loop Gain in Power Supplies*** white paper.

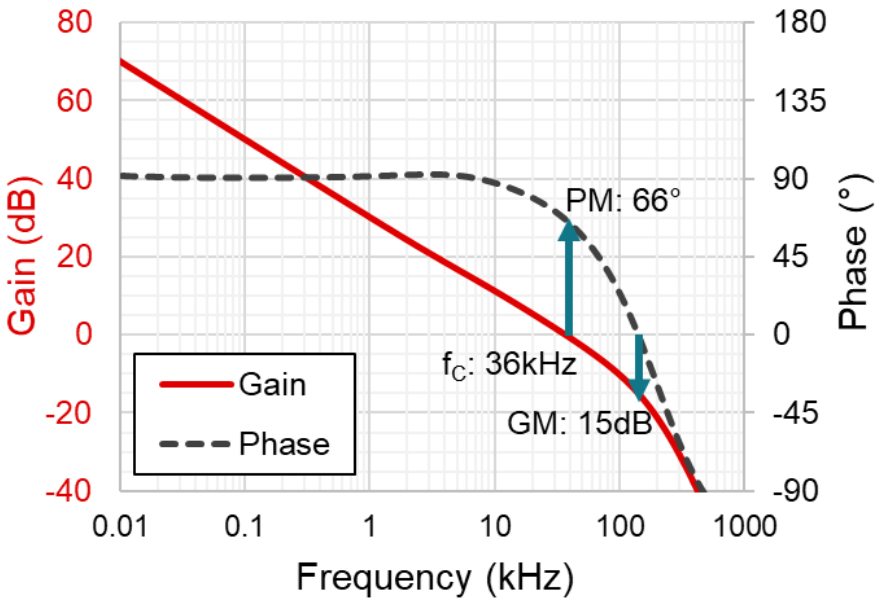


Figure 29. *Example loop gain response of the buck converter shown in a bode plot with 48V input and 8A output.*

Test: Load Transient Response

A load transient test is commonly used to evaluate the time domain response to large signal changes in the output load. A large, quick change in the output current provides a load step. In the example result shown in **Figure 30**, a 25% to 75% rated load current (2A to 6A) is applied with a 1A/µs slew rate. The output voltage is measured (AC coupled). The output deviates by less than 200mV and smoothly comes back to the target output voltage without any ringing. This is the desired and expected response.

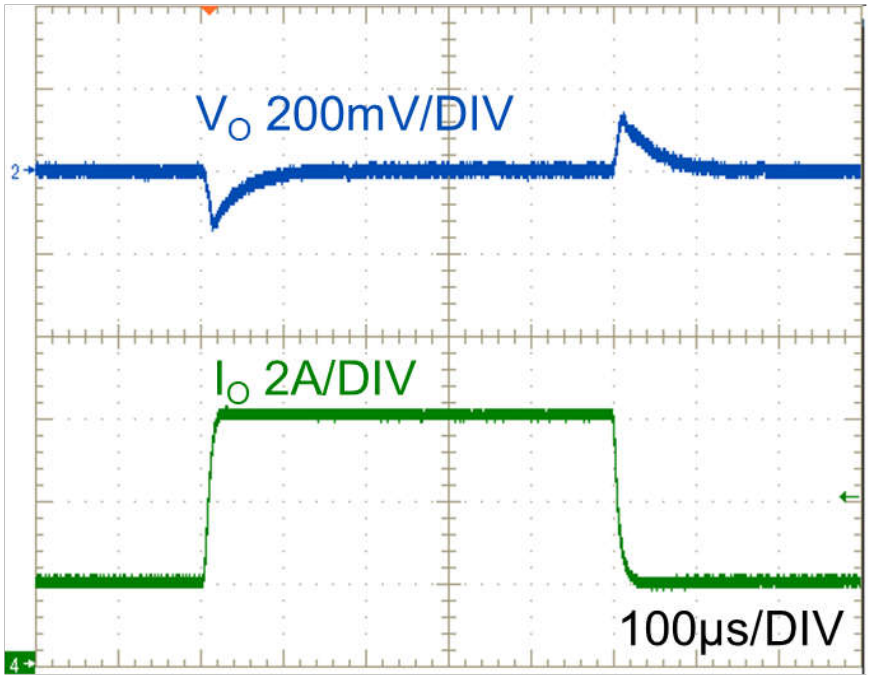


Figure 30. *Example buck converter's measured transient response.*

Conclusion

This white paper is an introductory guide to designing a buck converter. After covering some basics of the buck topology and control, a step-by-step design example showed how to select components, lay out a circuit board, and test the hardware. The intention of this document is to serve as a launching pad for further discovery and experience with designing power converters. Links to additional references are included for readers who want to learn more.

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8. **Power Tips: Calculating Capacitance for Load Transients**
9. **Considerations for Measuring Loop Gain in Power Supplies**
10. **Under the hood of low-voltage DC/DC converters**
11. **Constructing your power supply — layout considerations**
12. **Choosing the right fixed-frequency buck regulator control strategy**
13. **Choosing the right variable frequency buck regulator control strategy**

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