UCC34141-Q1 Automotive 1.5W, 12V V_{IN}, 25V V_{OUT}, High-Density, > 5kV_{RMS}, Isolated DC/DC Module

ADVANCE INFORMATION

1 Features

- Fully integrated high-density isolated DC/DC module with isolation planar transformer
- Wide input range: 5.5V to 28V (with 22V OVLO)
  - ≥ 0.6W typical output for 6V ≤ V_{VIN} ≤ 7V, and ≥ 0.5W for V_{VIN} = 5.5V, at T_A ≤ 85°C
  - ≥ 1.3W typical output for 8V ≤ V_{VIN} ≤ 18V, 18V ≤ $V_{VDD-COM}$ ≤ 20V, at T_A ≤ 85°C
  - ≥ 1.5W typical output for 11V ≤ V_{VIN} ≤ 13V, 18V ≤ $V_{VDD-COM}$ ≤ 20V, at T_A ≤ 85°C
  - ≥1.2W typical output for 11V ≤ V_{VIN} ≤ 13V, 15V ≤ $V_{VDD-COM}$ < 18V, at T_A ≤ 85°C
- Programmable (VDD – COM) output voltage
  - 15V to 20V, ≤ ±1.5% total regulation accuracy
- Programmable (VEE – COM) output voltage
  - -2V to -8V, ≤ ±5% total regulation accuracy
- Adaptive spread spectrum modulation (SSM)
- Strong magnetic and radiated field immunities
- Reduced inrush current soft-start
- ENA pin for logic enable and programming input UVLO
- Open-drain Power-Good for fault indicator
- Integrated protections: UVLO, OVLO, short-circuit, OVP, UVP, and thermal shutdown.
- < 3pF isolation capacitance
- Static and dynamic CMTI > ±250kV/µs
- AEC-Q100 qualified for automotive applications
  - Temperature grade 1:–40°C ≤ T_A ≤ 125°C
- Safety-related certifications (Planned):
  - Reinforced isolation per DIN EN IEC 60747-17 (VDE 0884-17)
  - UL 1577 / CSA component recognition program
- 16-pin, wide body SOIC package

2 Applications

- Hybrid, electric and power train system (EV/HEV)
  - Inverter and motor control
  - On-board (OBC) and wireless charger
  - DC/DC converter
- Grid infrastructure
  - EV charging station power module
  - DC charging (pile) station
  - String inverter
- Industrial transport
  - Off-highway vehicle electric drive
- Power delivery
  - Rack and server power

3 Description

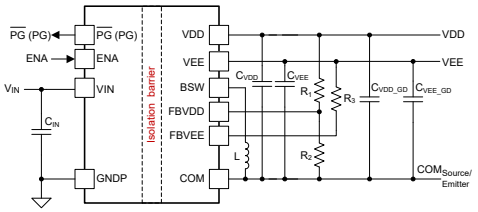
The UCC34141-Q1 is an automotive qualified high isolation voltage DC/DC power module designed to provide power to SiC and IGBT isolated gate drivers. Its proprietary integrated transformer, flip-chip package, and advanced control architectures achieve high power density, low noise, and lowest system BOM. This device is capable of delivering 1.5W typical output power at 85ºC ambient temperature. The highly accurate dual-output voltages, easily set by resistor dividers, enable low on-resistance, fast and reliable switching for SiC/IGBT. The low-latency feedback control reduces the output capacitance for fast load transient and supports dynamic voltage programming. The wide input voltage and adjustable V_{IN} UVLO supports both wide battery voltage of electric vehicles and regulated input rails. It is operational from 5.5V to 20V V_{IN}, and can withstand V_{IN} overvoltage transient up to 28V.

The integrated protection features, fault-report Power-Good pin, and enable function increase system robustness and save external components. The SOIC package with 8.2mm creepage and clearance distance ensures high isolation capability.

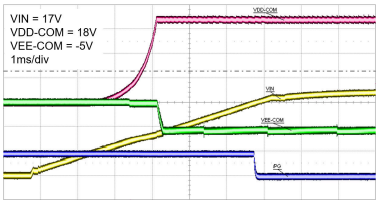
Device Information

ORDERABLE PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
PUCC34141QDHARQ1	DHA (SSOP, 16)	5.85mm × 7.50mm

(1) For all available packages, see Section 11.



Simplified Application



Typical Power-up Sequence

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4 Device Comparison

Table 4-1. Device Comparison Table

DEVICE NAME	V_{VIN} RANGE	OUTPUT (VDD-COM) ADJUSTABLE RANGE	OUTPUT (VEE-COM) ADJUSTABLE RANGE	TYPICAL POWER	POWER-GOOD ACTIVE POLARITY	FAULT RESPONSE
UCC34141-Q1	8V to 20V	18V to 20V	-2V to -8V	1.5W	LOW	LATCH-OFF
		15V to 18V	-2V to -8V	≥1W		
	5.5V to 8V	15V to 20V	-2V to -8V	≥0.3W		
UCC34141D-Q1	8V to 20V	18V to 20V	-2V to -8V	1.5W	HIGH	AUTO-RESTART
		15V to 18V	-2V to -8V	≥1W		
	5.5V to 8V	15V to 20V	-2V to -8V	≥0.3W		

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5 Pin Configuration and Functions

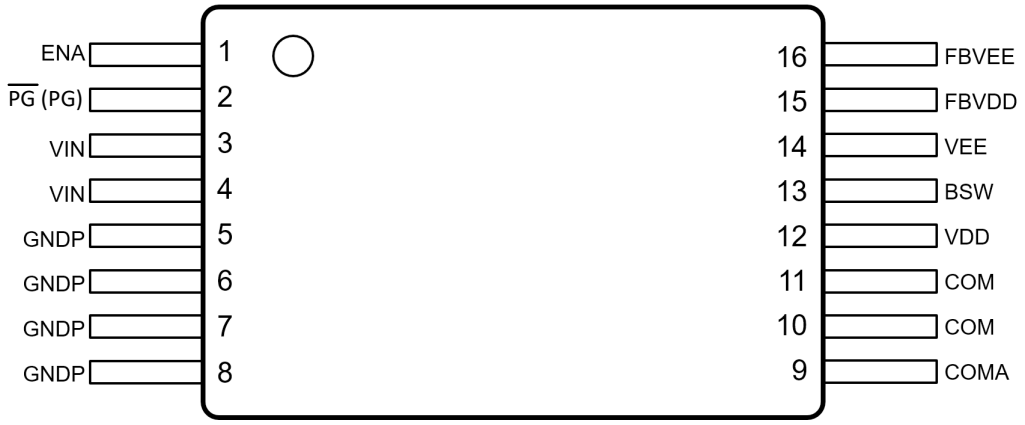

Figure 5-1. DHA Package, 16-Pin SSOP (Top View)

Table 5-1. Pin Functions

PIN		TYPE [1]	DESCRIPTION
NAME	NO.		
ENA	1	I	Enable pin. Forcing ENA LOW disables the device. Pull HIGH to enable normal device functionality. 5.5V recommended maximum. Can be used to program input UVLO with a resistor divider from VIN.
$\overline{PG}$(PG)	2	O	Power-Good open-drain output pin. Remains active when $V_{VIN\_UVLOP} \le V_{VIN} \le V_{VIN\_OVLOP}$; $V_{VDD\_UVP} \le V_{FBVDD} \le V_{VDD\_OVP}$; $V_{VEE\_UVP} \le V_{FBVEE} \le V_{VEE\_OVP}$; $T_{J\_Primary} \le T_{SHUT\_P\_R}$; and $T_{J\_secondary} \le T_{SHUT\_S\_R}$. Connect a decoupling capacitor in 0402 body size for by-passing the high frequency noise. It must be next to the Power-Good pin on the same side of the PCB as the IC.
VIN	3, 4	P	Primary input voltage. Connect a 10µF and a parallel 0.1µF ceramic capacitor from VIN to GNDP. The 0.1µF ceramic capacitor in 0402 body size is for by-passing the high frequency noise and must be next to the VIN and GNDP pins on the same side of the PCB as the IC.
GNDP	5, 6, 7, 8	G	Primary-side ground connection for VIN. Place several vias to copper pours for thermal relief. See the "Layout" section for more details.
COMA	9	G	Secondary-side analog sense reference connection for the noise sensitive analog feedback input FBVDD, and FBVEE. Connect the low-side FBVDD feedback resistor and high frequency decoupling filter capacitors close to the COMA pin and respective feedback pin FBVDD. Connect to secondary-side gate drive voltage reference, COM. Use a single point connection and place the high frequency decoupling ceramic capacitor close to the COMA pin.
COM	10, 11	G	Secondary ground. Connect to Source of power switch.
VDD	12	P	Secondary-side isolated output voltage from transformer. Connect a 10µF and a parallel 0.1µF ceramic capacitor from VDD to COM. The 0.1µF ceramic capacitor in 0402 body size is for bypassing high frequency noise and must be next to the VDD and COM pins.
BSW	13	P	Internal buck-boost converter switch pin. Connect an inductor from this pin to COM. Recommend a 3.3µH to 10µH chip inductor.
VEE	14	P	Secondary-side isolated output voltage for negative rail. Connect a 2.2µF ceramic capacitor from VEE to COM for bypassing high frequency noise.
FBVDD	15	I	Feedback (VDD – COM) output voltage sense pin and to adjust the output (VDD – COM) voltage. Connect a resistor divider from VDD to COMA so that the midpoint is connected to FBVDD. The equivalent FBVDD voltage is regulated at 2.5V with the internal hysteresis control across isolation. Adding a 220pF ceramic capacitor for high frequency decoupling in parallel with the low-side feedback resistor is needed. The 220pF ceramic capacitor for high frequency bypass must be next to the FBVDD and COMA pins on top layer or back layer connected with vias.

Table 5-1. Pin Functions (continued)

PIN		TYPE [1]	DESCRIPTION
NAME	NO.		
FBVEE	16	I	Feedback (COM – VEE) output voltage sense pin used to adjust the output (COM – VEE) voltage. Connect one feedback resistor to VEE to program the (COM – VEE) voltage from 2V to 8V. Connect a 10pF ceramic capacitor from FBVEE to COMA for bypassing high frequency noise. The 10pF ceramic capacitor must be next to the FBVEE pin on top layer or back layer connected with vias.

(1) P = power, G = ground, I = input, O = output

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	TYP	MAX	UNIT
V_{VIN}	VIN to GNDP	–0.3		30	V
V_{ENA}, V_{PG}	ENA, PG to GNDP	–0.3		7	V
$V_{FBVEE-COM}$	FBVEE to COM	-0.3		7	V
$V_{BSW-COM}$	BSW to COM	-10		25.5	V
$V_{BSW-VEE}$	BSW to VEE	-0.7		32	V
$V_{BSW-VEE\_tran}$	BSW to VEE (0.24ns transient)	-2.1		33.4	V
$V_{COM-VEE}$	COM to VEE	-0.3		10	V
$V_{VDD-COM}$, $V_{FBVDD-COM}$	VDD, FBVDD to COM	–0.3		25.5	V
$V_{VDD-VEE}$	VDD to VEE	–0.3		32	V
$P_{OUT\_VDD\_MAX}$	Total output power at T_A=25°C			3	W
T_J	Operating junction temperature range	–40		150	°C
T_{stg}	Storage temperature	–65		150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged-device model (CDM), per AEC Q100-011 Section 7.2	±750	V

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
V_{VIN}	Primary-side input voltage to GNDP during continuous operation	5.5(1)	12	20	V
V_{VIN}	Primary-side input voltage to GNDP during overvoltage transient			28	V
V_{ENA}	Enable to GNDP	0		5.5	V
V_{PG}	Power-Good to GNDP	0		5.5	V
$V_{VDD-COM}$	VDD to COM	15	18	20	V
$V_{VDD-VEE}$	VDD to VEE	15	22	25	V
$V_{COM-VEE}$	COM to VEE	2	4	8	V
T_A	Ambient temperature	–40		125	°C
T_J (2)	Junction temperature	–40		150	°C

(1) See the $V_{VIN\_UVLO\_R}$ and $V_{VIN\_UVLO\_F}$ electrical characteristics for the miminum operational V_{VIN}.
(2) See the (VDD-COM) and (COM-VEE) Load Recommended Operating Area section for maximum rated values across temperature and V_{VIN} conditions for different (VDD-COM) and (COM-VEE) output voltage settings.

6.4 Thermal Information

THERMAL METRIC[1]		DHA (SOIC) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	63.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	32.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	20.1	°C/W
Ψ_{JA}	Junction-to-ambient characterization parameter	47.8	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	20.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	3	°C/W

(1) The thermal resistances (R) are based on JEDEC board, and the characterization parameters (Ψ) are based on the EVM described in the Layout section. For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Insulation Specifications

PARAMETER		TEST CONDITIONS	VALUE	UNIT
General				
CLR	External clearance [1]	Shortest terminal-to-terminal distance through air	> 8.2	mm
CPG	External creepage [1]	Shortest terminal-to-terminal distance across the package surface	> 8.2	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance – transformer power isolation)	> 70	µm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	> 600	V
	Material group	According to IEC 60664-1	I	
	Overvoltage category	Rated mains voltage ≤ 300V_{RMS}	I-IV	
		Rated mains voltage ≤ 600V_{RMS}	I-IV	
		Rated mains voltage ≤ 1000V_{RMS}	I-III	
DIN EN IEC 60747-17 (VDE 0884-17) (Planned Certification Targets) [2]				
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	1700	V_{PK}
V_{IOWM}	Maximum working isolation voltage	AC voltage (sine wave) Time dependent dielectric breakdown (TDDB) test	1202	V_{RMS}
		DC voltage	1700	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t = 60s (qualification); $V_{TEST} = 1.2 \times V_{IOTM}$, t = 1s (100% production)	7071	V_{PK}
V_{IMP}	Maximum impulse voltage [3]	Tested in air, 1.2/50µs waveform per IEC 62368-1	8000	V_{PK}
V_{IOSM}	Maximum surge isolation voltage [3]	$V_{IOSM} \geq 1.3 \times V_{IMP}$; Tested in oil (qualification test), 1.2/50µs waveform per IEC 62368-1	10400	V_{PK}
q_{pd}	Apparent charge [4]	Method a: After I/O safety test subgroup 2/3, $V_{ini} = V_{IOTM}$, t_{ini} = 60s; $V_{pd(m)} = 1.2 \times V_{IORM}$, t_m = 10s	≤ 5	pC
		Method a: After environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, t_{ini} = 60s; $V_{pd(m)} = 1.6 \times V_{IORM}$, t_m = 10s	≤ 5	pC
		Method b1: At routine test (100% production), $V_{ini} = 1.2 \times V_{IOTM}$, t_{ini} = 1s; $V_{pd(m)} = 1.875 \times V_{IORM}$, t_m = 1s	≤ 5	pC
C_{IO}	Barrier capacitance, input to output [5]	V_{IO} = 0.4 sin (2πft), f = 1MHz	< 3	pF
R_{IO}	Isolation resistance, input to output [5]	V_{IO} = 500V, T_A = 25°C	> 10^{12}	Ω
		V_{IO} = 500V, 100°C ≤ T_A ≤ 125°C	> 10^{11}	Ω
		V_{IO} = 500V at T_S = 150°C	> 10^9	Ω
	Pollution degree		2	

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6.5 Insulation Specifications (continued)

PARAMETER		TEST CONDITIONS	VALUE	UNIT
	Climatic category		40/125/21	
UL 1577 (Planned Certification Target)				
V_{ISO}	Withstand isolation voltage	$V_{TEST} = V_{ISO} = 5000V_{RMS}$, t = 60s (qualification); $V_{TEST} = 1.2 \times V_{ISO} = 6000V_{RMS}$, t = 1s (100% production)	5000	V_{RMS}

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed-circuit board are used to help increase these specifications.
(2) This coupler is suitable for *safe electrical insulation* only within the maximum operating ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
(3) Testing is carried out in air to determine the surge immunity of the package. Testing is carried out in oil to determine the intrinsic surge immunity of the isolation barrier.
(4) Apparent charge is electrical discharge caused by a partial discharge (pd).
(5) All pins on each side of the barrier tied together creating a two-terminal device.

6.6 Electrical Characteristics

Over operating temperature range (T_J = –40°C to 150°C), unless otherwise noted. All typical values at T_A = 25°C and V_{VIN} = 12V. External BOM components are listed in the pin description table.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SUPPLY (Primary-side. All voltages with respect to GNDP)						
V_{VIN}	Input voltage range	Primary-side input voltage to GNDP. (VDD-COM)=18V; (COM-VEE)=4V; $P_{VDD-COM}$ = 0.3W; $P_{COM-VEE}$ = 0; T_A=85ºC.	5.5(1)	12	20	V
V_{VIN}	Input voltage range	Primary-side input voltage to GNDP. (VDD-COM)=18V; (COM-VEE)=4V; $P_{VDD-COM}$ = 1.3W; $P_{COM-VEE}$ = 0; T_A=85ºC.	8(1)	12	18	V
I_{VINQ}	VIN quiescent current, disabled	V_{ENA} = 0V; V_{VIN} = 5.5V-20V;			600	µA
I_{VINP_NL}	VIN operating current, enabled, No Load	V_{ENA} = 5V; V_{VIN} = 12V; (VDD-COM) = 18V, (COM-VEE)=4V, regulating; $I_{VDD-COM}$ = $I_{COM-VEE}$ = 0 mA.			12	mA
I_{VINP_FL}	VIN operating current, enabled, Full Load	V_{ENA} = 5V; V_{VIN} = 12V; (VDD-COM) = 18V, (COM-VEE)=4V, regulating; $I_{VDD-COM}$ = 83mA; $I_{COM-VEE}$ =0		250		mA
UVLOP COMPARATOR (Primary-side. All voltages with respect to GNDP)						
$V_{VIN\_UVLO\_R}$	VIN analog undervoltage lockout rising threshold	Analog Comparator Always Active First	4	4.25	4.5	V
$V_{VIN\_UVLO\_F}$	VIN analog undervoltage lockout falling threshold	Analog Comparator Always Active First	3.8	4.04	4.28	V
OVLOP COMPARATOR (Primary-side. All voltages with respect to GNDP)						
$V_{VIN\_OVLO\_R}$	VIN overvoltage lockout rising threshold		21.5	22	22.5	V
$V_{VIN\_OVLO\_F}$	VIN overvoltage lockout falling threshold		20	20.3	20.6	V
TSHUTP THERMAL SHUTDOWN COMPARATOR (Primary-side. All voltages with respect to GNDP)						
$T_{SHUT\_P\_R}$	Primary-side over-temperature shutdown rising threshold		150	165		°C
$T_{SHUT\_P\_HYST}$	Primary-side over-temperature shutdown hysteresis		15	20		°C
ENA INPUT PIN (Primary-side. All voltages with respect to GNDP)						

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6.6 Electrical Characteristics (continued)

Over operating temperature range (T_J = –40°C to 150°C), unless otherwise noted. All typical values at T_A = 25°C and V_{VIN} = 12V. External BOM components are listed in the pin description table.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{ENA_R}	Enable pin rising threshold	Rising edge	1.425	1.5	1.575	V
V_{ENA_F}	Enable pin falling threshold	Falling edge	1.282	1.35	1.418	V
I_{ENA}	Enable Pin Input Current	V_{ENA} = 5.0V		5	10	µA
$t_{ENA\_LO\_RST}$	Minimum period for EN = Low to reset latch off		400			µs
$t_{ENA\_LO\_DLY}$	Minimum period required before EN = Low to reset latch off		200			µs
PG OPEN-DRAIN OUTPUT PIN (Primary-side. All voltages with respect to GNDP)						
V_{PG_L}	PG output-low saturation voltage	Sink Current = 5mA			0.5	V
I_{PG_H}	PG Leakage current	V_{PG} = 5.5V			5	µA
PRIMARY-SIDE SOFT START						
t_{PG_Delay}	Deglitch time during soft start between VDD reaches regulation and Power-Good signal (PG) is issued.		2.7	3	3.3	ms
Primary-side Control (All voltages with respect to GNDP)						
f_{SW}	Switching frequency	V_{VIN} = 12V; V_{ENA} = 5V; (VDD-COM)=18V, (COM-VEE)=4V		16.5		MHz
t_{SSTO}	Primary-side soft-start time-out	Timer begins when VIN > UVLOP and ENA = High and reset when Power-Good pin indicates Good		32		ms
(VDD-COM) OUTPUT VOLTAGE (Secondary-side)						
V_{VDD}	(VDD – COM) output voltage range		15	18	20	V
V_{VDD_REG}	(VDD – COM) output voltage DC regulation accuracy	Secondary-side (VDD – COM) output voltage accuracy at FBVDD, over load, line and temperature range, externally adjust with external resistor divider, within SOA range.	-1.45		1.45	%
(VDD-COM) REGULATION HYSTERETIC COMPARATOR (Secondary-side)						
V_{FBVDD_REF}	Feedback regulation reference voltage rising threshold for (VDD – COM)		2.473	2.51	2.547	
V_{FBVDD_HYST}	(VDD-COM) hysteresis comparator hysteresis settings. Hysteresis at the FBVDD pin. The value represents peak-to-peak magnitude.		18	20	22	mV
(COM-VEE) REGULATION HYSTERETIC COMPARATOR (Secondary-side)						
V_{FBVEE_HYST}	(COM-VEE) hysteresis comparator settings. Hysteresis at the FBVEE pin. The value represents peak-to-peak magnitude.	Hysteresis Setting	50	60	70	mV
(VDD-COM) UVLOs COMPARATOR (Secondary-side)						
$V_{VDD\_UVLOS\_R}$	(VDD – COM) undervoltage lockout rising threshold	Voltage from VDD to COM, rising	3.2	3.45	3.7	V
$V_{VDD\_UVLOS\_F}$	(VDD – COM) undervoltage lockout falling threshold	Voltage from VDD to COM, falling	3	3.25	3.5	V
(VDD-COM) OVLOs COMPARATOR (Secondary-side)						
$V_{VDD\_OVLOS\_R}$	(VDD – COM) over-voltage lockout rising threshold	Voltage from VDD to COM, rising	22.5	23	23.5	V

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6.6 Electrical Characteristics (continued)

Over operating temperature range (T_J = –40°C to 150°C), unless otherwise noted. All typical values at T_A = 25°C and V_{VIN} = 12V. External BOM components are listed in the pin description table.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{VDD\_OVLOS\_F}$	(VDD – COM) over-voltage lockout falling threshold	Voltage from VDD to COM, falling	21.7	22.2	22.7	V
(VDD-COM) UVP, UNDER -VOLTAGE PROTECTION COMPARATOR (Secondary-side)						
$V_{VDD\_UVP\_R}$	(VDD – COM) under-voltage protection rising threshold, V_{UVP} = V_{REF} × 90%	At FBVDD	2.175	2.25	2.35	V
$V_{VDD\_UVP\_HYST}$	(VDD – COM) under-voltage protection hysteresis	At FBVDD		22		mV
(VDD-COM) OVP, OVER-VOLTAGE PROTECTION COMPARATOR (Secondary-side)						
$V_{VDD\_OVP\_R}$	(VDD – COM) over-voltage protection rising threshold, V_{OVP} = V_{REF} ×110%	At FBVDD	2.7	2.75	2.825	V
$V_{VDD\_OVP\_HYST}$	(VDD – COM) over-voltage protection hysteresis	At FBVDD		23		mV
(COM-VEE) Buck-Boost Converter (Secondary Side)						
V_{VEE_REG}	(COM-VEE) regulation accuracy	COM-VEE=2V, with 1% feedback resistance accuracy			7.5	%
		COM-VEE=3V, 4V, 5V, with 1% feedback resistance accuracy			4.5	%
		COM-VEE=6V, 7V, 8V, with 1% feedback resistance accuracy			6.5	%
$V_{VEE\_OVLOS\_R}$	(COM-VEE) over-voltage lockout rising threshold	Voltage from COM to VEE, rising	8.8	9	9.2	V
$V_{VEE\_OVLOS\_F}$	(COM-VEE) over-voltage lockout falling threshold	Voltage from COM to VEE, falling	8.4	8.6	8.8	V
f_{SW_VEE}	Switching frequency of VEE converter	VDD-COM=18V, COM-VEE=4V, 3.3uH external inductor		3.2		MHz
I_{LIM}	Buck boost inductor current limit, out of BSW pin	Max current limit without VDD feedforward	0.235	0.261	0.287	A
I_{LIM}	Buck boost inductor current limit, out of BSW pin	VDD-COM=18V	0.127	0.141	0.155	A
t_{VEE_SSTO}	Timeout threshold to determine if the VEE soft start is succesful		1.3	1.6	2	ms
(COM-VEE) UVP, UNDER -VOLTAGE PROTECTION COMPARATOR (Secondary-side)						
$V_{VEE\_UVP\_F}$	(COM – VEE) under-voltage protection falling threshold	COM-VEE=2V		83		%
		COM-VEE=5V		90		%
		COM-VEE=8V		92		%
$V_{VEE\_UVP\_HYST}$	(COM – VEE) under-voltage protection hysteresis	COM-VEE=5V		85		mV
(COM-VEE) OVP, OVER-VOLTAGE PROTECTION COMPARATOR (Secondary-side)						
$V_{VEE\_OVP\_R}$	(COM – VEE) over-voltage protection rising threshold	COM-VEE=2V		117		%
		COM-VEE=5V		110		%
		COM-VEE=8V		108		%
$V_{VEE\_OVP\_HYST}$	(COM – VEE) over-voltage protection hysteresis	COM-VEE=5V		84		mV
TSHUTS THERMAL SHUTDOWN COMPARATOR (Secondary-side)						
$T_{SHUT\_S\_R}$	Secondary -side over-temperature shutdown rising threshold		150	165		°C
$T_{SHUT\_S\_HYST}$	Secondary-side over-temperature shutdown hysteresis		15	20		°C

ADVANCE INFORMATION

6.6 Electrical Characteristics (continued)

Over operating temperature range (T_J = –40°C to 150°C), unless otherwise noted. All typical values at T_A = 25°C and V_{VIN} = 12V. External BOM components are listed in the pin description table.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CMTI (Common Mode Transient Immunity)						
CMTI	Common Mode Transient Immunity	Positive COM with respect to GNDP	250			V/ns
		Negative COM with respect to GNDP			-250	V/ns
INTEGRATED TRANSFORMER						
N	Transformer effective turns ratio	Secondary side to primary side		2.43		

(1) See the $V_{VIN\_UVLO\_R}$ and $V_{VIN\_UVLO\_F}$ electrical characteristics for the miminum operational V_{VIN}.

6.7 Safety-Related Certifications

VDE	UL
Plan to certify according to DIN EN IEC 60747-17 (VDE 0884-17)	Plan to certify under UL 1577 / CSA Component Recognition Program
Certificate planned	Certificate planned

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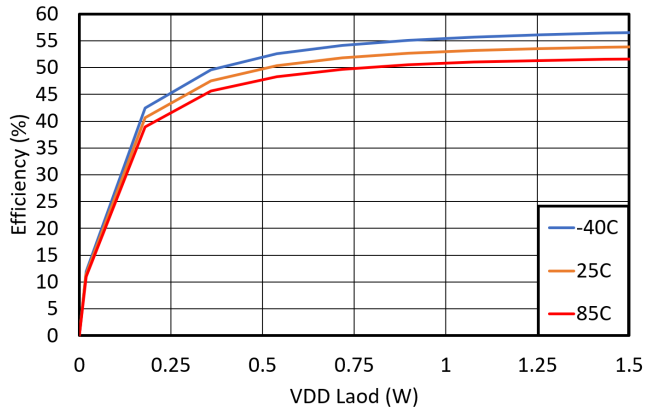
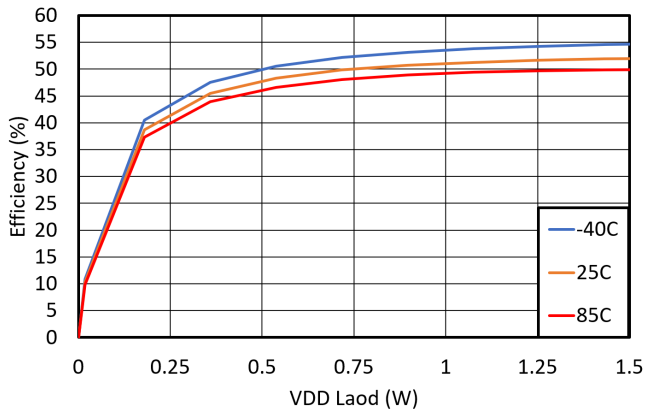
6.8 Typical Characteristics

As shown in Figure 6-4, Figure 6-5, Figure 6-6, and Figure 6-7, the VDD-COM maximum recommended average power safe operating area (SOA) at each V_{IN} is determined by the lower value of the 3W limit (dotted line) and the corresponding thermal derating curve (solid line) at that input voltage. It is not recommended to operate at an ambient temperatures higher than 125ºC. As shown in the Electrical Characteristics table, the typical T_{SHUT} value is 165ºC, and minimal T_{SHUT} value is 150ºC. The SOA derating curves with T_{SHUT} = 150ºC are provided below. The thermal derating power is acquired with the EVM shown in the "Layout" section. The total power requirement in the application can be calculated by the last row of "design requirements"section of the Excel calculator tool, as another design supporting doucment besides this datasheet.



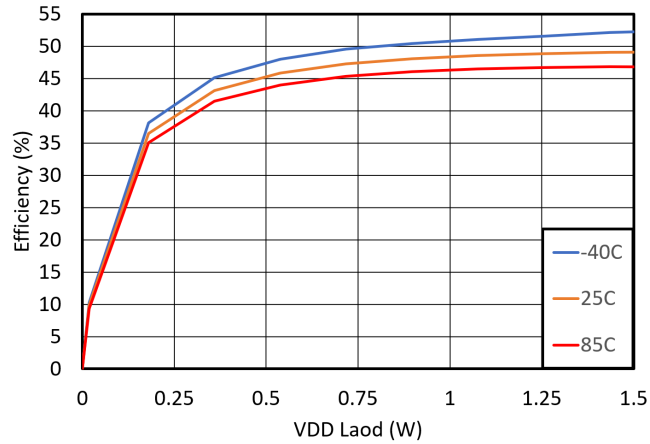
V_{IN} = 12V $V_{VDD-COM}$ = 18V $V_{COM-VEE}$ = 5V
No Load on $V_{COM-VEE}$

Figure 6-1. Efficiency vs. Load on $V_{VDD-COM}$



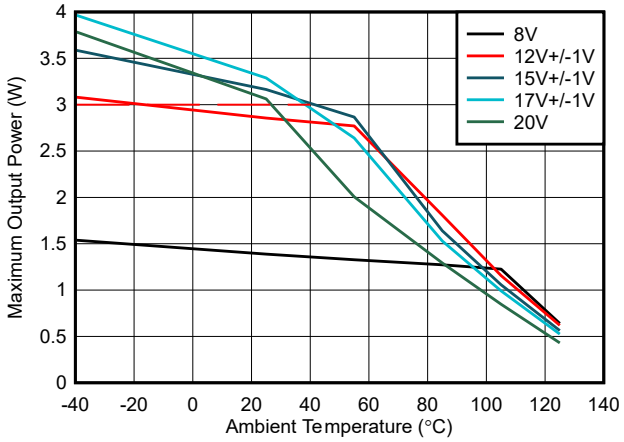
V_{IN} = 15V $V_{VDD-COM}$ = 18V $V_{COM-VEE}$ = 5V
No Load on $V_{COM-VEE}$

Figure 6-2. Efficiency vs. Load on $V_{VDD-COM}$



V_{IN} = 17V $V_{VDD-COM}$ = 18V $V_{COM-VEE}$ = 5V
No Load on $V_{COM-VEE}$

Figure 6-3. Efficiency vs. Load on $V_{VDD-COM}$

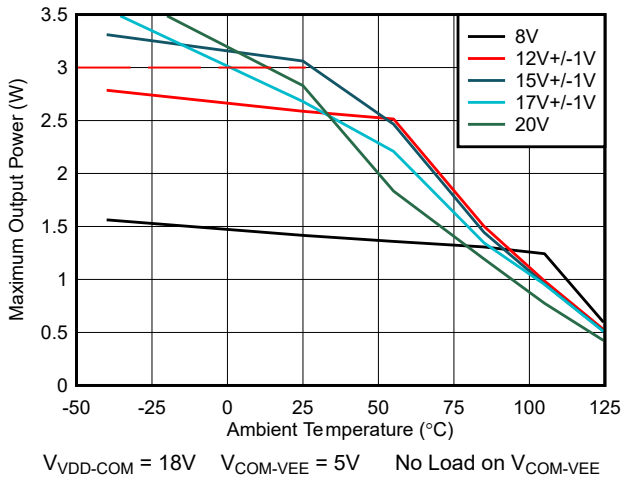


$V_{VDD-COM}$ = 20V $V_{COM-VEE}$ = 5V No Load on $V_{COM-VEE}$

Figure 6-4. SOA Derating Curves for Pre-regulated Input Voltages

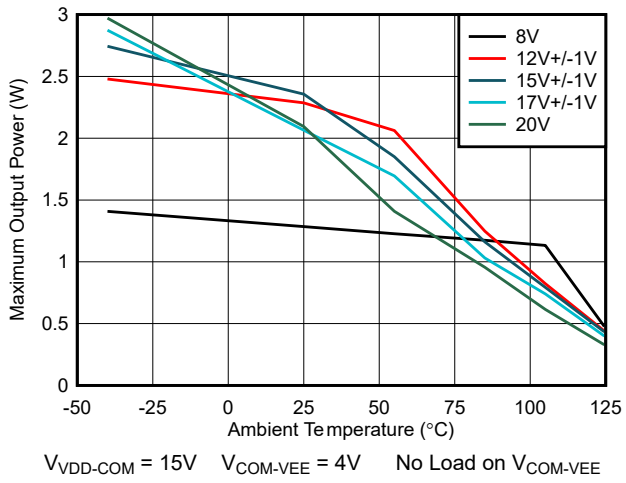
6.8 Typical Characteristics (continued)

As shown in Figure 6-4, Figure 6-5, Figure 6-6, and Figure 6-7, the VDD-COM maximum recommended average power safe operating area (SOA) at each V_{IN} is determined by the lower value of the 3W limit (dotted line) and the corresponding thermal derating curve (solid line) at that input voltage. It is not recommended to operate at an ambient temperatures higher than 125ºC. As shown in the Electrical Characteristics table, the typical T_{SHUT} value is 165ºC, and minimal T_{SHUT} value is 150ºC. The SOA derating curves with T_{SHUT} = 150ºC are provided below. The thermal derating power is acquired with the EVM shown in the "Layout" section. The total power requirement in the application can be calculated by the last row of "design requirements"section of the Excel calculator tool, as another design supporting doucment besides this datasheet.



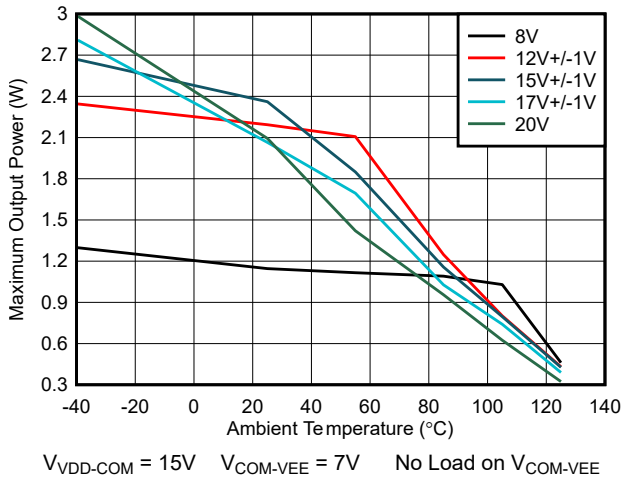
$V_{VDD-COM}$ = 18V $V_{COM-VEE}$ = 5V No Load on $V_{COM-VEE}$

Figure 6-5. SOA Derating Curves for Pre-regulated Input Voltages



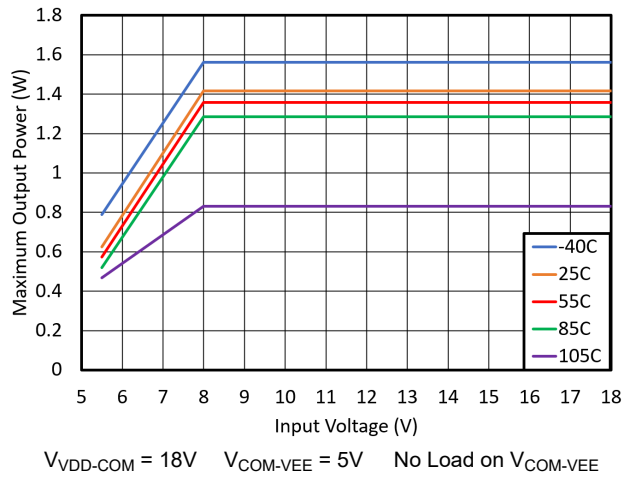
$V_{VDD-COM}$ = 15V $V_{COM-VEE}$ = 4V No Load on $V_{COM-VEE}$

Figure 6-6. SOA Derating Curves for Pre-regulated Input Voltages



$V_{VDD-COM}$ = 15V $V_{COM-VEE}$ = 7V No Load on $V_{COM-VEE}$

Figure 6-7. SOA Derating Curves for Pre-regulated Input Voltages



$V_{VDD-COM}$ = 18V $V_{COM-VEE}$ = 5V No Load on $V_{COM-VEE}$

Figure 6-8. SOA Derating Curves with Wide Input Voltage for Direct Battery Connection

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7 Detailed Description

7.1 Overview

The UCC34141-Q1 device is suitable for applications that have limited board space and require more integration. It is also suitable for very-high voltage applications, where power transformers meeting the required isolation specifications are bulky and expensive. The low-profile, low-center of gravity, and low weight provides a higher vibration tolerance than systems using large bulky transformers. The device is easy-to-use and provides flexibility to adjust both positive and negative output voltages as needed when optimizing the gate voltage for maximum efficiency while also protecting gate oxide from over-stress with its tight voltage regulation accuracy.

The device integrates a high-efficiency, low-emissions, isolated DC/DC converter for powering the gate drive of SiC or IGBT power devices in traction inverter motor drives, on-board-charger (OBC), server telecom rectifiers, industrial motor drives, or other high voltage DC/DC converters. This DC/DC converter can provide greater than 1.5W of power.

The integrated DC/DC converter uses switched mode operation and proprietary circuit techniques to reduce power losses and boost efficiency. Specialized control mechanisms, clocking schemes, and the use of an on-chip transformer provide high efficiency and low radiated emissions.

The integrated transformer provides power delivery throughout a wide temperature range while maintaining a $5000V_{RMS}$ isolation, and an $1202V_{RMS}$ continuous working voltage. The low isolation capacitance of the transformer provides high CMTI allowing fast dv/dt switching and higher switching frequencies, while emitting less noise.

The VIN supply is provided to the primary-side power controller that switches the input stage connected to the integrated transformer. Power is transferred to the secondary-side output stage, and regulated to a level set by the resistor divider connected between the VDD pin and the FBVDD pin with respect to the COMA pin. The output voltage is adjustable with external resistor divider allowing a wide (VDD – COM) range.

For optimal performance ensure to maintain the V_{VIN} input voltage within the recommended operating voltage range. Do not exceed the absolute maximum voltage rating to avoid over-stressing the input pins.

A fast hysteretic feedback burst control loop monitors (VDD – COM) and ensures the output voltage is kept within the hysteresis with low overshoot and undershoot during load and line transients. The burst control loop enables efficient operation across full load and allows a wide output voltage adjustability throughout the whole V_{VIN} range. The undervoltage lockout (UVLO) protection monitors the input voltage pin, VIN, with hysteresis and input filter ensuring robust system performance under noisy conditions. The overvoltage lockout (OVLO) protection monitors the input voltage pin, VIN, to protect against over-voltage stress by disabling switching and reducing the internal peak voltage. Controlled soft-start timing, provided throughout the full power-up time, limits the peak input inrush current while charging the output capacitor and load.

The UCC34141-Q1 can also provide a second output rail, (COM – VEE), that is used as a negative bias for the gate drivers allowing quicker turn-off switching for the IGBTs and also to protect from unwanted turn-on during fast switching of SiC devices. (COM – VEE) has a simple yet fast and efficient bias controller to ensure the positive and negative rails are regulated during the PWM switching. In this case, COM pin is used as the common reference point. The COM pin connects to the source of SiC device or emitter of an IGBT device.

A fault protection and Power-Good status pin provides a mechanism for the host controller to monitor the status of the DC/DC converter and provide proper sequencing of power and PWM control signals to the gate driver. Fault protection includes undervoltage, overvoltage, over-temperature shutdown, and isolated channel communication interface watchdog timer.

A typical soft-start ramp-up time is lower than t_{SSTO}, and varies based on input voltage, output voltage, output capacitance, and load. If either output is shorted or over-loaded, the device will not be able to power-up within the t_{SSTO} soft-start time, so the device will shut down. The fault response of the device varies based on the part number as listed in Table 4-1. For latch-off operation, the device will shut down and latches-off for protection and can be reset by toggling the ENA pin or resetting V_{VIN}. For auto-restart operation the device shuts down and an auto-restart timer of $t_{RESTART}$ will start afterwords, and then the part will attempt to auto-restart after that

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timer expires. If the fault has been removed, the part will soft-start to regulation successfullly. If the fault condition remains, the part will shut down again and attempt another auto-restart. The device can continuously operate safely in hiccup mode as long as the fault occurs.

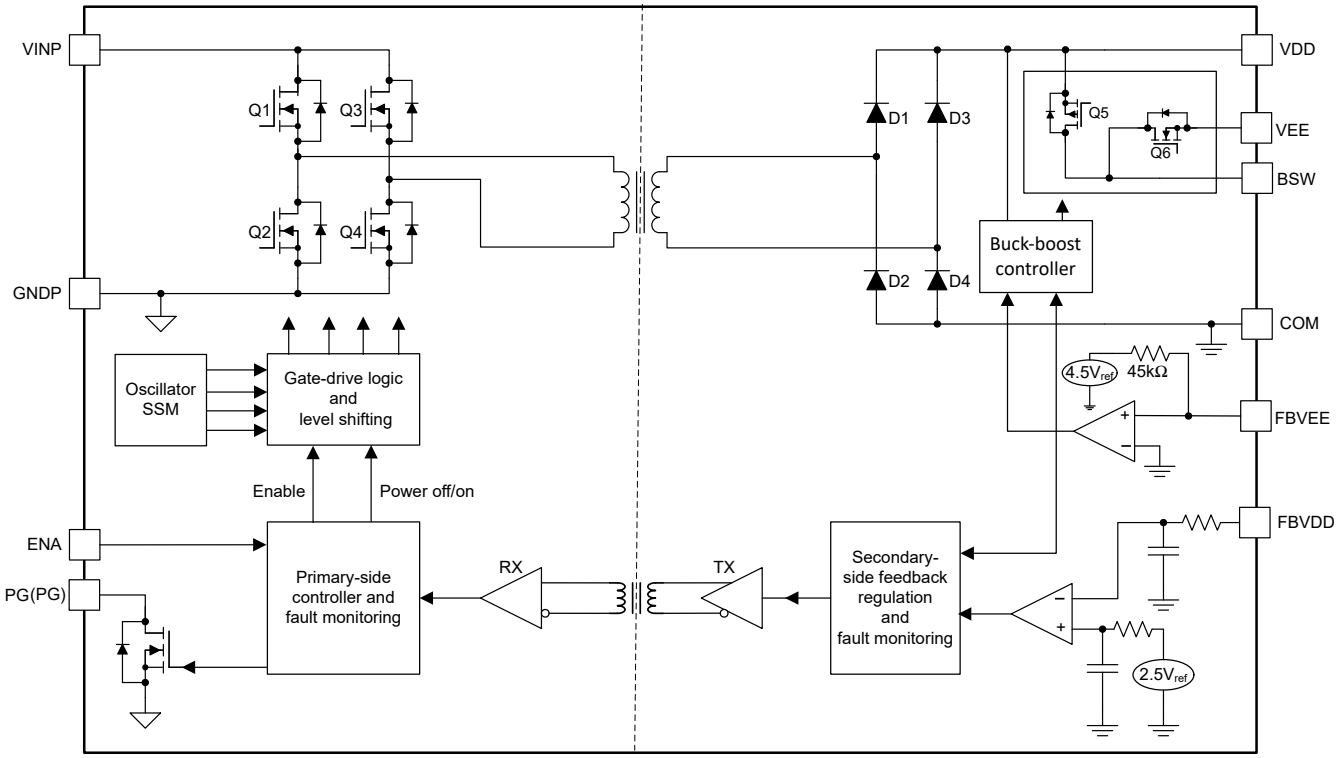
The UCC34141-Q1 has a Power-Good indicator with active polarity either High or Low based on the he part number as listed in Table 4-1. The output load must be kept low until start-up is complete and Power-Good pin becomes Active. For succesful soft-start, do not apply a heavy load to (VDD – COM) or (COM – VEE) outputs until the Power-Good pin has indicated Active status.

TI recommends to use the Power-Good status indicator as a trigger point to start the PWM signal into the gate driver. Power-Good output removes any ambiguity as to when the outputs are ready by providing a robust closed loop indication of when both (VDD –COM) and (COM – VEE) outputs have reached their regulation threshold within ±10%.

Do not allow the host to begin PWM to gate driver until Power-Good goes Active. This action typically occurs less than t_{SSTO} after V_{VIN} > V_{VIN_UVLOP} and ENA goes high. The Power-Good status output indicates the power is good after soft-start of (VDD – COM) and (COM – VEE) and are within ±10% of regulation.

If the host is not monitoring Power-Good, it is recommended that the host disables PWM to gate driver until 50 ms after V_{VIN} > V_{VIN_UVLOP} and ENA goes high in order to allow enough time for power to be good after soft-start of VDD and VEE.

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 Power Stage Operation

The UCC34141-Q1 module uses a soft-switching full-bridge converter on the primary-side and a passive full-bridge rectifier on the secondary-side. The small integrated transformer operates with a high switching frequency to reduce the size for integrating into the 16-pin SSOP package. The power stage switching frequency is within 16.5MHz to 27MHz. The power stage switching frequency is determined by input voltage with a feed-forward control as illustrated by the figure below. Adapative spread spectrum modulation, ASSM, is used to reduce emissions. ZVS operation is maintained to reduce switching power losses.

The UCC34141-Q1 module creates two regulated outputs. It can be configured as a single output converter, VDD to COM only, or a dual-output converter, VDD to COM and COM to VEE.

These two outputs are controlled independently through hysteretic control. Furthermore, the VDD to COM is the main output, and COM to VEE uses the main output as its input to create a second regulated output voltage.

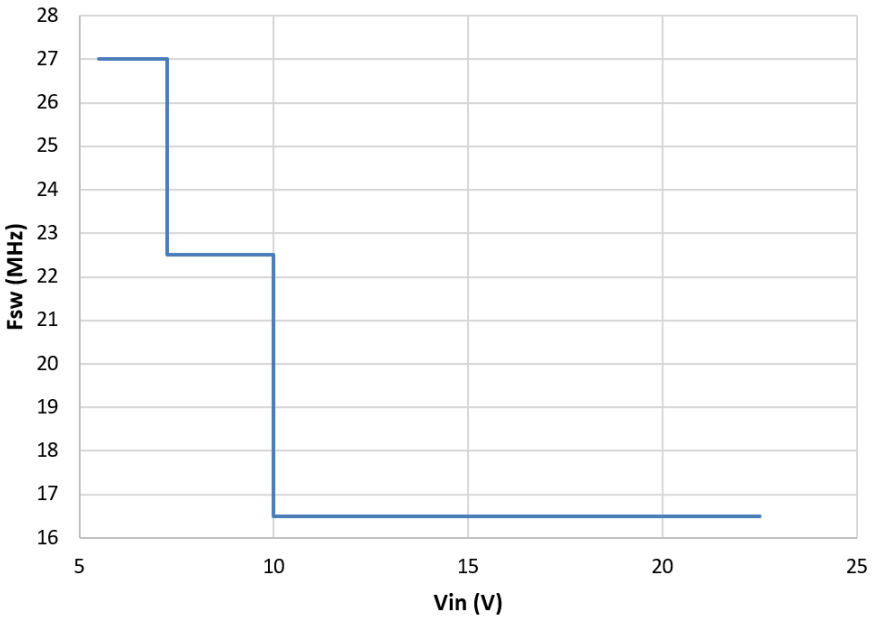

Figure 7-1. VDD-COM Switching Frequency with Respect to Input Voltage

7.3.1.1 VDD-COM Voltage Regulation

The VDD output is the main output of the module. The power stage operation is determined by the sensed VDD voltage on FBVDD pin using hysteresis control. The internal reference voltage V_{FBVDD_REF} = 2.5V. The VDD voltage is sensed through a voltage divider R_{FBVDD_TOP} and R_{FBVDD_BOT}. When FBVDD voltage stays below the turn-off threshold, the power stage operates in burst on state, delivers power to the secondary side and makes the VDD output voltage rise. After FBVDD reaches the turn-off threshold, the power stage turns off. VDD Output voltage drops because of the load current. After FBVDD voltage drops below the turn-on threshold, the power stage is turned on again. With the accurate voltage reference and hysteresis control, the VDD output voltage can be regulated with ≤1.5% accuracy.

To improve the noise immunity, a small capacitor C_{FBVDD} of 220pF should be added between FBVDD and COMA pins. In an environment with high EM noise, higher feedback decoupling capacitance C_{FBVDD}, and lower feedback resistance R_{FBVDD_TOP} and R_{FBVDD_BOT} values can be selected to further improve the noise immunity of the VDD feedback loop.

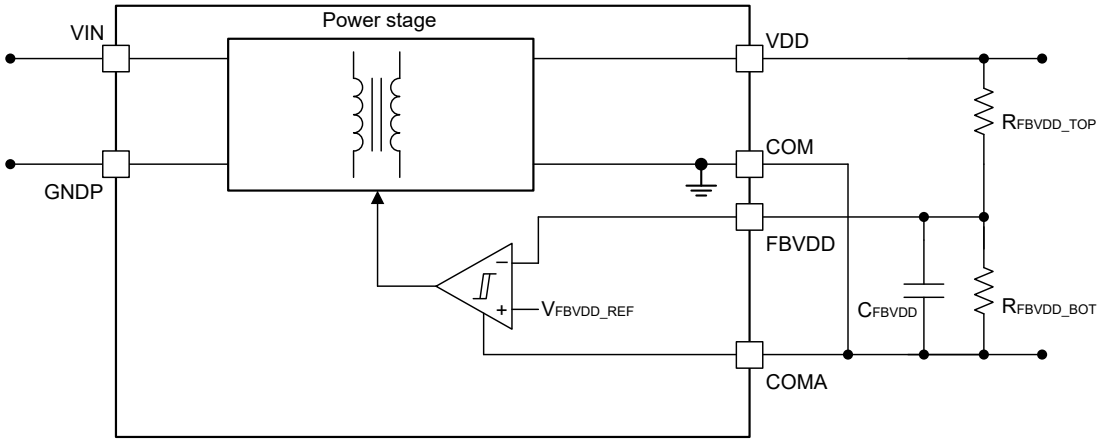

Figure 7-2. VDD-COM Voltage Regulation Functional Block Diagram

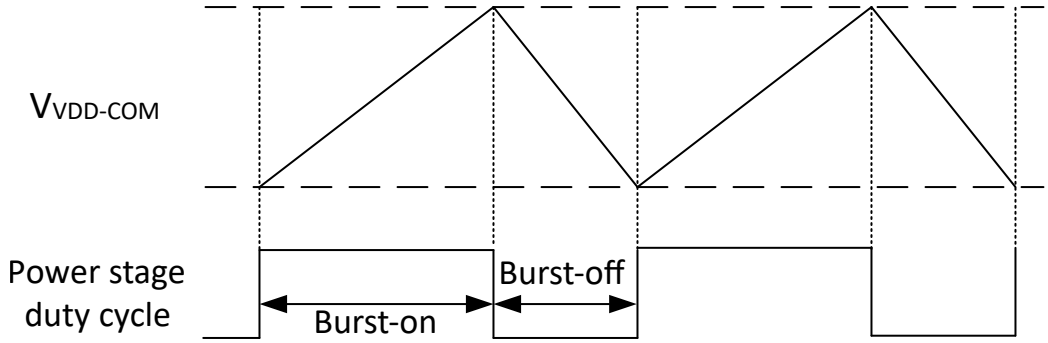

Figure 7-3. Concept of VDD-COM Regulation Scheme

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7.3.1.2 COM-VEE Voltage Regulation

An internal buck-boost converter generates the regulated negative VEE voltage. The buck-boost converter operation is determined by the sensed VEE voltage on FBVEE pin. With an internal 90k resistor and a 4.5V reference voltage, VEE voltage can be programed and regulated between -2V to -8V.

The buck-boost converter is controlled by an integrated hysteresis voltage feedback loop for COM-to-VEE voltage regulation and an integrated current control loop for cycle-to-cycle current limit. When FBVEE voltage stays below the turn-off threshold, the buck-boost converter operates with peak current mode control. The inductor current increases at the beginning of a switching cycle until it reaches the peak current limit, then returns to zero. In normal operation, the converter operates in boundary conduction mode, but can enter continuous conduction mode during start-up. As the peak current of the buck-boost is limited to less than I_{LIM}, the chosen inductor must have a saturation current above I_{LIM}. As shown in the Electrical Characteristics table, the peak current limit, I_{LIM}, is implemented with a feedforward control based on VDD voltage, so that the maximum inductor current will not exceed I_{LIM}, considering the overshoot due to the control loop delay at different VDD voltages. A higher VDD voltage leads to a bigger overshoot, and thus results in a lower I_{LIM} value for compensation. The recommended inductor selection is between 3.0µH and 10.0µH. The typical switching frequency is f_{SW_VEE} under the conditions listed in the Electrical Characteristics table.

After the FBVEE voltage reaches the turn-off threshold, the buck-boost converter turns off. After the FBVEE voltage drops below the turn-on threshold due to the load current, the buck-boost converter is turned on again. With the accurate voltage reference and hysteresis control, the VEE output voltage can be regulated with ≤5% accuracy.

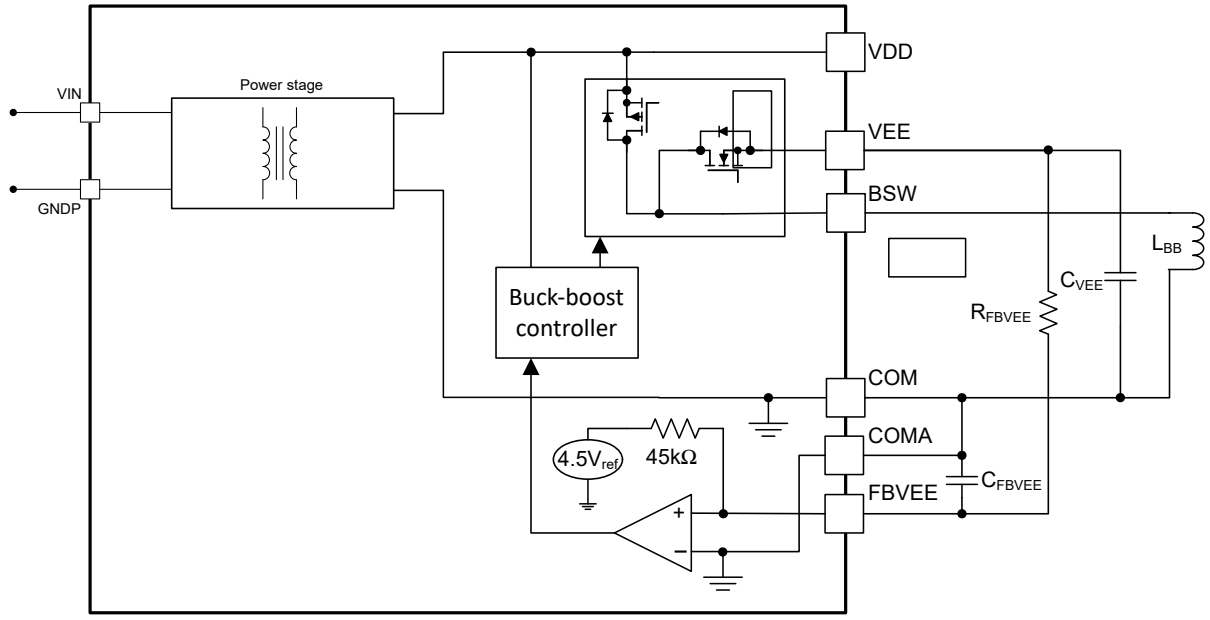

Figure 7-4. COM-VEE Voltage Regulation Functional Block Diagram

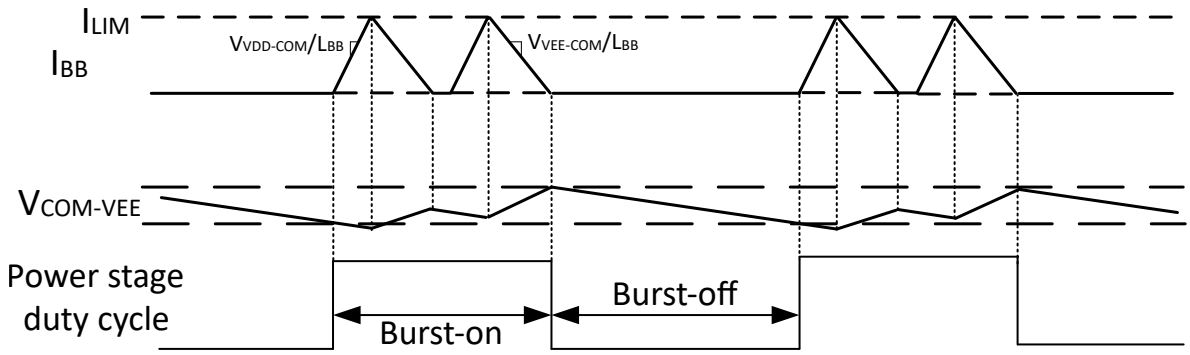

Figure 7-5. Concept of COM-VEE Regulation Scheme

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7.3.1.3 COM-VEE Output Capability

The maximum output current and output power capability of the VEE buck-boost converter at different VDD-COM and COM-VEE voltages are shown in Figure 7-6 and Figure 7-7. It can also be calculated in the Excel calculator tool, as another design supporting doucment besides this datasheet. The power module has two independent output power capablilities: one is of VDD-COM output as shown by the SOA curves in the Typical Characteristics section, and the other one is of COM-VEE output as shown in this section. Excessive output power requirement out of either of the two output power capablity can cause an output undervoltage protection and shutdown of the device.

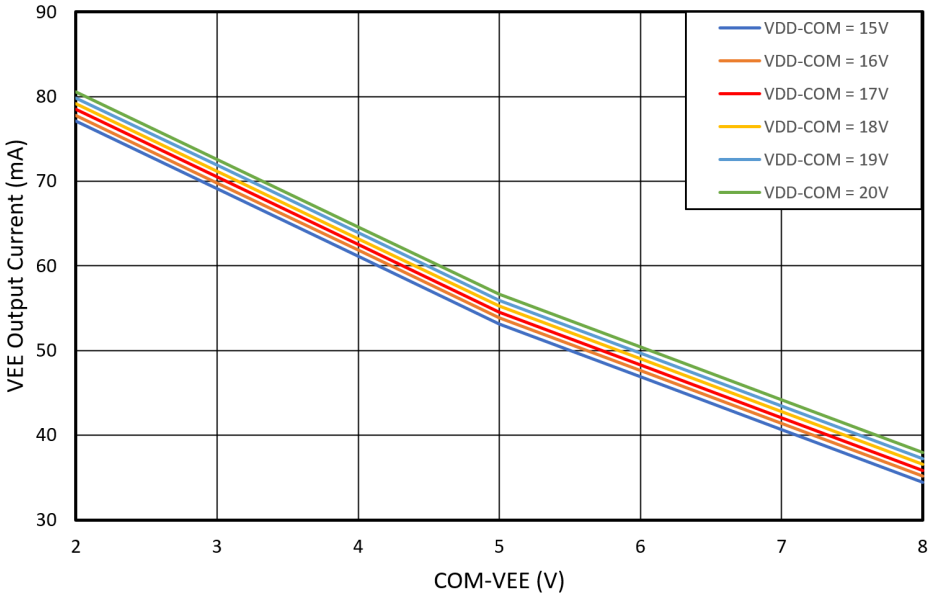

Figure 7-6. Output Current Capablity of VEE Buck-Boost Converter at Different VDD-COM and VEE-COM Voltages

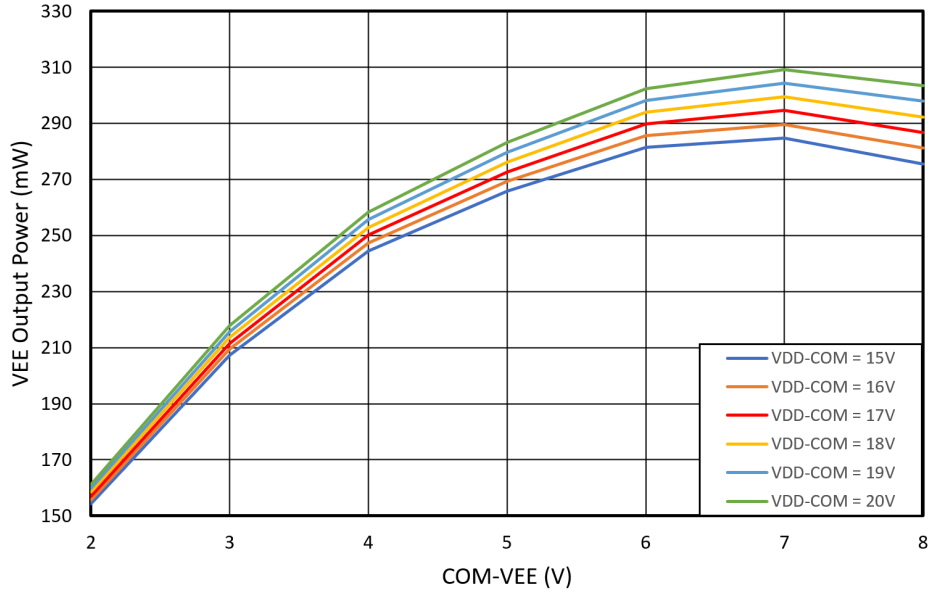

Figure 7-7. Output Power Capablity of VEE Buck-Boost Converter at Different VDD-COM and VEE-COM Voltages

7.3.2 Output Voltage Soft Start

UCC34141-Q1 has soft-start mechanism that ensures a smooth and fast soft-start operation with minimum input inrush current. The output voltage soft-start diagram is shown in the figure below. After input voltage is higher than the VIN_UVLO threshold, and the ENA signal is pulled high, the soft-start sequence starts with a primary duty cycle open loop control. The power stage operates with a fixed burst frequency with an incremental increasing duty cycle starting at 6.5%. The rate of change of the duty cycle is pre-programmed in the part to reduce the input inrush current while building the output voltage VDD. The primary side limits the maximum duty cycle to 62.5% during this phase till the secondary side VDD voltage passes VDD_UVLO before releasing this duty cycle limit. This limit will ensure minimum input current in case the device starts on a short circuit and the VDD is not building up. Once the VDD reaches the regulation range, the duty cycle is no longer determined from the primary side controller but instead VDD hysteretic control is active to tightly regulate the output voltage within the defined hysteresis band.

When VDD passes V_{VDD_UVLO}, a FBVEE status check will be performed, and then a single inductor current pulse is generated for BSW pin fault detection. When VDD reaches regulation, the VEE soft start occurs with low peak current. In this way, the charge current of isolated converter can dedicatedly supply VDD cap first before the VEE soft start. The soft start process of VEE voltage has two phases. In phase 1, limited VEE soft start peak current at the beginning reduces the power loss before the soft-start timeout expires, especially when VEE pin is shorted to COM. When $V_{COM\text{-}VEE}$ is higher than V_{VEE_SS} (0.5V Typ.), the VEE soft start enters phase 2, and the inductor peak current is increased to a higher value so that the startup time of charging VEE capacitor will show faster ramp rate.

For the Power-Good signal generation, when VDD voltage reaches regulation, two timers of t_{VEE_SSTO} and t_{PG_Delay} are started. If VEE does not pass VEE_UVP threshold within t_{VEE_SSTO} period, a fault will be triggered to shut down the part and flag a failed soft start. If no fault is detected up within t_{PG_Delay} period, Power-Good signal will change to active status to indicate a Power-Good state. If VDD voltage does not reach regulation within t_{SSTO} peroid, a fault will be triggered to shut down the part and flag a failed soft start.

To ensure VEE reaches VEE_UVP threshold within t_{VEE_SSTO} period, the sum of the COM-to-VEE output capacitance at gate driver side (C_{VEE_GD}) and at isolated-converter bias side (C_{VEE_BIAS}) should not exceed a maximum allowed value. The maximum allowed value at gate driver side (C_{VEE_GD}) is available in a calculation tool, as another design supporting document besides this datasheet. The equation to determine the maximum allowed capacitor value is shown as below, and is implemented in the calculation tool. In the equation, $I_{LOAD\_SS\_VEE}$ represents the quiescent current of output load during VEE soft start.

$$C_{VEE\_GD} \leq \frac{t_{VEE\_SSOT\_min}}{\frac{V_{VEE\_SS}}{I_{VEE\_Phase1} - I_{LOAD\_SS\_VEE}} + \frac{V_{VEE} - V_{VEE\_SS}}{I_{VEE\_Phase2} - I_{LOAD\_SS\_VEE}}} - C_{VEE\_BIAS} \quad (1)$$

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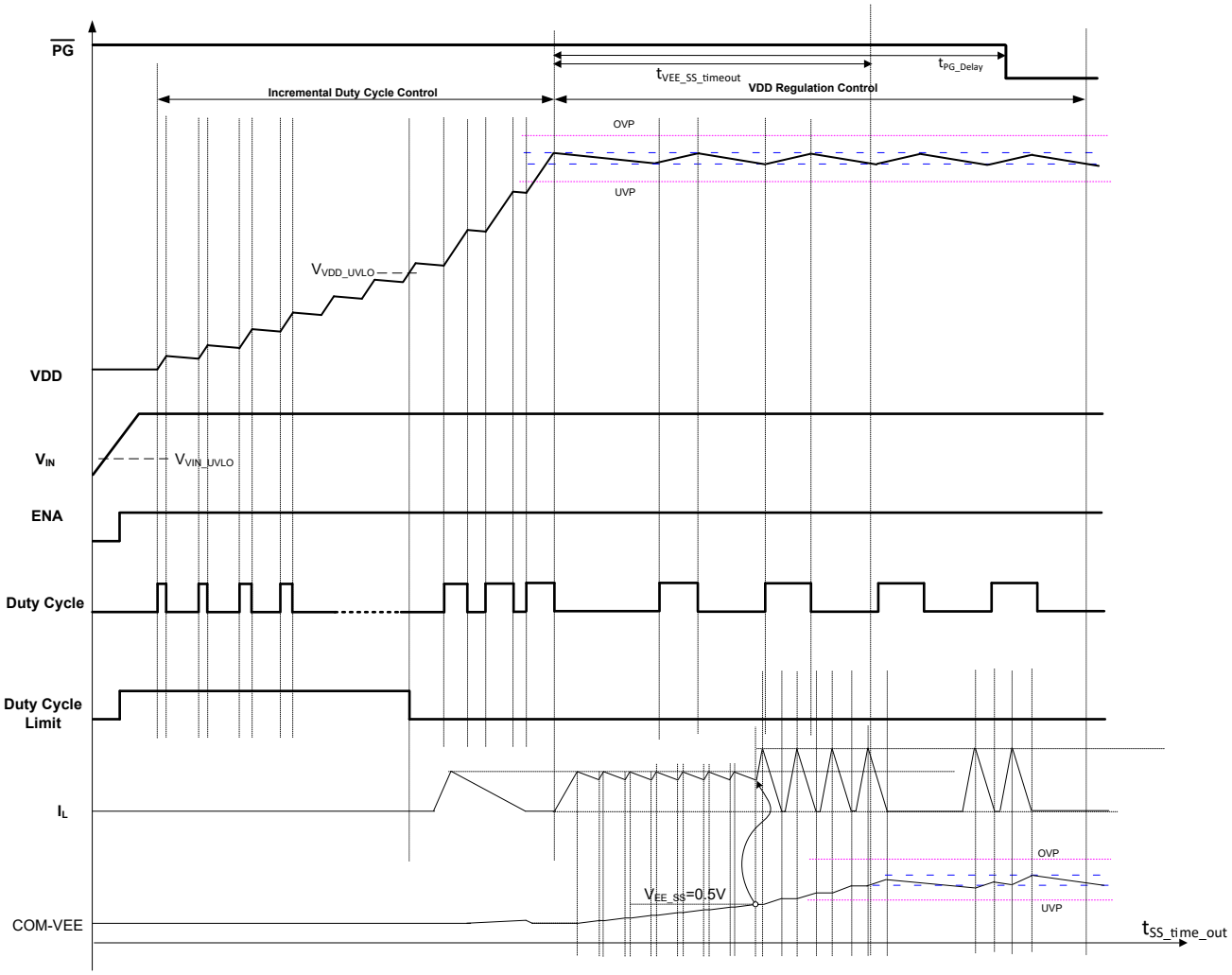

Figure 7-8. Output Voltage Soft-Start Diagram with Power-Good Active LOW

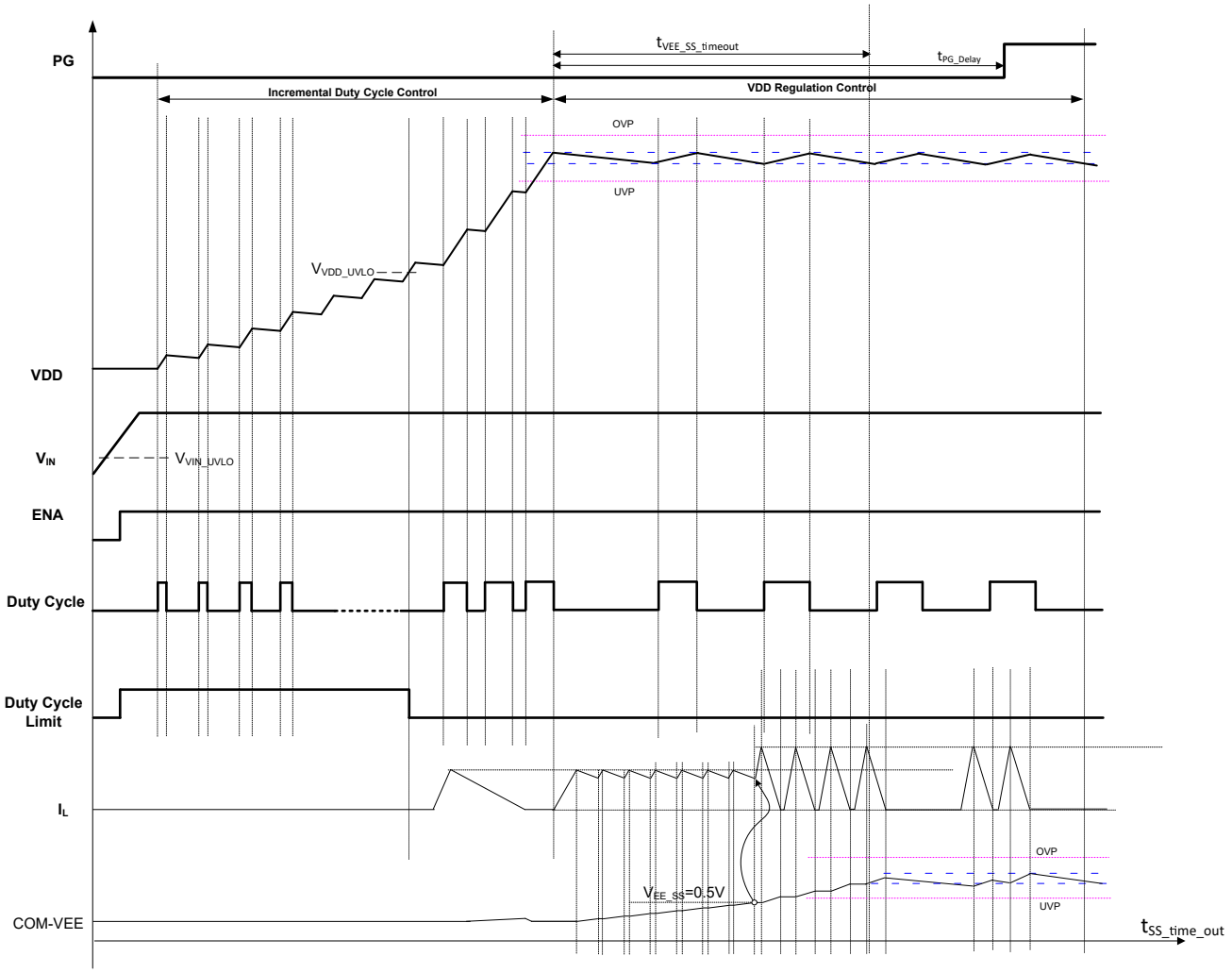

Figure 7-9. Output Voltage Soft-Start Diagram with Power-Good Active HIGH

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7.3.3 ENA and Power-Good

The ENA input pin and Power-Good output pin on the primary-side support both TTL and CMOS logic levels in 5V or 3.3V domain. The active-high enable input (ENA) pin is used to turn-on the isolated DC/DC converter. Either 3.3V or 5V logic rail can be used. The recommended maximum ENA-pin voltage is 5.5V. After ENA pin voltage rises above the enable threshold V_{ENA_R}, the power module starts switching, goes through the soft-start process and delivers power to the secondary side. After ENA pin voltage falls below the disable threshold V_{ENA_F}, UCC34141-Q1 is disabled, and the internal power stage stops switching.

For Latch-off devices, the ENA pin can also be used to reset the device after it enters the protection safe-state mode. After a detected fault, the protection logic will latch off and place the device into a safe state. To reset the part, the user is required to wait for $t_{EN\_LO\_DLY}$ after fault, then toggle the ENA-pin voltage below V_{ENA_F} for longer than $t_{EN\_LO\_RST}$, then toggle back up to 3.3V or 5V. The device will then exit the latch-off mode and a soft-start sequence will be reinitiated.

The ENA pin can also be used to implement a programmable input UVLO by using an external resistor divider between VIN and ENA pins. For the device and application with relatively low input UVLO and relatively high V_{IN}, when there is a slow V_{IN} ramp during start-up, the relatively low transformer turns-ratio will not be able to generate enough power to charge up the output capacitor and will thus fail the start-up. This issue can be solved by adding a resistor divider between VIN, ENA, and GNDP pins to program the ENA signal time and override the internal input UVLO. The V_{ENA_R} rising threshold is set at 1.5V and the V_{ENA_F} falling threshold is set at 1.35V. The programmable input UVLO feature can also be used to sequentially start-up multiple integrated DC/DC modules, by adding delay capacitors between ENA and GNDP pins to program the delay time between each power module. Specifically, the ENA1 signal can enable one module or one grouped modules, while the delayed ENA2 signal from ENA1 can sequentially enable another module or another grouped modules. For the appliation where ENA1 and ENA2 are too far away for the R_{ENA2} routing, the RC circuitry for ENA1 can be duplicated at the ENA pin of each module to enable sequential startup. If the sequential power up is not needed, multiple modules can share the same resistor divider to program input UVLO threshold. To facilitate the implementation, the recommended resistor and capacitor values are available in a calculation tool, as another design supporting document besides this datasheet.

If a single fault event on the resistor divider needs to be considered, e.g. the single bottom resistor is failed open, the risk of exceeding the 7V absolute maximum of ENA pin needs to be mitigated in application level. Two approaches can be applied: one option is adding an external Zener diode on ENA pin; another option is to split the bottom resistance into two resistor components.

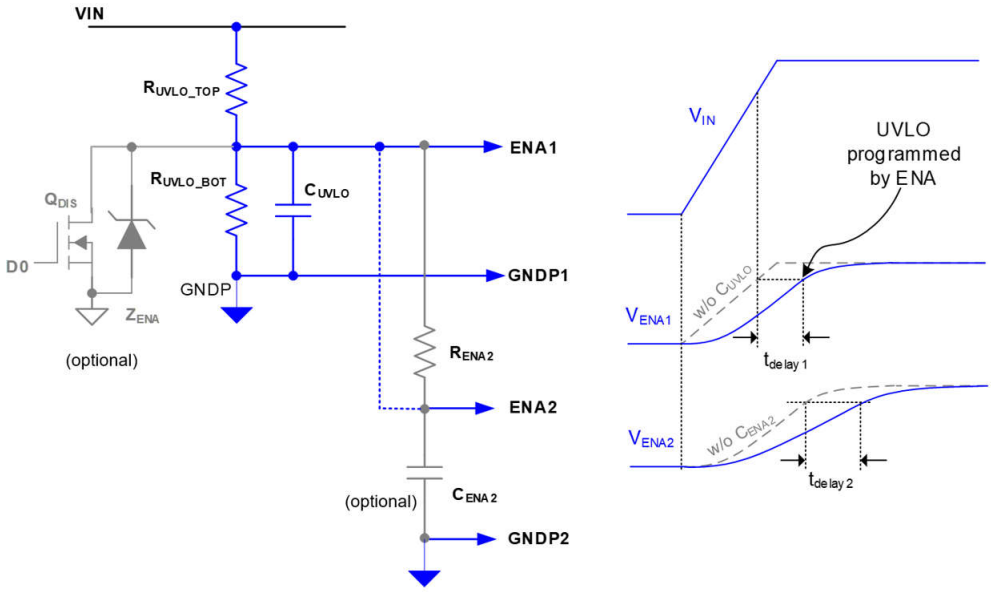

Figure 7-10. Input UVLO Programming Circuit and Operation Principle

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The Power-Good is an open-drain output which active state indicates when the module has no fault and the output voltages are within ±10% of the output voltage regulation setpoints. To account for the maximum current sinking capability of the internal pull-down MOSFET < 5mA, a pull-up resistor (> 1kΩ) from Power-Good pin to either a 5V or 3.3V logic rail is recommended. Higher resistance will reduce the quiescent current in normal logic state of Power-Good pin. It is essential to maintain the Power-Good pin voltage below 5.5V without exceeding its recommended operating voltage.

For Active-Low Power-Good polarity, there is a voltage drop in the $\overline{PG}$ signal during start up, due to the parasitic capacitance between the adjacent VIN pin and $\overline{PG}$ pin. This capacitive coupling generates a pulling currect into the $\overline{PG}$ pin and therefore leads to a volage drop across the pull-up resistor and thus a voltage drop on $\overline{PG}$ signal during start up. A 4.99kΩ pull-up resistor, and a 1µF decoupling capacitor connecting $\overline{PG}$ pin and ground are recommended to diminish the voltage drop during start up.

For Active-High Power-Good polarity, the PG will be grounded during the start up, so a small decoupling capacitor in the range of 0.1µF - 1µF with a 10kΩ pull-up resistor can be selected. The active-high setting allows an easy group fault reporting by direct connection of the PG pin signals from multiple DC/DC modules, becasue the combined PG signal will stay low when a power-bad condition in any one (or more) module(s) turns-on the pull-down FET; during power-good condition on the other hand, the combined PG signal will stay high becasue the pull-down FETs of all the DC/DC modules stay off

7.3.4 Protection Functions

UCC34141-Q1 is equipped with a full feature of protection functions, including input undervoltage lockout, overvoltage lockout, output undervoltage, overvoltage, and over-temperature. The input undervoltage and overvoltage lockout protections have an auto recovery response. All other protections have a fault response based on the part number as listed in Table 4-1. For the latch-off-response, protections are triggered, the converter enters a latch-off state, and stops switching. The latch is reset by either toggling the ENA pin Off then On, or by lowering the V_{VIN} voltage below the $V_{VIN\_UVLO\_F}$ threshold, and then above the $V_{VIN\_UVLO\_R}$ threshold. For auto-restart response, once the part shuts down, a $t_{RESTART}$ timer will start and then the part will attempt an auto-restart with a new soft-start sequence as shown in Figure 7-11. If the fault has been removed, the part will soft-start to regulation successfullly. If the fault condition remains, the part will shut down again and attempt another auto-restart. The device can continuously operate safely in hiccup mode as long as the fault occurs.

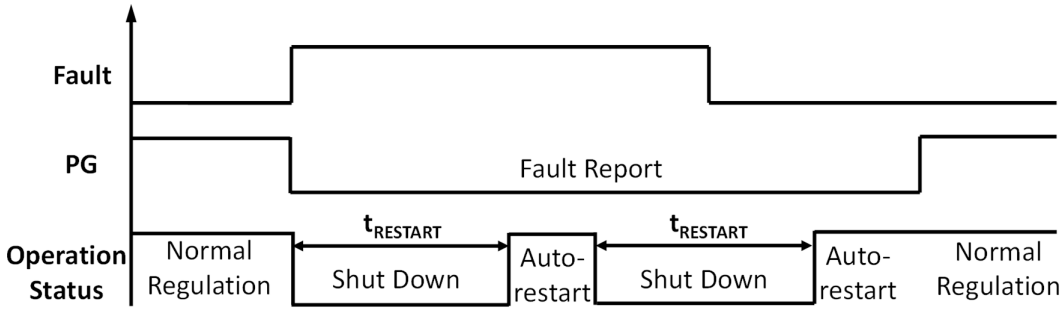

Figure 7-11. Auto-Restart Operation with PG Active High

7.3.4.1 Input Undervoltage Lockout

The UCC34141-Q1 enters input undervoltage lockout when V_{VIN} voltage becomes lower than the UVLO threshold $V_{VIN\_UVLO\_F}$. In UVLO mode, the converter stops switching. After VIN pin voltage falls lower than the $V_{VIN\_UVLO\_F}$, UCC34141-Q1 resets all the protections. And then, after the V_{VIN} voltage rises above the UVLO threshold $V_{VIN\_UVLO\_R}$, the converter is enabled. Depending on the ENA pin voltage, the converter can start switching, go through the soft-start process, or in the disable mode, waiting for ENA pin voltage becomes high.

7.3.4.2 Input Overvoltage Lockout

The input overvoltage lockout protection is used to protect the UCC34141-Q1 from overvoltage damage. The UCC34141-Q1 also has an auto-recovery response. When the V_{VIN} pin voltage becomes higher than the input

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overvoltage lockout threshold $V_{VIN\_OVLO\_R}$, switching stops and the converter stops sending energy to the secondary side. Once V_{VIN} pin voltage drops below the recovery threshold $V_{VIN\_OVLO\_F}$ following an overvoltage lockout, depending on the ENA pin voltage status, the converter can either resuming operation, go through the full soft-start process, or in the disabled mode, wait for ENA pin to go high.

The input overvoltage lockout does not reset other latch-off protections.

7.3.4.3 Output Undervoltage Protection

The output voltage under voltage protection is based on the FBVDD and FBVEE pin voltages. When the FBVDD pin voltage falls below the UVP threshold $V_{VDD\_UVP\_F}$, or the FBVEE pin voltage falls below the UVP threshold $V_{VEE\_UVP\_F}$, the undervoltage protection is activated. The UCC34141-Q1 stops switching, and the Power-Good pin change to non-active status.

During soft start, the output voltages rise from zero volts, thus, both FBVDD and FBVEE pin voltages are below the UVP thresholds. The UVP is disabled during the soft start. If the pin voltage cannot reach the UVP recovery thresholds ($V_{VDD\_UVP\_R}$, $V_{VEE\_UVP\_R}$) after the soft start completes, undervoltage protection is activated, the UCC34141-Q1 stops switching, and the Power-Good pin change to non-active status.

7.3.4.4 Output Overvoltage Protection

The UCC34141-Q1 senses the output voltage through FBVDD and FBVEE pins to control the output voltage. To prevent the output voltage from getting too high, damaging the load or UCC34141-Q1 device, the UCC34141-Q1 is equipped with the output overvoltage protection. There are two levels of overvoltage protection based on the feedback pin voltage, and the output voltage.

During the normal operation, because of load transient, the output voltages can exceed the regulation level. Based on the pin voltages on FBVDD and FBVEE, after the voltage exceeds the threshold, $V_{VDD\_OVP\_R}$, or $V_{VEE\_OVP\_R}$, the converter stops switching immediately.

In rare cases, the voltage divider can malfunction resulting in the wrong output voltage information. In turn, the control loop will regulate the output voltages at a wrong voltage level. For instances like this, the UCC34141-Q1 is also equipped with a fail-safe overvoltage protection. After the VDD-COM or COM-VEE voltage exceeds the overvoltage protection threshold $V_{VDD\_OVLOS\_R}$ or $V_{VEE\_OVLOS\_R}$, the converter shuts down immediately. This fail-safe protection level is meant to protect UCC34141-Q1 rather than the load. The design must specify the voltage feedback divider normal operation at all conditions.

7.3.4.5 Over-Temperature Protection

UCC34141-Q1 integrates the primary-side, secondary-side power stages, as well as the isolation transformer. The power loss caused by the power conversion causes the module temperature higher than the ambient temperature. For the safe operation of the power module, the UCC34141-Q1 is equipped with over-temperature protection. Both the primary-side power stage, and the secondary-side power stage temperatures are sensed and compared with the over-temperature protection threshold. If the primary-side power stage temperature becomes higher than $T_{SHUT\_P\_R}$, or the secondary-side power stage temperature becomes higher than $T_{SHUT\_S\_R}$, the module enters over-temperature protection mode. The module stops switching and the Power-Good pin change to non-active status.

7.3.4.6 BSW Pin Faults Protection

UCC34141-Q1 has protection mechanism against BSW Pin faults during the soft-start period for the COM-VEE buck-boost converter.

In the case of BSW pin-open, when VDD voltage passes $V_{VDD\_UVLOS\_R}$ threshold, the part detects the first inductor current pulse width, which is the current ramp-up period until it hits the peak current limit. If the first inductor current pulse width is higher than the normal pulse width using largest inductance (>2.9µs), the BSW fault protection will be triggered to disable the buck-boost switching. Then, the device will stop switching after VDD soft start completion.

In the case of BSW pin-short to COM or VEE pin, the part detects the inductor current at the end of leading-edge-blank period. If the current is higher than the inductor peak current limit during soft-start, the BSW fault

protection will be triggered to disable the buck-boost switching. Then the device will stop switching after VDD soft start completion.

7.4 Device Functional Modes

Depending on the input and output conditions, ENA pin voltage, as well as the device temperature, the UCC34141-Q1 operates in one of the below operation modes.

1. Disable mode. In this mode, the module is off, waiting for ENA pin to go high to begin operation.
2. Soft-start mode. In this mode, the module starts to deliver power to the secondary side. The primary-side operation duty cycle is raised gradually to reduce the stress to the module.
3. Normal operation mode. In this mode, the module operates normally, delivering power to the secondary side.
4. Protection mode, auto-recovery. In this mode the module is off due to the input UVLO or OVLO protection. After the input voltage fault is cleared, depending on the ENA pin voltage condition, it either becomes disabled mode if the ENA pin voltage is low, or it goes through soft-start mode to the normal operation mode.
5. Protection mode, latched-off. In this mode the part is off due to other protections. The module remains off even the fault causing the protection is cleared. Recycling V_{VIN} operation must ensure the input voltage goes below the analog UVLO falling threshold ($V_{VIN\_UVLO\_F}$) first to reset the latch-off state, or the ENA pin is toggled Low (OFF) then High (ON).
6. Protection mode, auto-restart after defined duration $t_{RESTART}$. In this mode, the part shuts down due to other protections.Once the part shuts down, a $t_{RESTART}$ timer will start and then the part will attempt an auto-restart with a new soft-start sequence. If the fault has been removed, the part will soft-start to regulation successfullly. If the fault condition remains, the part will shut down again and attempt another auto-restart. The device can continuously operate safely in hiccup mode as long as the fault occurs.

Table 7-1 lists the supply functional modes for this device. The ENA pin has an internal weak pull-down resistance to ground, but TI does not recommend leaving this pin open.

Table 7-1. Device Functional Modes

INPUT			OUTPUTS			OPERATION MODE
V_{VIN}	ENA	FAULT	$V_{(VDD-COM)}$ Isolated Output1	$V_{(COM-VEE)}$ Isolated Output2	Power-Good(1) (2) Open Drain	
$V_{VIN} < V_{VIN\_UVLO\_R}$	X	X	OFF	OFF	Non-Active Status	Protection mode, auto-recovery
$V_{VIN\_UVLO\_R} < V_{VIN} < V_{VIN\_OVLO\_R}$	LOW	X	OFF	OFF	Non-Active Status	Disable mode
$V_{VIN\_UVLO\_R} < V_{VIN} < V_{VIN\_OVLO\_R}$	HIGH	NO FAULT	Regulating at Setpoint	Regulating at Setpoint	Active Status	Normal operation
$V_{VIN\_UVLO\_R} < V_{VIN} < V_{VIN\_OVLO\_R}$	HIGH	YES FAULT	OFF	OFF	Non-Active Status	Protection mode, latched-off or auto-restart after $t_{RESTART}$
$V_{VIN} > V_{VIN\_OVLO\_R}$	X	X	OFF	OFF	Non-Active Status	Protection mode, auto-recovery

(1) For Power-Good active HIGH devices listed in Table 4-1: Active status PG = HIGH , Non-Active status PG = LOW .
(2) For Power-Good active LOW devices listed in Table 4-1: Active status $\overline{PG}$ = LOW , Non-Active status $\overline{PG}$ = HIGH.

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8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The UCC34141-Q1 is suitable for applications that have limited board space and desire more integration. This device is also suitable for very high voltage applications, where power transformers meeting the required isolation specifications are bulky and expensive.

8.2 Typical Application

The following figures show the typical application schematics for the UCC34141-Q1 device configurations supplying an isolated load.

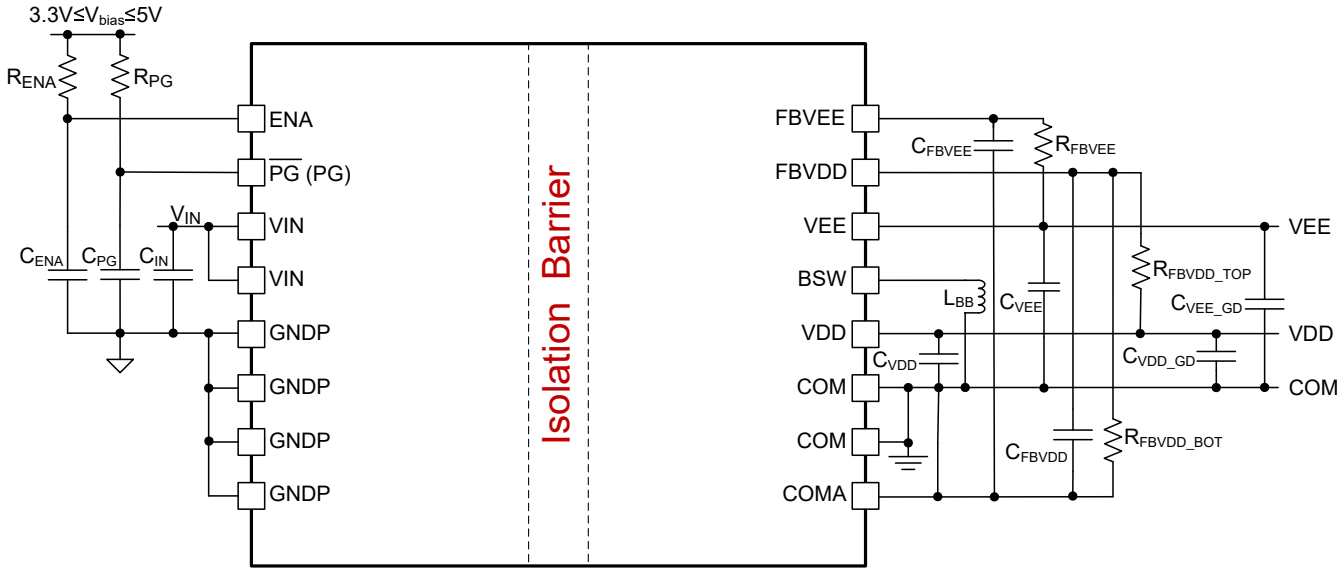

Figure 8-1. Dual Adjustable Output Configuration

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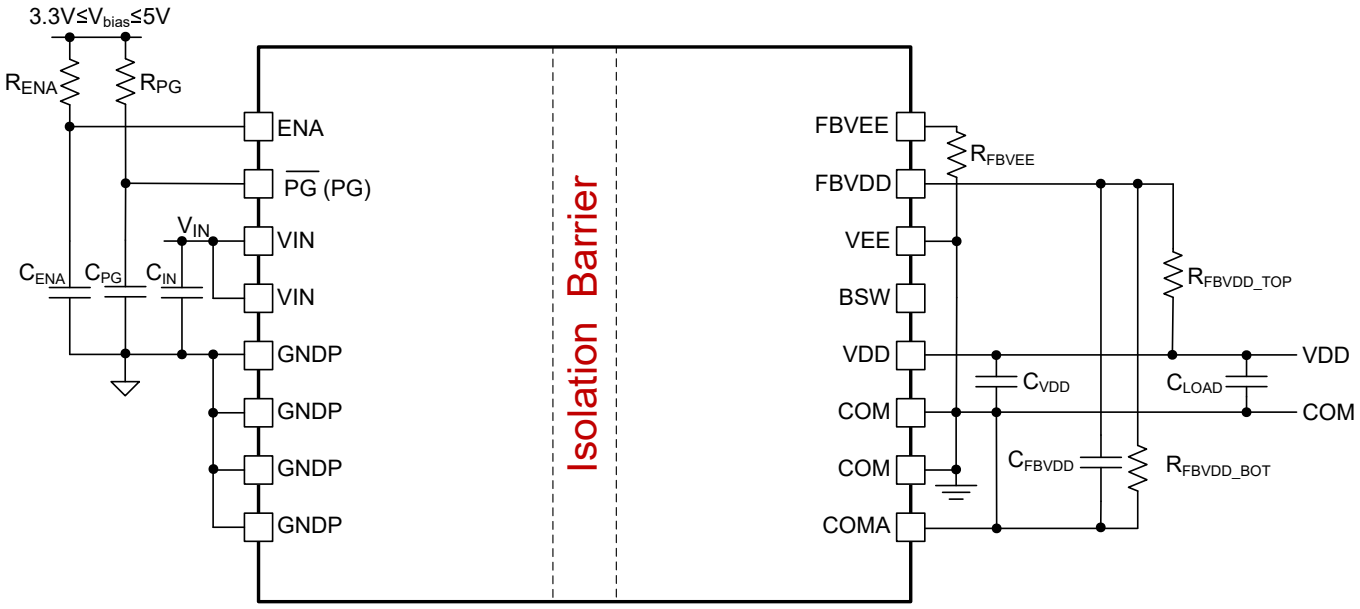

Figure 8-2. Single Adjustable Output Configuration

8.2.1 Design Requirements

Designing with the UCC34141-Q1 is simple. First, choose single output or dual output. Determine the voltage for each output and then set the regulation through feedback resistors. The gate charge of the power device determines the amount of output decoupling capacitance needed at the gate driver input.

For dual adjustable output configuration an internal inverting buck-boost converter generates a regulated negative rail for the turn-off supply (VEE). The buck-boost converter is controlled by a peak current mode, hysteretic controller. In normal operation, the converter remains in discontinuous-conduction mode, but can enter continuous-conduction mode during start-up. The converter is controlled internally and requires only a single surface-mount inductor (L_{BB}) and output bypass capacitor (C_{VDD}). Typically, the converter is designed to use a 3.3µH inductor and a 2.2µF output capacitor.

A summary table for the recommended values of BOM components is available in a calculation tool, as another design supporting document besides this datasheet.

8.2.2 Detailed Design Procedure

Place ceramic decoupling capacitors as close as possible to the device pins. For the input supply, place the capacitors between pin 4 (VIN) and pin 5 (GNDP). For the isolated output supply, (VDD – COM), place the C_{VDD} capacitor between pin 12 (VDD) and pin 11 (COM). For the negative votage supply, (COM – VEE), place the C_{VEE} capacitor between pin 14 (VEE) and pin 11 (COM). These locations are of particular importance to all the decoupling capacitors because the capacitors supply the transient current associated with the fast switching waveforms of the power drive circuits. Ensure the capacitor dielectric material is compatible with the target application temperature.

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8.2.2.1 VDD-COM Voltage Regulation

The UCC34141-Q1 creates an isolated output VDD-COM as its main output. The power stage operation is determined by sensing the VDD voltage on FBVDD pin using hysteresis control. The internal reference voltage V_{FBVDD_REF} = 2.5V. To determine the values for R_{FBVDD_TOP} with a chosen R_{FBVDD_BOT}, please use the equation

$$R_{FBVDD\_TOP} = \frac{V_{VDD}{}^{*}R_{FBVDD\_BOT}}{2.5V} - R_{FBVDD\_BOT} \quad (2)$$

As an example, to set a VDD value of 20V, a 10kΩ resistor can be chosen as R_{FBVDD_BOT}, and the R_{FBVDD_TOP} can be calculated as

$$R_{FBVDD\_TOP} = \frac{20V{}^{*}10k\Omega}{2.5V} - 10k\Omega = 70k\Omega \quad (3)$$

To improve the noise immunity, a small capacitor C_{FBVDD} of 220pF should be added between FBVDD and COMA pins.

8.2.2.2 COM-VEE Voltage Regulation and Single Output Configuration

UCC34141-Q1 can be configured either as a dual output or a single output converter, using the VEE feedback resistor R_{FBVEE}. The table below summarizes the programmable range with different R_{FBVEE} value. The VDD single output mode can be programmed by a R_{FBVEE} value between 150kΩ and 300kΩ. We recommend a 180kΩ SMD resistor with ≤±5% tolerance. A R_{FBVEE} lower than 150kΩ could trigger VDD & VEE dual output mode, and a R_{FBVEE} higher than 300kΩ could trigger FBVEE pin-open fault. The typical application schematic of single output configuration is shown in Figure 8-2

Table 8-1. R_{FBVEE} Programming

R_{FBVEE}	0 - 3kΩ	20kΩ - 80kΩ	150kΩ - 300kΩ	>500kΩ
Operation Mode	Trigger FBVEE pin-short fault SMD resistor with ±5% tolerance is enough	VEE in regulation, VDD & VEE dual output Recommend a SMD resistor with ≤ ±1% tolerance for best regulation accuracy.	VDD single output Recommend a 180kΩ SMD resistor with ≤±5% tolerance.	Trigger FBVEE pin-open fault

An internal buck-boost converter generates the regulated negative VEE voltage. The buck-boost converter operation is determined by sensing the VEE voltage on FBVEE pin. With an internal 45k resistor and a 4.5V reference voltage, VEE voltage can be programed and regulated between -2V to -8V. The transfer function between COM-VEE and R_{FBVEE} in dual output mode is

$$R_{FBVEE} = \frac{-V_{VEE}{}^{*}45k\Omega}{4.5V} \quad (4)$$

An example equation to set a VEE regulation value at -5V

$$R_{FBVEE} = \frac{-(-5V){}^{*}45k\Omega}{4.5V} = 50k\Omega \quad (5)$$

8.3 System Examples

The UCC34141-Q1 module is designed to allow a microcontroller host to enable it with the ENA pin for proper system sequencing. The Power-Good output also allows the host to monitor the status of the module. The Power-Good pin goes to its active status when there are no faults. The output voltage is meant to power a gate driver for either IGBT or SiC FET power device. The microcontroller can start sending PWM control to the gate driver after the Power-Good pin goes to its active status to ensure proper sequencing. The system diagrams for the dual-output configuration and single-output configuration are shown below.

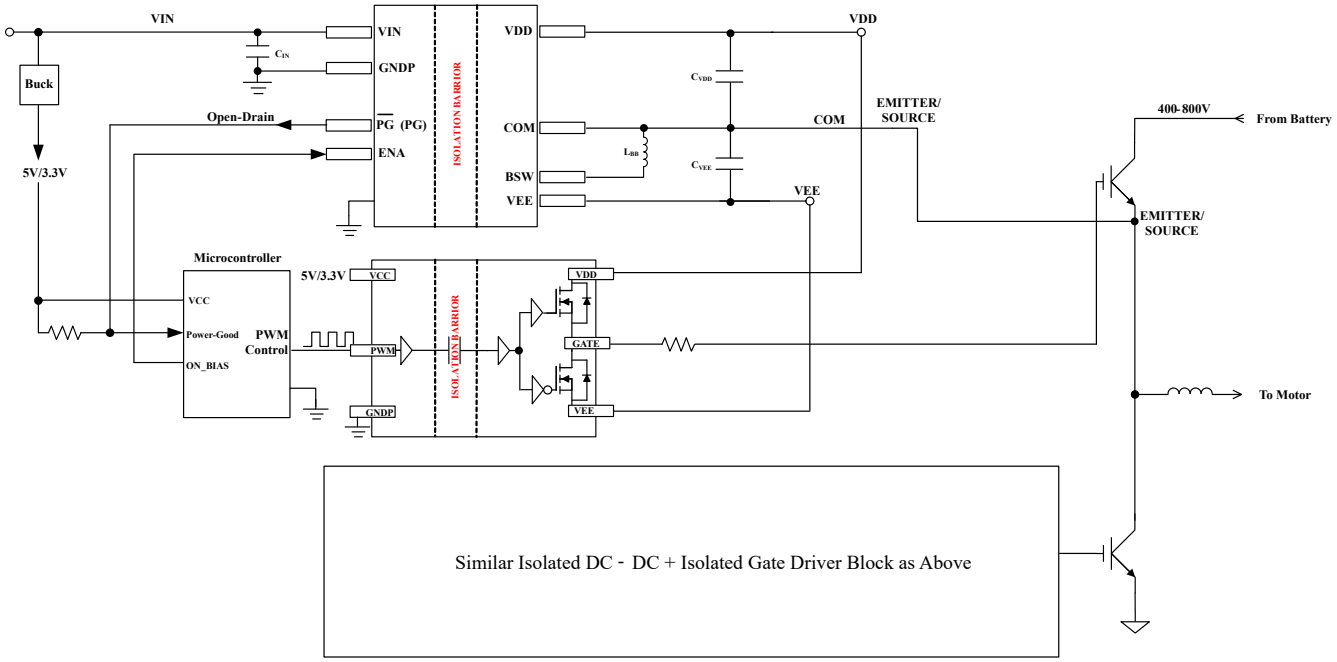

Figure 8-3. Dual Output System Configuration

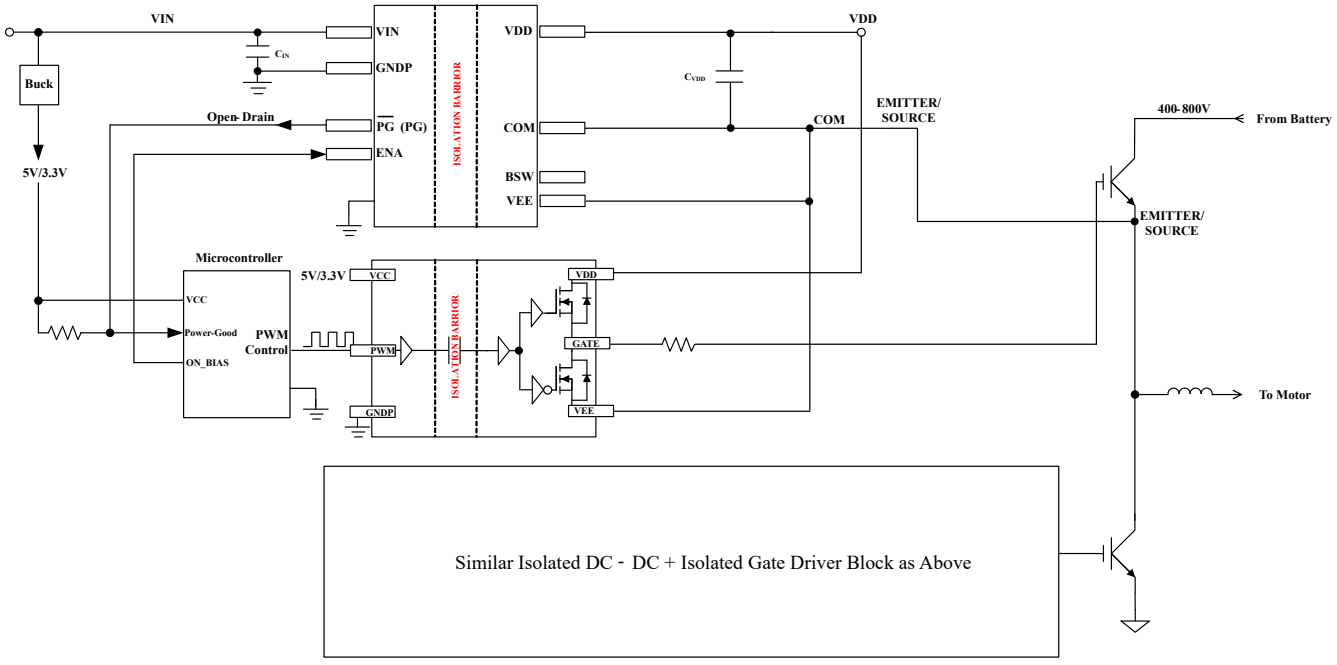

Figure 8-4. Single Output System Configuration

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8.4 Power Supply Recommendations

The recommended input supply voltage (V_{VIN}) for UCC34141-Q1 is between 5.5V and 20V. To help ensure reliable operation, adequate decoupling capacitors must be located as close to supply pins as possible. Local bypass capacitors must be placed between the VIN and GNDP pins at the input; between VDD and COM, and between COM and VEE at the output. TI recommends low ESR, ceramic surface mount capacitors to provide the recommended capacitance for high frequency decoupling. The input supply must have an appropriate current rating to support output load required by the end application.

8.5 Layout

8.5.1 Layout Guidelines

The UCC34141-Q1 integrated isolated power solution simplifies system design and reduces board area usage. Follow these guidelines for proper PCB layout to achieve optimum performance. A minimum of 4-layer PCB layer stack using 2-ounce copper on external layers is recommended to accomplish a good thermal PCB design. It is not recommended to route signal tracks or place components directly beneath the UCC34141-Q1.

1. Input capacitors between VIN pin and GNDP pin:
   a. Place the 0.1µF high frequency bypass capacitor (C3) as close as possible to pins 3, 4 (VIN) and pins 5–8 (GNDP) and on the same side of the PCB as the IC. 0402 ceramic SMD or smaller is a desired size for optimal placement. The self-resonant frequency in a range between 10MHz to 30MHz is most ideal to offer low impedance decoupling for the switching frequency noise of the internal isolated convertor. Do not place any vias between the bypass capacitor and the IC pins so as to force the high frequency current through the capacitor.
   b. Place the bulk VIN capacitor(s) (C2) as close as possible and parallel to the 0.1µF high frequency bypass capacitor (C3) and on the same side of the PCB as the IC as shown in Figure 8-5.
2. Power good pin decoupling capacitor: The decoupling capacitor should be placed close to pin 2 (power good pin) and on the same side of the PCB as the UCC34141-Q1. Refer to C13 placement shown in Figure 8-5.
3. Output capacitors between VDD pin and COM pin:
   a. Place the 0.1µF high frequency bypass capacitor (C5) as close as possible to pin 12 (VDD) and pins 10, 11 (COM) and on the same side of the PCB as the IC. 0402 ceramic SMD or smaller is a desired size for optimal placement. The self-resonant frequency in a range between 10MHz to 30MHz is most ideal to offer low impedance decoupling for the switching frequency noise of the internal isolated convertor. Do not place any vias between the bypass capacitor and the IC pins so as to force the high frequency current through the capacitor.
   b. Place the bulk VDD-COM capacitor (C8) as close as possible and parallel to the 0.1µF high frequency bypass capacitor (C5) and on the same side of the PCB as the IC as shown in Figure 8-5.
4. Output capacitors between VEE pin and COM pin:
   a. Place the 2.2µF high frequency bypass capacitor (C9) as close as possible to VEE and COM pins. The self-resonant frequency in 3MHz to 4MHz is most ideal to offer low impedance decoupling for the switching frequency noise of the buck-boost converter with the 3.3uH inductor (L1) selection. It is possible to put the capacitor on the different side of PCB and use vias to connect, in order to reduce the switching loop between the capacitor and the internal low-side MOSFET of the VEE buck-boost converter. In addition, putting the capacitor on different side will also simplify the decoupling capacitor placement of VDD pin and COM pin. An example of bottom side PCB placement of C9 and L1 is shown in Figure 8-9.
5. Feedback:
   a. COMA should be isolated through all PCB layers, from the COM plane. Use one via to make a direct connection to the low-side resistor and filter capacitor from FBVDD pin, same as the low-side filter capacitor from FBVEE pin.
   b. Place the RFBVDD feedback resistors (R6 and R7) and the decoupling ceramic capacitor (C6) close to the IC.
   c. The top-side feedback resistor should be placed next to the low-side resistor with a short, direct connection between both resistors and single connection to FBVDD pin. The top connection to sense the

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regulated rail (VDD-COM) should be routed and connected at the VDD bias capacitor remote location near the gate driver pins for best accuracy and best transient response.

d. The VEE feedback resistor (R5) should be placed with the decoupling ceramic capacitor (C4) next to FBVEE (pin 15); while the connection to sense the regulated rail (COM-VEE) should be routed and connected at the COM bias capacitor remote location near the gate driver pins for best accuracy and best transient response.
e. When using the dual output mode, the buck-boost inductor (L1) and a 2.2uF decoupling ceramic capacitor (C9) must be populated. They can be place on the opposite side of the IC or on the same layer as IC.
f. A layout example is shown in Figure 8-6, where L2 (yellow) is routed on layer 2 and L3 (green) is routed on layer 3.

6. Thermal vias: The UCC34141-Q1 internal transformer makes a direct connection to the lead frame. It is therefore critical to provide adequate space and proper heatsinking designed into the PCB as outlined in the steps below.
   a. TI recommends to connect the VIN, GNDP, VDD, and COM pins to internal ground or power planes through multiple vias. Alternatively, make the polygons connected to these pins as wide as possible.
   b. Use multiple thermal vias connecting PCB top side GNDP copper to bottom side GNDP copper. If possible, it is recommended to use 2-ounce copper on external top and bottom PCB layers.
   c. Use multiple thermal vias connecting PCB top side VEE copper to bottom side VEE copper. If possible, it is recommended to use 2-ounce copper on external top and bottom PCB layers.
   d. Thermal vias connecting top and bottom copper can also connect to internal copper layers for further improved heat extraction.
   e. Thermal vias should be similar to pattern shown below but apply as many as the copper area will allow. TI recommends to use thermal via with 30mil diameter, 12mil hole size.
   f. A layout example is shown in Figure 8-7. For cases where less copper area is available, use as many thermal vias as the design permits, placed close to pins 5-8 (primary) and 9-11 (secondary).
7. Creepage clearance: To maintain the full creepage, clearance and voltage isolation ratings specified in the data sheet, avoid routing signal traces or placing components directly under the UCC34141-Q1. Maintain the clearance width highlighted in red, throughout the entire defined isolation barrier. Keep-out clearance for basic isolation can be 50% less than the reinforced isolation requirement (8.2mm). Using 8.2mm provides additional margin. A layout example is shown in Figure 8-8.
8. Gate driver output capacitors: C_{VDD_GD} (C11 and C12) and C_{VEE_GD} (C10) are reference designators referred to in the UCC34141-Q1 Excel Calculator Tool. C11 and C12 are the capacitors between VDD-COM and C10 is the capacitor between COM-VEE. C10-12 are capacitors required by the gate driver IC.
   a. C_{VDD_GD} and C_{VEE_GD} should be placed next to the gate driver IC for best decoupling and gate driver switching performance.
   b. For optimal voltage regulation, the feedback trace from VEE (FBVEE) and VDD (FBVDD) should be as direct as possible so that the voltage feedback is being sensed directly at the VDD and VEE capacitors near the gate driver IC.

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8.5.2 Layout Example

The PCB layout example, highlighted in the following figures, is based on the schematic shown in Figure 8-1.

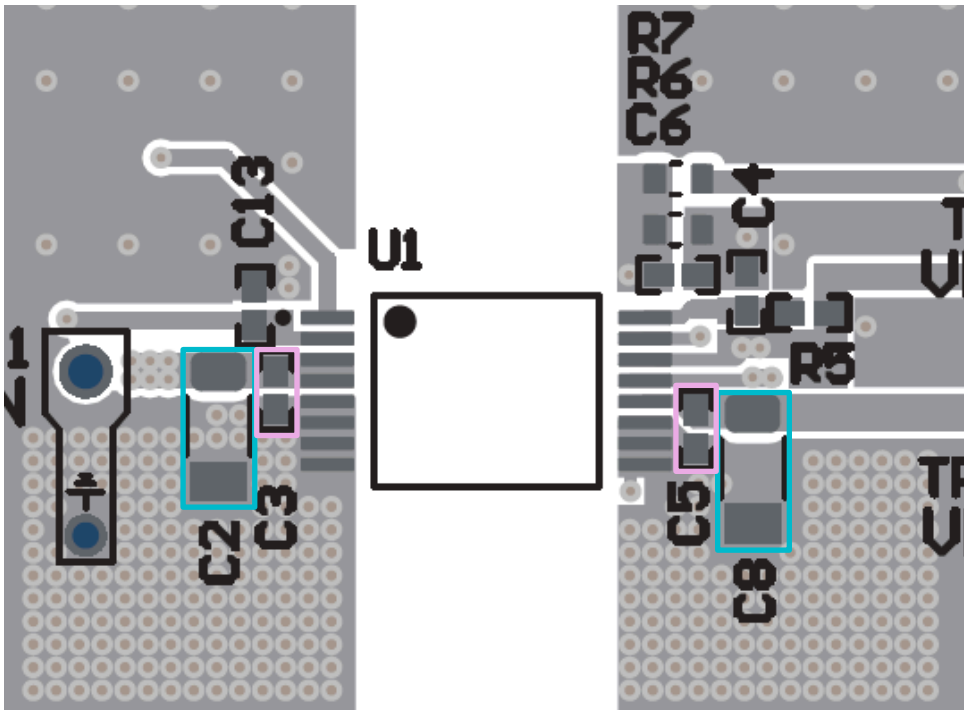

Figure 8-5. VIN (C2, C3) and VDD (C5, C8) Capacitors

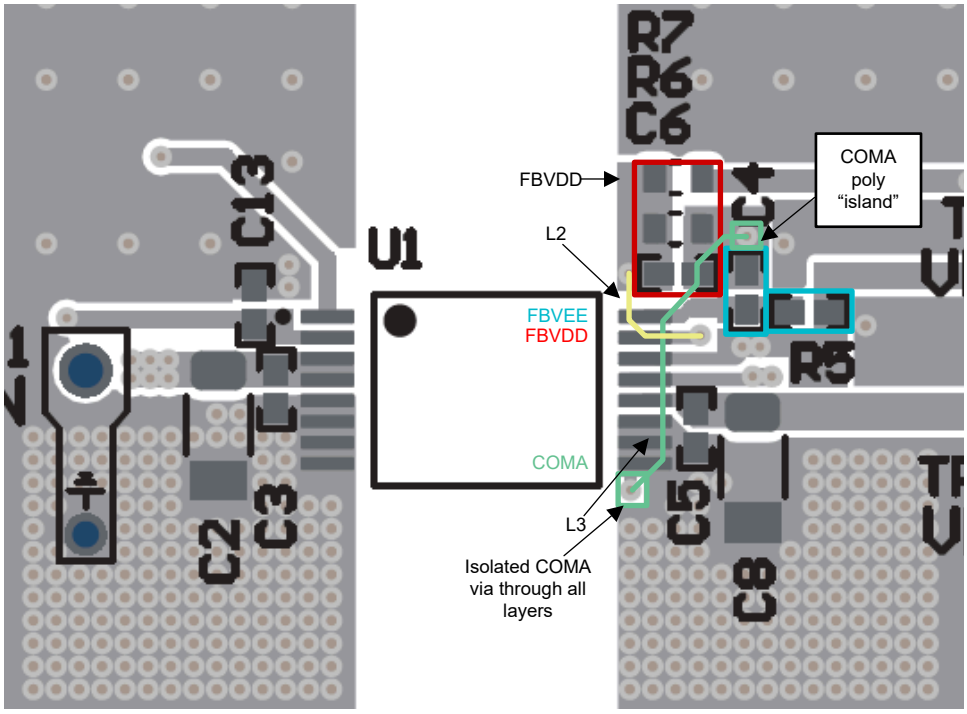

Figure 8-6. FBVDD (R6-7, C6), FBVEE (R5, C4), COMA Routing

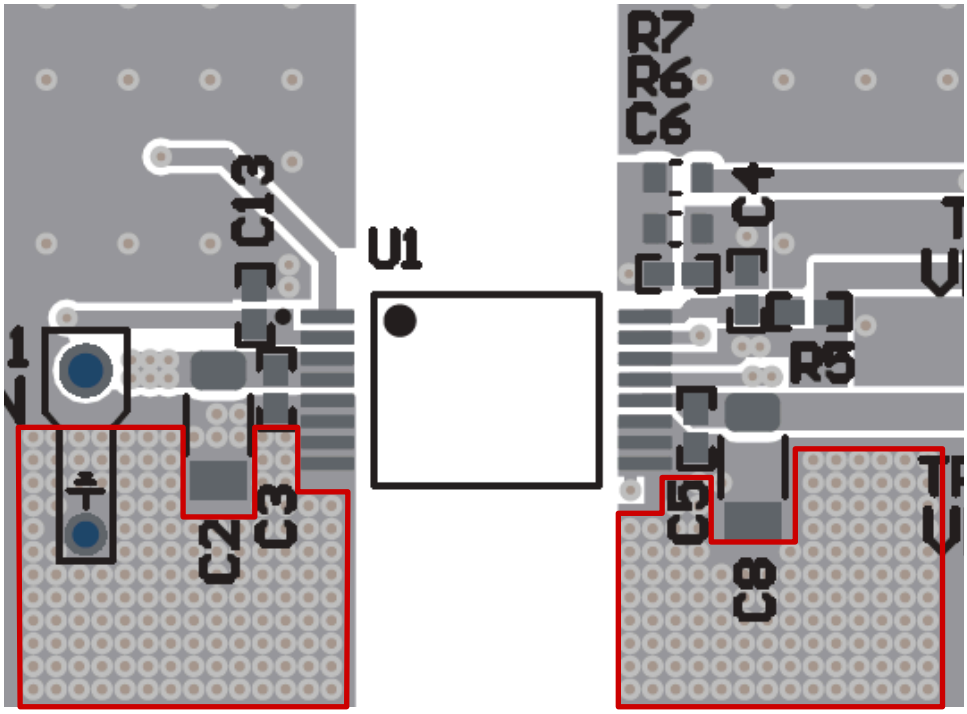

Figure 8-7. Thermal Vias

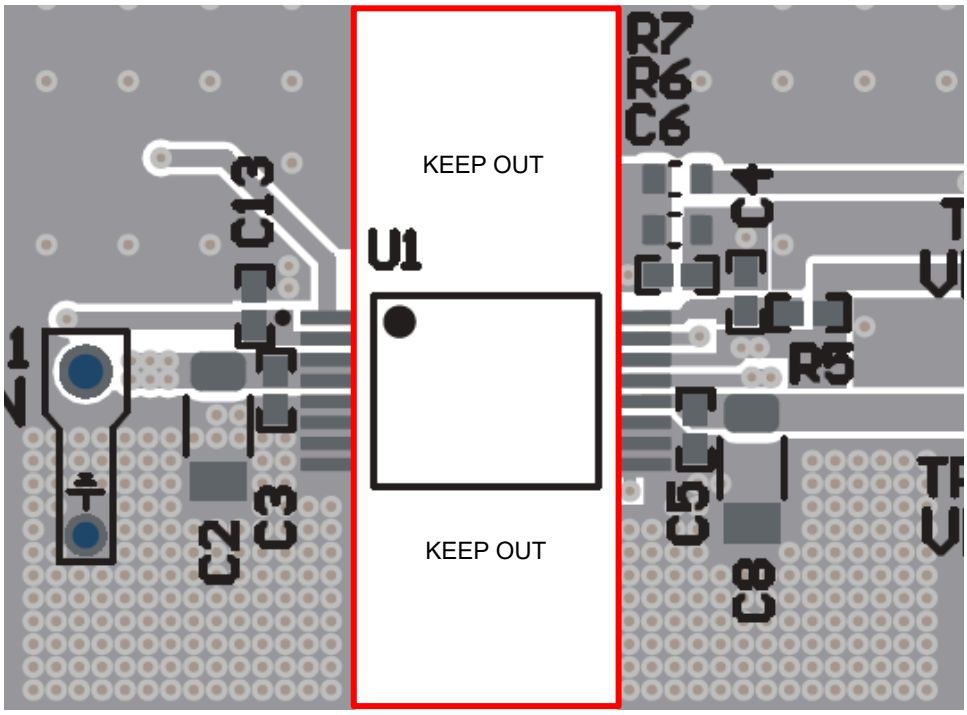

Figure 8-8. Isolation Keep Out Region

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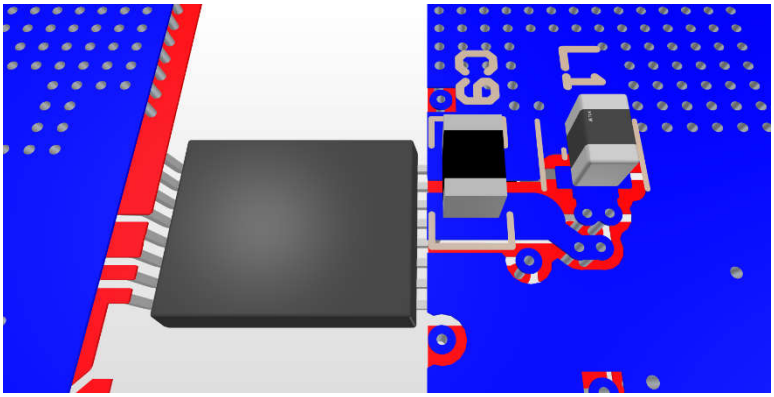

Figure 8-9. Bottom Side, Buck Boost, VEE LC Placement and Routing

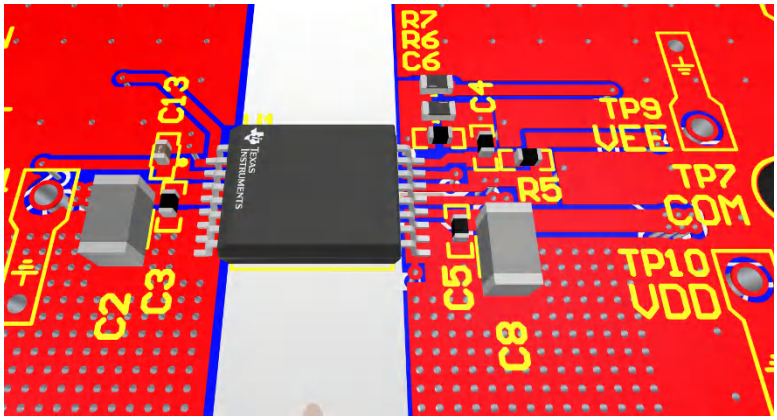

Figure 8-10. Top Side, Component Placement and Routing

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9 Device and Documentation Support

9.1 Third-Party Products Disclaimer

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9.2 Documentation Support

9.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Isolation Glossary*

9.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.
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9.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (August 2025) to Revision B (November 2025)	Page
• Updated Si PG version	1

Changes from Revision * (April 2025) to Revision A (August 2025)	Page
• Added Typical Characteristics section	12
• Added COM-VEE Output Capability seciton	20

ADVANCE INFORMATION

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

TI recommends to install the device with JEDEC standard J-STD-020 reflow process. The peak solder temperature should not exceed 260°C. If manual installation is needed durning testing process, TI recommends to limit the peak temperature not exceeding 260°C.

11.1 Packaging Information

Orderable Device	Status(1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan(2)	Lead finish/ Ball material(6)	MSL Peak Temp(3)	Op Temp (°C)	Device Marking(4) (5)
PUCC34141QDHARQ1	PREVIEW	SSOP	DHA	16					-40 to 125	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design. **PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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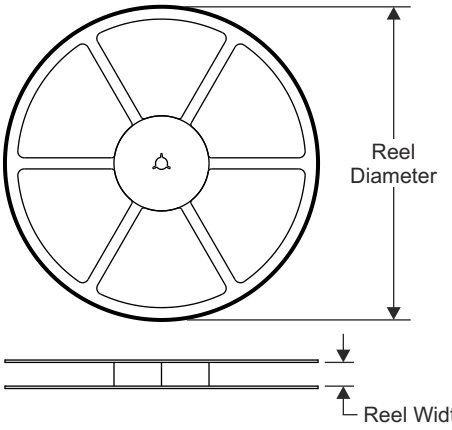
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

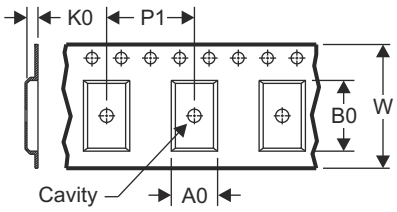
ADVANCE INFORMATION

11.2 Tape and Reel Information

REEL DIMENSIONS

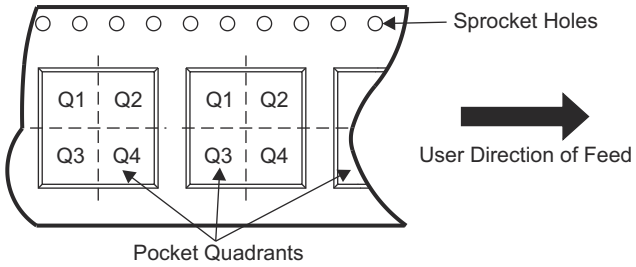


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

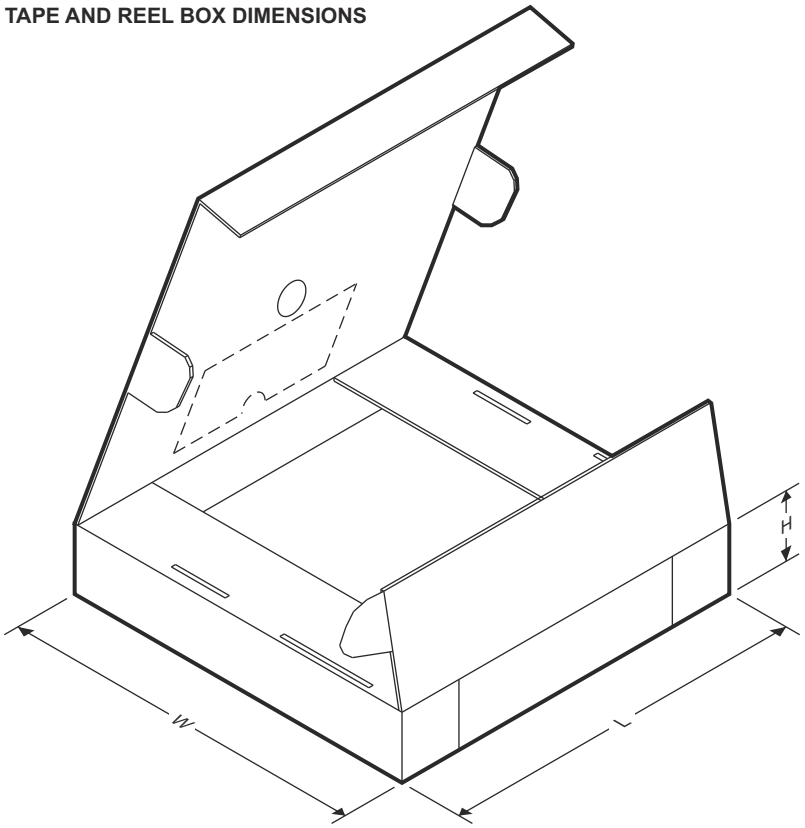
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PUCC34141QDHARQ1	SSOP	DHA	16									

ADVANCE INFORMATION

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PUCC34141QDHARQ1	SSOP	DHA	16				

ADVANCE INFORMATION

ADVANCE INFORMATION

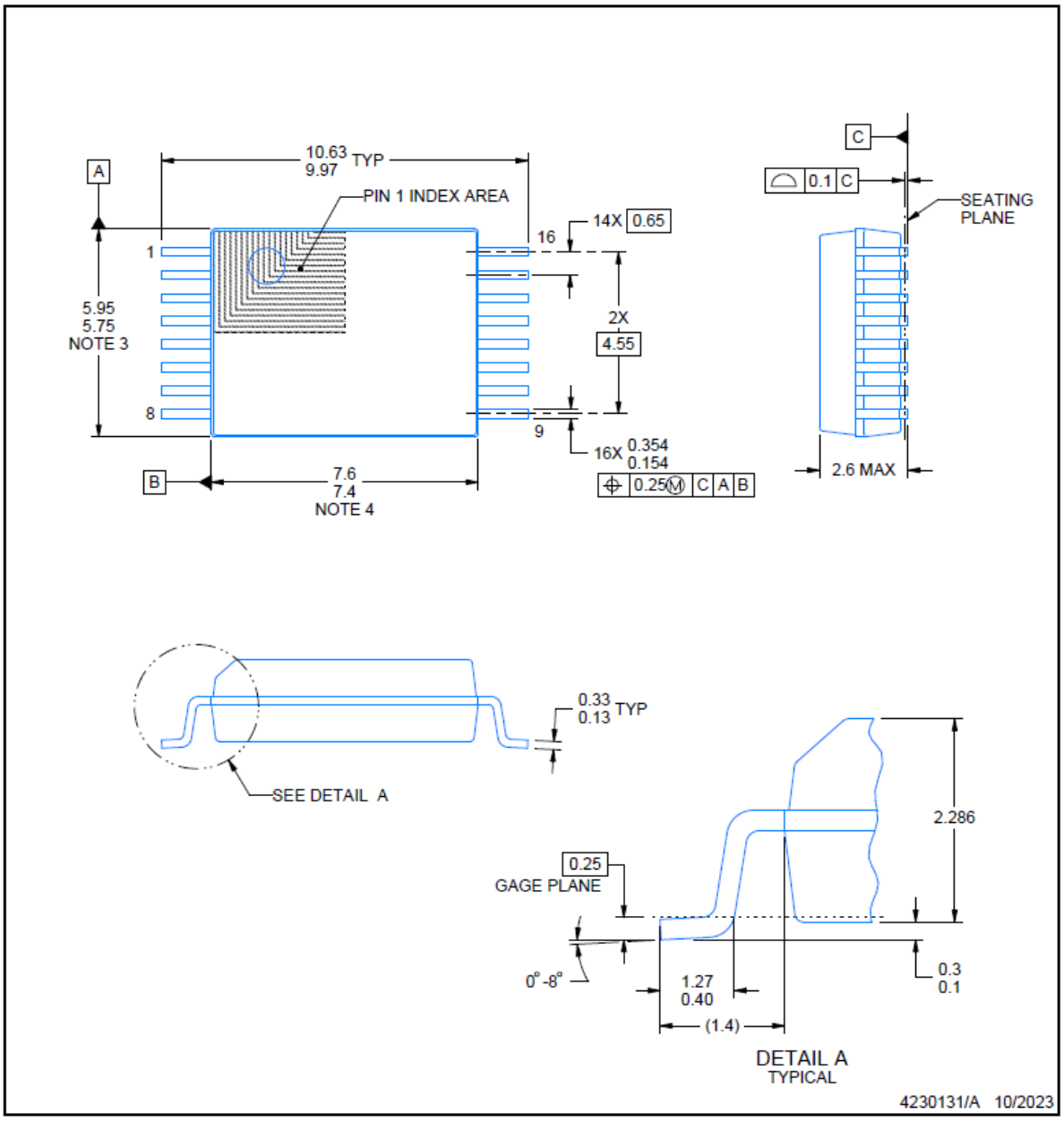
11.3 Mechanical Data

DHA0016A

PACKAGE OUTLINE

SSOP - 2.6 mm max height

SMALL OUTLINE PACKAGE



NOTES:

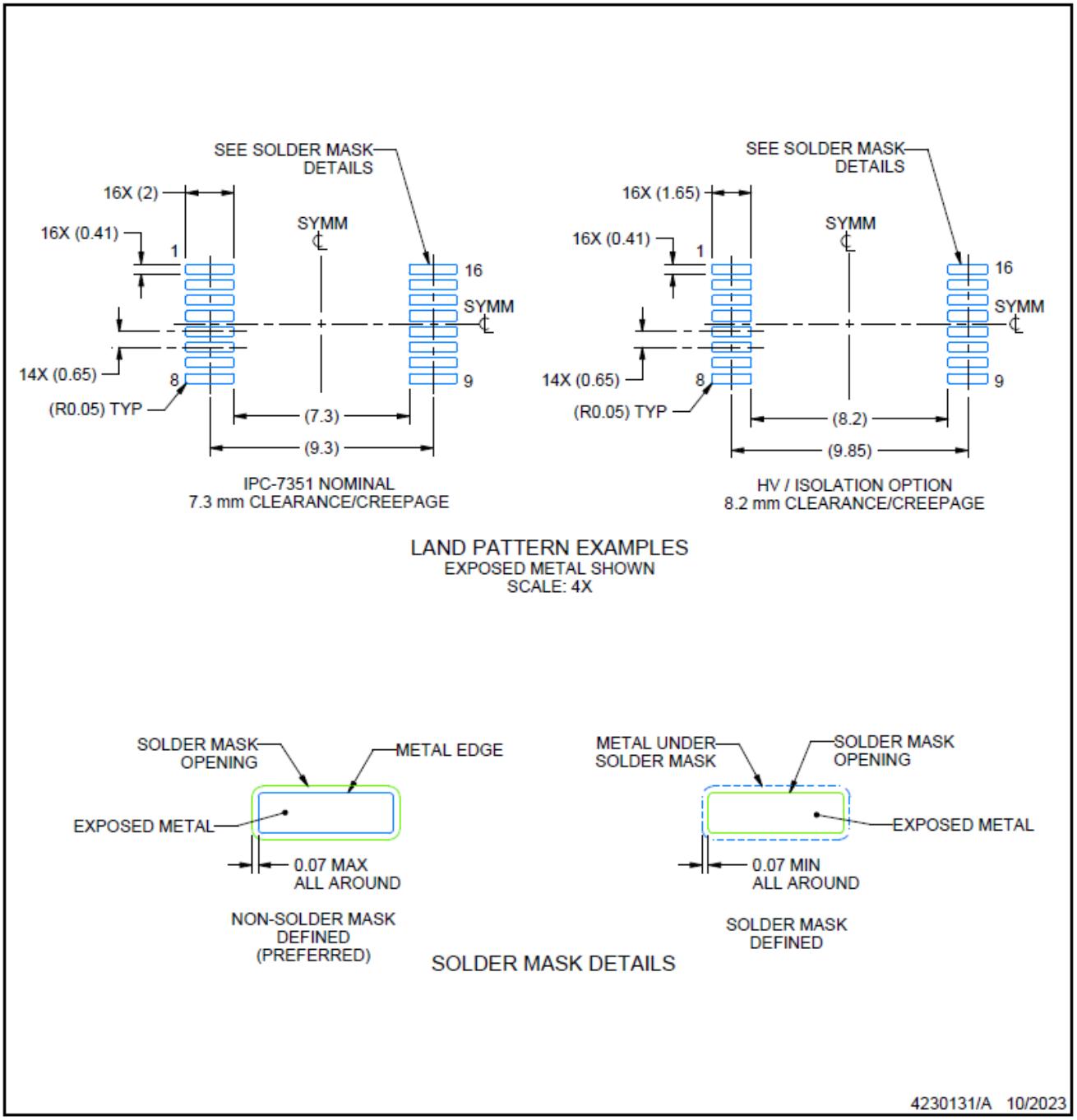
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.

EXAMPLE BOARD LAYOUT

DHA0016A

SSOP - 2.6 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

ADVANCE INFORMATION

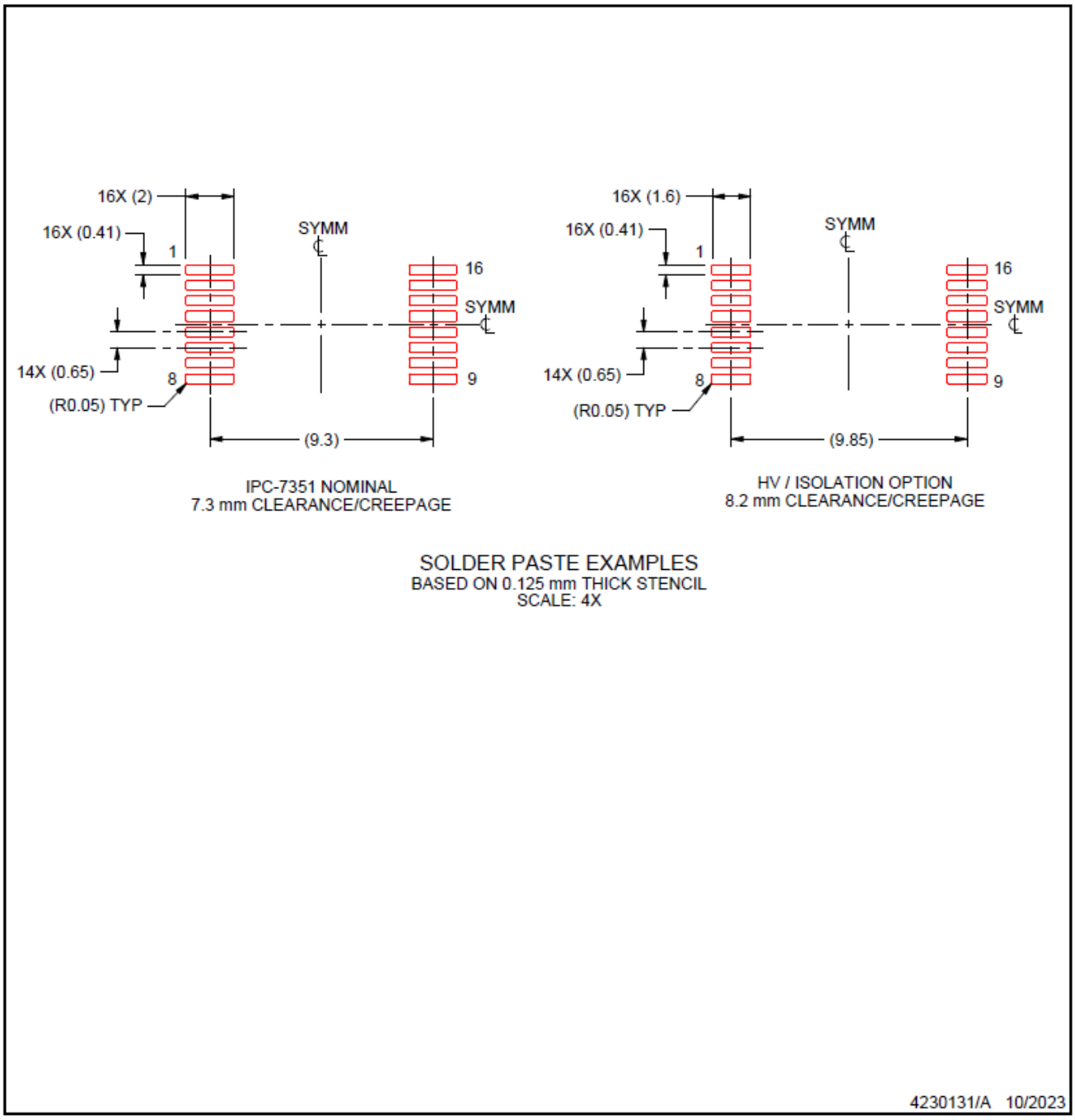
ADVANCE INFORMATION

EXAMPLE STENCIL DESIGN

DHA0016A

SSOP - 2.6 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PUCC34141QDHARQ1	Active	Preproduction	SO-MOD (DHA) | 16	1000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
PUCC34141QDHARQ1.A	Active	Preproduction	SO-MOD (DHA) | 16	1000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF UCC34141-Q1 :

- Military : UCC14141-Q1

NOTE: Qualified Version Definitions:

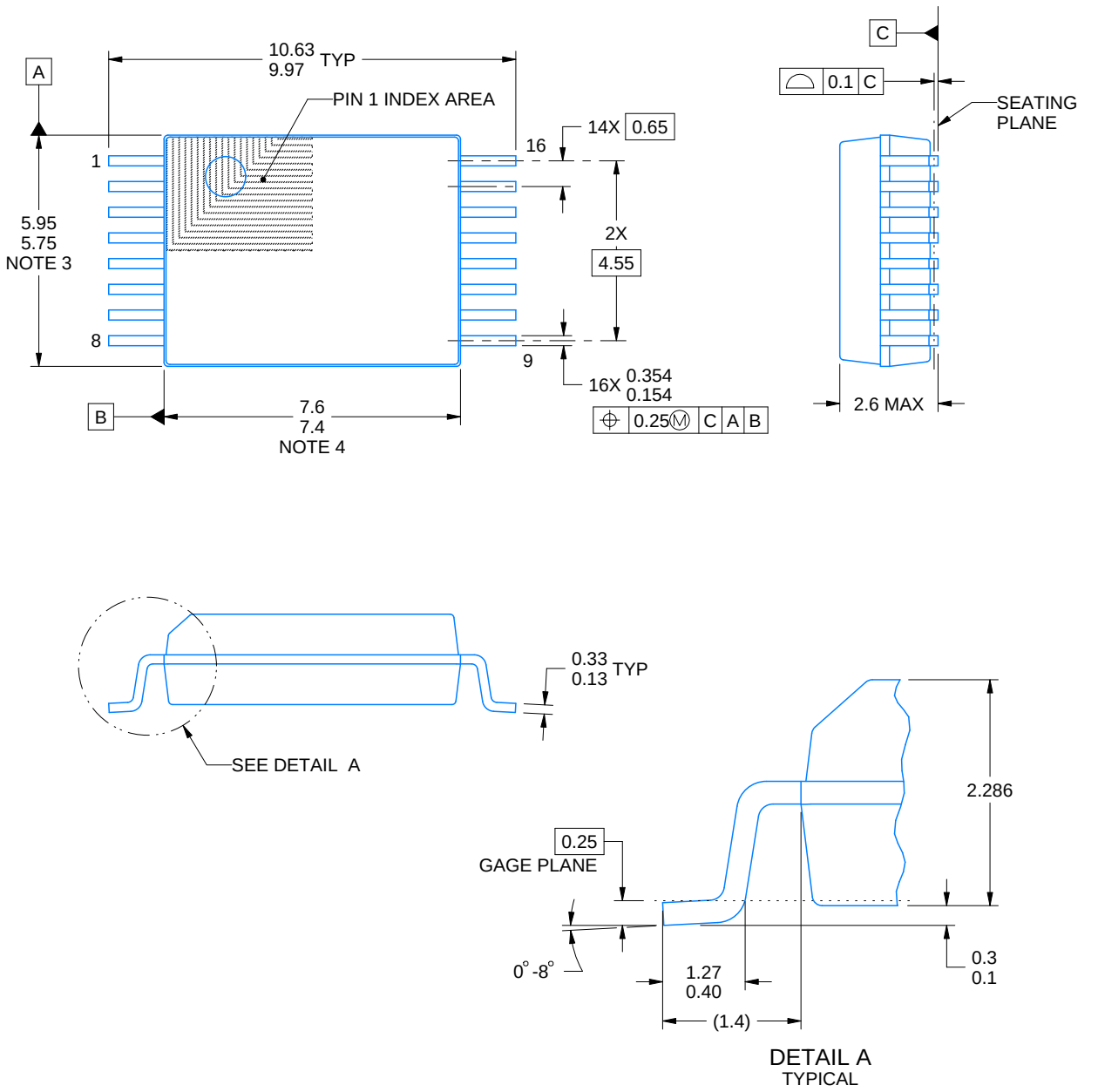
- Military - QML certified for Military and Defense Applications

PACKAGE OUTLINE

DHA0016A

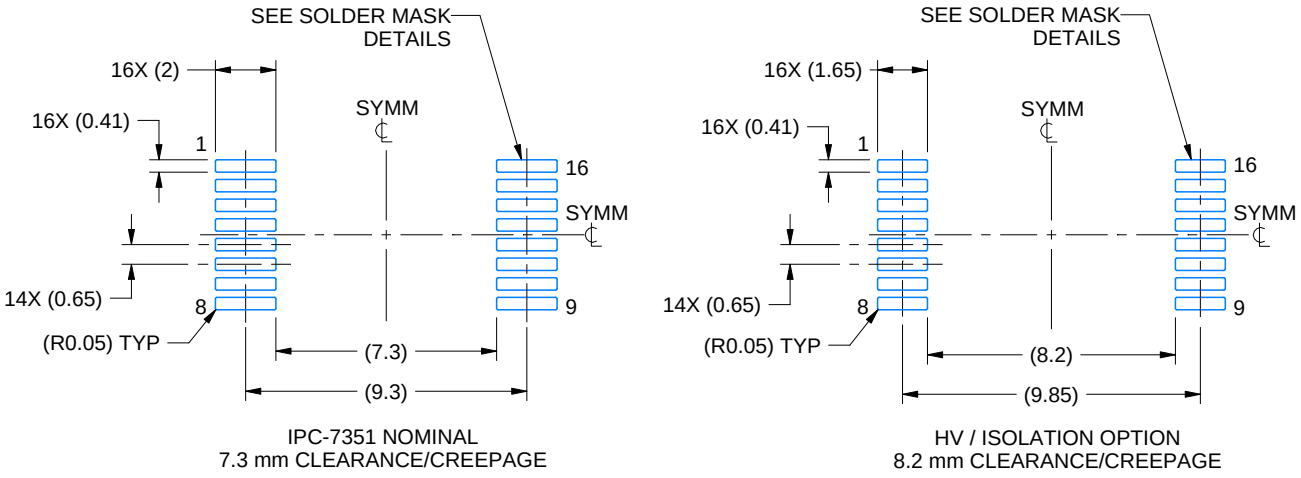
SSOP - 2.6 mm max height

SMALL OUTLINE PACKAGE

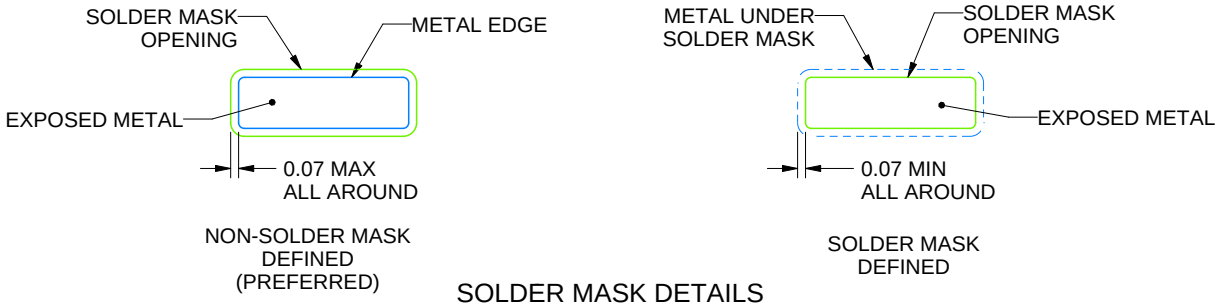


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.



LAND PATTERN EXAMPLES
EXPOSED METAL SHOWN
SCALE: 4X



SOLDER MASK DETAILS

4230131/A 10/2023

NOTES: (continued)

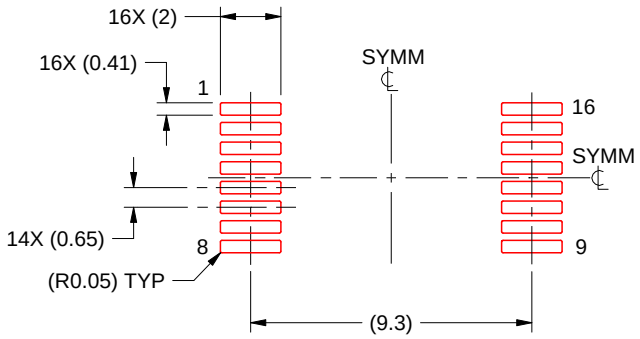
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

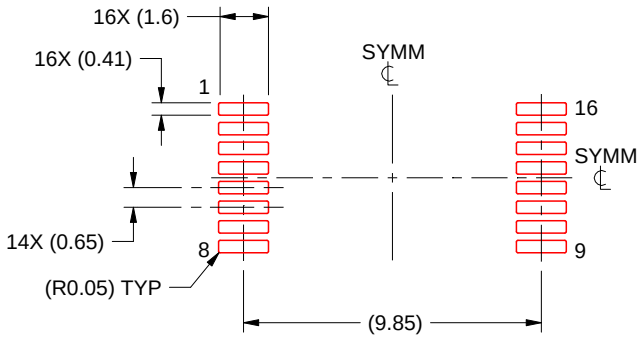
DHA0016A

SSOP - 2.6 mm max height

SMALL OUTLINE PACKAGE



IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE



HV / ISOLATION OPTION
8.2 mm CLEARANCE/CREEPAGE

SOLDER PASTE EXAMPLES
BASED ON 0.125 mm THICK STENCIL
SCALE: 4X

4230131/A 10/2023

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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