

Chipscale-Packaged bq24165, 24166, 24167 Evaluation Modules

The bq24165, 24166, 24167 evaluation module is a complete charger module for evaluating a compact, flexible, high-efficiency, USB-friendly, switch-mode charge management solution for single-cell, Li-ion and Li-polymer batteries used in a wide range of portable applications.

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1 Introduction

1.1 bq2416x IC Features

The bq24165, 24166, 24167 integrates a synchronous PWM controller, power MOSFETs, input current sensing, high-accuracy current and voltage regulation, charge termination and power path management into a chipscale package. Key integrated circuit (IC) features include:

- High-efficiency, fully integrated, NMOS-NMOS, synchronous buck charger with 1.5-MHz frequency
- Integrated power FETs for up to 2.5-A charge rate
- Power path management between battery and system voltages

For details, see the bq24165, 24166, 24167 data sheet ([SLUSAP4](#)).

1.2 bq24165, 24166, 24167 EVM Features

The bq24165, 24166, 24167 evaluation module (EVM) is a complete charger module for evaluating compact, flexible, high-efficiency, USB-friendly, switch-mode battery charge and power path management solution for single-cell, Li-ion and Li-polymer battery-powered systems used in a wide range of portable applications. Key EVM features include:

- Programmable charge current, input current on, and V_{INDPM} threshold using jumpers
- Input power connectors for both USB input and ac adapter
- Programmable charge current, input current on, and V_{INDPM} threshold using jumpers
- IN operating range of 4.2 V – 10 V
- USB operating range of 4.2 V – 6 V
- LED indication for status signals
- Test points for key signals available for testing purposes. Easy probe hook-up

1.3 Schematic

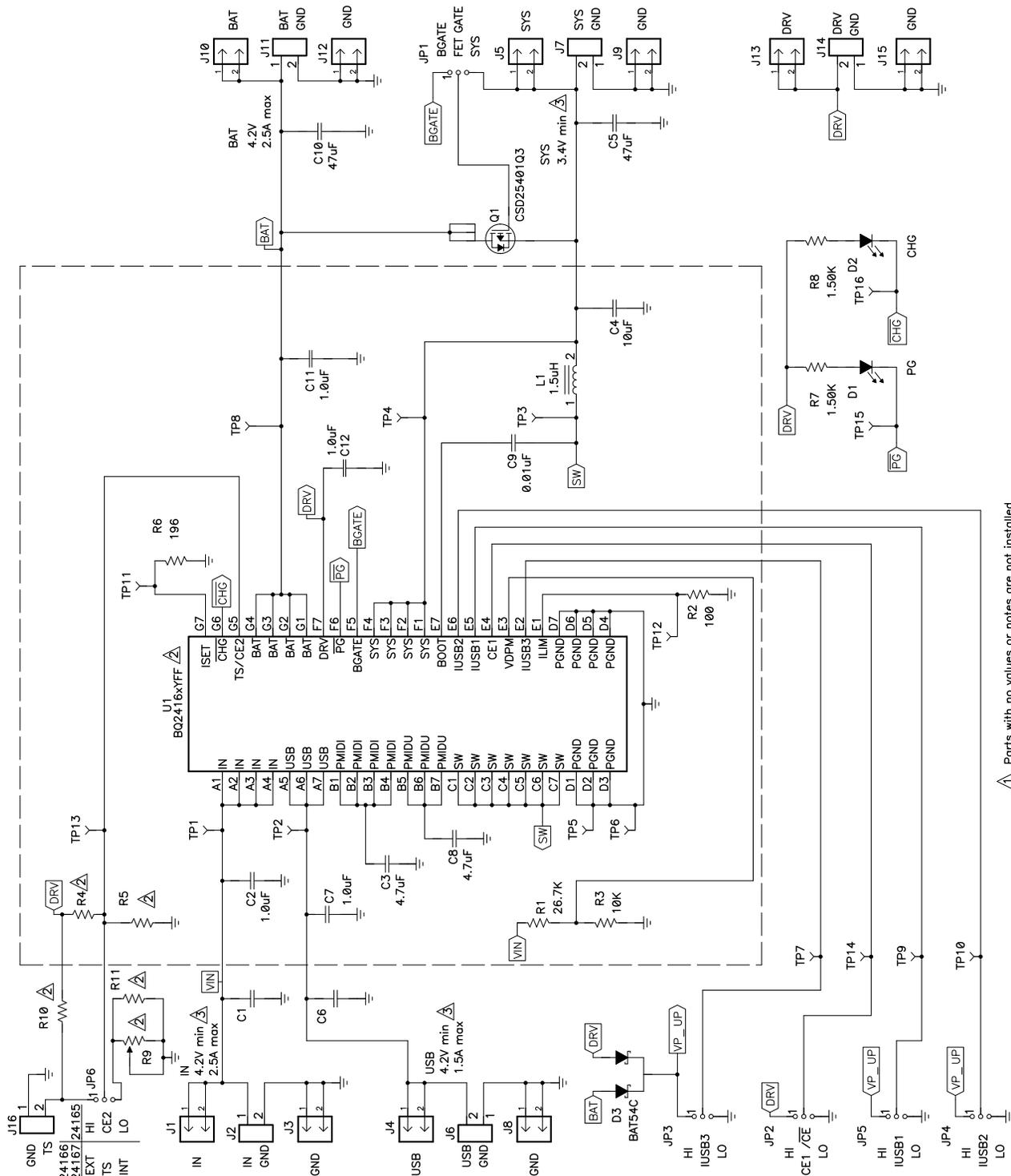


Figure 1. bq24165/166/167EVM (HPA741) Schematic

NOTE: EVMs with a printed-circuit board label that contain the suffix -X may have been assembled with incorrectly marked ICs. Regardless of the IC's marking, the EVM was assembled with the correct part number as specified in the EVM bill of material.

- △ Parts with no values or notes are not installed
- △ See BOM for values
- △ See datasheet for explanation of full voltage range

1.4 I/O Description

Header/Terminal Block	Description
J1-IN	Adapter positive header
J2-IN	Adapter positive terminal
J2-GND	Adapter negative terminal
J3-GND	Adapter negative header
J4-USB	USB positive header
J5-SYS	System output positive header
J6-USB	USB positive terminal
J6-GND	USB negative terminal
J7-SYS	System output positive terminal
J7-GND	System output negative terminal
J8-GND	USB negative header
J9-GND	System output negative header
J10-BAT+	Battery positive header
J11-BAT+	Battery positive terminal
J11-GND	Battery negative terminal
J12-GND	Battery negative header
J13-DRV	DRV reference voltage positive header
J14-DRV	DRV reference voltage positive terminal
J14-GND	DRV reference voltage negative terminal
J15-GND	DRV reference voltage negative header
J16-IN	External thermistor positive terminal
J16-GND	Ground connection for external thermistor

1.5 Test Points

Test Point	Description
TP1	Kelvin to IN
TP2	Kelvin to USB
TP3	SW
TP4	Kelvin to SYS
TP5	GND
TP6	GND
TP7	IUSB3
TP8	Kelvin to BAT
TP9	IUSB1
TP10	IUSB2
TP11	ISET
TP12	ILIM
TP13	$\overline{CE}2$ for bq24165 or TS for bq24166/167
TP14	$\overline{CE}1$ for bq24165 or \overline{CE} for bq24166/167

1.6 Control and Key Parameters Setting

IC	Jumper	Description	Default Factory Setting
All	JP1	1-2: FET GATE = BGATE: External PFET's gate tied to BGATE pin and therefore controlled by IC. 2-3: FET GATE = SYS: External PFET's gate tied to SYS and therefore disabled. It is recommended that this jumper be changed only when the device is not enabled or in Hi-Z mode so that the PFET's gate is never left open.	1-2 (FET GATE = BGATE)
bq24165	JP2	1-2: $\overline{CE1}$ = HI: Active-low enable for reduced VBAT voltage (if CE2 = LO) or suspended charging (if CE2 = HI) 2-3: $\overline{CE1}$ = LO: Active-low enable for full current charging (if CE2 = LO) or charging at half current (if CE2 = HI)	2-3 ($\overline{CE1}$ = LO)
bq24166 bq24167	JP2	1-2: \overline{CE} = HI: Active-low charge enable high to disable charge and enter Hi-Z mode 2-3: \overline{CE} = LO: Active-low charge enable low for normal operation	2-3 (\overline{CE} = LO)
All	JP3	1-2: IUSB3 = HI 2-3: IUSB3 = LO See data sheet Table 1 for description of USB input current limit and VINDPM threshold setting. Default setting is for 500-mA input current limit and 4.68-V threshold.	2-3 (IUSB3 = LO)
All	JP4	1-2: IUSB2 = HI 2-3: IUSB2 = LO See data sheet Table 1 for description of USB input current limit and VINDPM threshold setting. Default setting is for 500-mA input current limit and 4.68-V threshold.	2-3 (IUSB2 = LO)
All	JP5	1-2: IUSB1 = HI 2-3: IUSB1 = LO See data sheet Table 1 for description of USB input current limit and VINDPM threshold setting. Default setting is for 500-mA input current limit and 4.68-V threshold.	1-2 (IUSB1 = HI)
bq24165	JP6	1-2 ($\overline{CE2}$ = HI): Active-low enable for charging at half current (if $\overline{CE1}$ = LO) or suspended charging (if CE1 = HI) 2-3 ($\overline{CE2}$ = LO): Active-low enable for full current charging (if $\overline{CE1}$ = LO) or reduced VBAT voltage (if $\overline{CE1}$ = HI)	2-3 ($\overline{CE2}$ = LO)
bq24166 bq24167	JP6	1-2 (TS = EXT): Connects the TS pin to an external thermistor. The resistor divider formed by R4 and R5 has been sized to accommodate a 10-k Ω thermistor. If a different thermistor is used, R4 and R5 need to be resized. 2-3 (TS = INT): Connects a potentiometer to the TS pin so the potentiometer can emulate a thermistor. The potentiometer has been preset to approximately 3.4 k Ω so that the TS voltage is 0.5 x V(DRV).	2-3 (TS = INT)

1.7 Recommended Operating Conditions

		Min	Typ	Max	Unit
Supply voltage, V_{IN}	Operating input voltage from ac adapter	4.2		10	V
USB voltage, V_{USB}	Operating input voltage from USB or equivalent supply	4.2		6	V
Battery voltage, V_{BAT}	Voltage applied at VBAT terminal (depends on status of $\overline{CE1}$ and $\overline{CE2}$)	4.02	4.2	4.24	V
System voltage, V_{SYS}	Voltage output at SYS terminal (depends on VBAT voltage and status of V_{INDPM})	3.4		4.37	V
Supply current, $I_{IN(MAX)}$	Maximum input current limit for ac adapter input (set by user-selectable resistor)	1.5		2.5	A
Supply current, $I_{USB(MAX)}$	Maximum input current limit for USB input (set by USBx input pins)	0.1	0.5	1.5	A
Max fast charge current, $I_{CHRG(MAX)}$	Battery charge current	0.550		2.5	A
Operating junction temperature range, T_J		-40		125	$^{\circ}$ C

2 Test Summary

This procedure describes one test configuration of the HPA741 evaluation board for bench evaluation.

2.1 Definitions

The following naming conventions are followed.

VXXX :	External voltage supply name (VIN, VUSB)
LOAD#:	External load name
V(TPyyy):	Voltage at internal test point TPyyy. For example, V(TP12) means the voltage at TP12.
V(Jxx):	Voltage at header Jxx
V(TP(XXX)):	Voltage at test point XXX. For example, V(ACDET) means the voltage at the test point which is marked as ACDET.
V(XXX, YYY):	Voltage across point XXX and YYY.
I(JXX(YYY)):	Current going out from the YYY terminal of header XX.
Jxx(BBB):	Terminal or pin BBB of header xx
JPx ON :	Internal jumper Jxx terminals are shorted.
JPx OFF:	Internal jumper Jxx terminals are open.
JPx (-YY-)	ON: Internal jumper Jxx adjacent terminals marked as YY are shorted.
Measure: → A,B	Check specified parameters A, B. If measured values are not within specified limits the unit under test has failed.
Observe → A,B	Observe if A, B occur. If they do not occur, the unit under test has failed.

Assembly drawings have location for jumpers, test points, and individual components.

2.2 Recommended Test Equipment

2.2.1 Power Supplies

1. Power Supply number 1 (PS1) capable of supplying 6 V at 3 A is required.
2. If not using a battery as the load, then power supply number 2 (PS2) capable of supplying up to 5 V at 5 A is required to power the circuit shown in [Figure 2](#).

2.2.2 Load #1 between BAT and GND

Testing with an actual battery is the best way to verify operation in the system. If a battery is unavailable, then a circuit similar to the one shown in [Figure 2](#) can simulate a battery when connected to a second power supply.

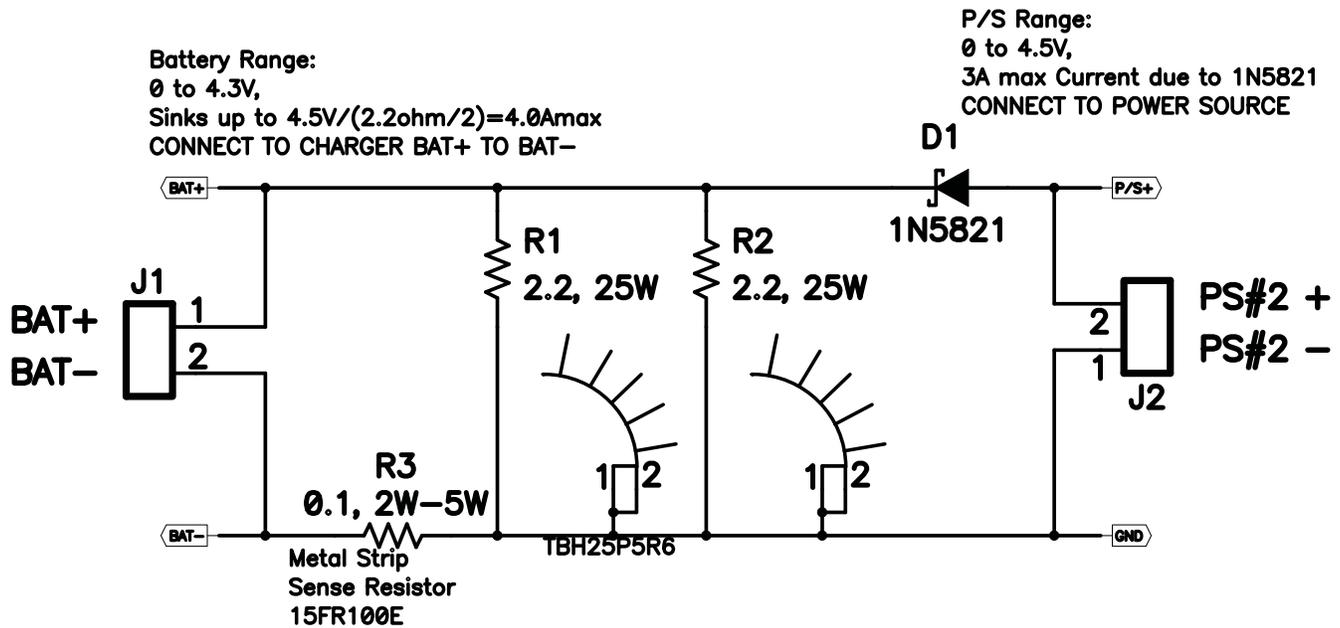


Figure 2. BAT Load (PR1010) Schematic

2.2.3 Load #2 Between SYS and GND

Although not required, a resistive load capable of sinking up to 3 A can be used.

2.2.4 Meters

Four equivalent voltage meters (VMx) and two equivalent current meters (CMx) are required. The current meters must be able to measure at least 3-A current.

2.3 Recommended Test Equipment Setup

1. For all power connections, use short, twisted-pair wires of appropriate gauge wire for the amount of the current.
2. Set Power Supply number 1 for 6 V \pm 100 mV, 3-A current limit, and then turn off supply.
3. If BAT_Load (PR1010) as shown in Figure 2 is used, connect Power Supply number 2 (PS2) set to approximately 3.6 V to the input side (PS2+/-) of BAT_Load (PR1010), then turn off PS2.
4. Connect the output side of the battery or BAT_Load (PR1010) in series with current meter (multimeter) number 2 (CM2) to J2 and J6 or J3 (BAT, GND). Ensure that a voltage meter is connected across J2 or TP3 and J6 or TP9 (BAT, GND).
5. Connect VM3 across J5 or TP4 and J9 (SYS, GND).
6. Connect VM4 across J13 and J15 (DRV, GND).
7. Ensure jumpers are at the default factory settings per Section 1.6
8. After the preceding steps are accomplished, the test setup for HPA741 is as shown in Figure 3

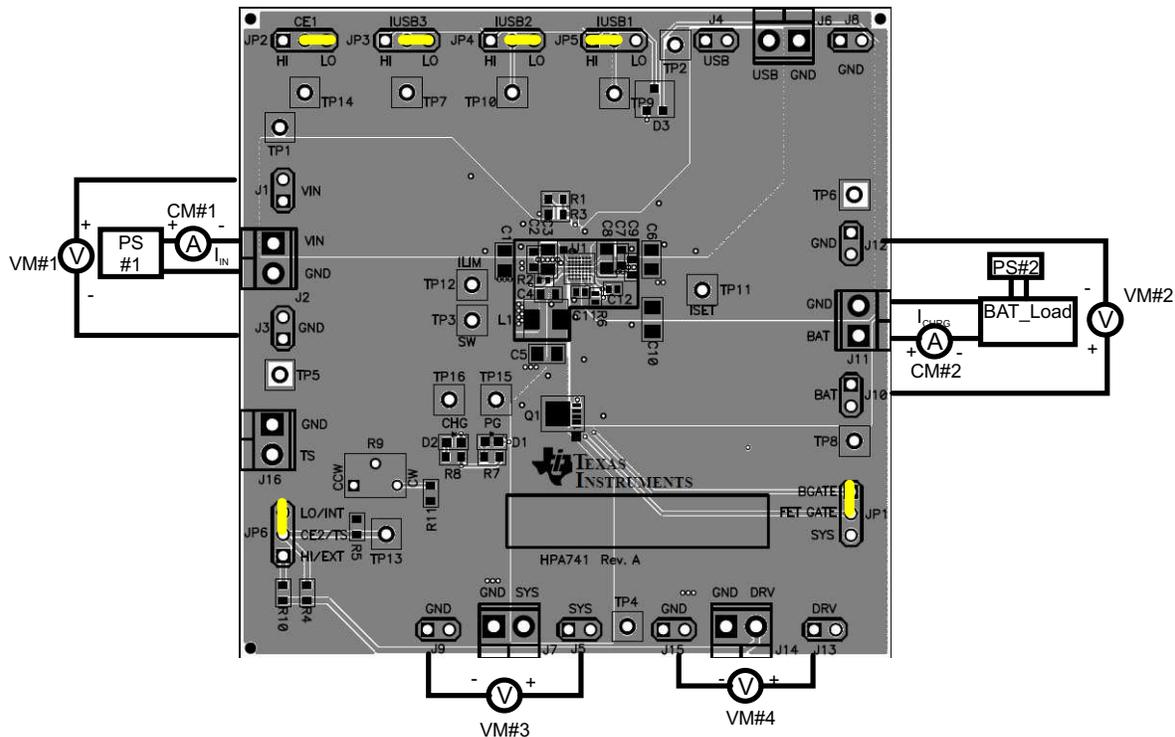


Figure 3. Original Test Setup for bq24165/166/167 EVM (HPA741)

2.4 Recommended Test Procedure

The following test procedure may be useful for evaluating the charger IC outside of a real system, if no battery is available to connect to the output and a simulated battery is needed.

2.4.1 Charge Voltage and Current Regulation of IN

1. Ensure that the [Section 2.3](#) steps are followed.
2. Move JP2 ($\overline{CE1}$ or \overline{CE}) = HI and JP6 = HI.
3. Connect the output of Power Supply #1 (PS #1) in series with current meter number 1 (CM1) to J2 (IN, GND).
4. Connect voltage meter number 1 (VM1) across J1 or TP1 and J3 or TP6 (IN, GND).
5. With PS2 disabled, turn on PS1.
6. Measure:
 - Measure on VM3 $\rightarrow V(J5/TP4(SYS), J9(GND)) = 4.3 \pm 100 \text{ mV}$
 - Measure on VM4 $\rightarrow V(J13(DRV), J15(GND)) = 5.2 \pm 200 \text{ mV}$
7. Move JP2 ($\overline{CE1}$ or \overline{CE}) = LO and JP6 = LO. Adjust the power supply so that VM1 still reads $6 \text{ V} \pm 100 \text{ mV}$ if necessary.
8. Enable PS2 and adjust PS2 so that the voltage measured by VM2, across BAT and GND, measures $3.2 \text{ V} + 50 \text{ mV}$
9. Measure and Observe:
 - Measure on CM2 $\rightarrow I_{\text{CHRG}} = 2500 \text{ mA} \pm 150 \text{ mA}$
 - Measure on CM1 $\rightarrow I_{\text{IN}} = 1800 \text{ mA} \pm 180 \text{ mA}$
 - Observe \rightarrow D1 and D2 are on.
10. Turn off PS1 and PS2.

2.4.2 Charge Voltage and Current Regulation of USB

1. Ensure that the [Section 2.3](#) steps are followed.
2. Move JP2 ($\overline{CE1}$ or \overline{CE}) = HI and JP6 = HI.
3. Connect the output of Power Supply number 1 (PS1) in series with current meter (multimeter) number 1 (CM1) to J4 and J8 or J6 (USB, GND).
4. Connect voltage meter 1 (VM1) across J4 or TP2 and J8 or TP5 (USB, GND).
5. With PS2 disabled, turn on PS1.
6. Measure:
Measure on VM3 → $V(J5/TP4(SYS),J9(GND)) = 4.3 \pm 100 \text{ mV}$
Measure on VM4 → $V(J13(DRV),J15(GND)) = 5.2 \pm 200 \text{ mV}$
7. Move JP2 ($\overline{CE1}$ or \overline{CE}) = LO and JP6 = LO while keeping the default settings for JP3 (USB3), JP4 (USB2) and JP5 (USB1). Adjust PS1 so that VM1 still reads $6 \text{ V} \pm 100 \text{ mV}$ if necessary.
8. Enable PS2 and adjust PS2 so that the voltage measured by VM2, across BAT and GND, measures $3.2 \text{ V} \pm 50 \text{ mV}$.
9. Measure:
Measure on CM2 → $I_{\text{CHRG}} = 735 \text{ mA} \pm 75 \text{ mA}$
Measure on CM1 → $I_{\text{IN}} = 475 \text{ mA} \pm 50 \text{ mA}$
Observe → D1 and D2 are on.
10. Turn off PS1 and PS2.

2.4.3 Helpful hints

1. To observe the taper current as the battery voltage approaches the set regulation voltage, allow the battery to charge or, if using BAT_Load (PR1010), slowly increase the PS2 voltage powering BAT_Load (PR1010). Use VM2 across BAT and GND to measure the battery voltage seen by the IC.
2. To observe the V_{INDPM} function, lower the current limit on PS1.
3. To observe battery supplement mode, apply a resistive load across SYS and GND that is higher than the maximum charge current.

3 Printed-Circuit Board Layout Guideline

1. To obtain optimal performance, the power input capacitors, connected from the PMID input to PGND, must be placed as close as possible to the bq2416x.
2. Place 4.7- μ F input capacitor as close to PMID pin and PGND pin as possible to make high-frequency current loop area as small as possible. Place 1- μ F input capacitor GNDs as close to the respective PMID capacitor GND and PGND pins as possible to minimize the ground difference between the input and PMID_.
3. The local bypass capacitor from SYS to GND must be connected between the SYS pin and PGND of the IC. The intent is to minimize the current path loop area from the SW pin through the LC filter and back to the PGND pin.
4. Place all decoupling capacitors close to their respective IC pins and as close as to PGND (do not place components such that routing interrupts power stage currents). All small control signals must be routed away from the high-current paths.
5. The PCB must have a ground plane (return) connected directly to the return of all components through vias (two vias per capacitor for power-stage capacitors, one via per capacitor for small-signal components). It is also recommended to put vias inside the PGND pads for the IC, if possible. A star ground design approach is typically used to keep circuit block currents isolated (high-power/low-power small-signal) which reduces noise-coupling and ground-bounce issues. A single ground plane for this design gives good results. With this small layout and a single ground plane, no ground-bounce issue occurs, and having the components segregated minimizes coupling between signals.
6. The high-current charge paths into IN, USB, BAT, SYS, and from the SW pins must be sized appropriately for the maximum charge current in order to avoid voltage drops in these traces. The PGND pins must be connected to the ground plane to return current through the internal low-side FET.
7. For high-current applications, the balls for the power paths must be connected to as much copper in the board as possible. This allows better thermal performance because the board conducts heat away from the IC.

4 Bill of Materials and Board Layout

4.1 Bill of Materials

Table 1. Bill of Materials - HPA741A

Count			RefDes	Value	Description	Size	Part Number	MFR
-001	-002	-003						
0	0	0	C1, C6	Open	Capacitor, Ceramic	805	Std	Std
2	2	2	C2, C7	1.0 μ F	Capacitor, Ceramic, 25V, X5R, 10%	603	Std	Std
2	2	2	C3, C8	4.7 μ F	Capacitor, Ceramic, 25V, X5R, 10%	805	Std	Std
1	1	1	C4	10 μ F	Capacitor, Ceramic, 10V, X5R, 20%	603	Std	Std
1	1	1	C5	47 μ F	Capacitor, Ceramic, 6.3V, X5R, 20%	805	Std	Std
1	1	1	C9	0.01 μ F	Capacitor, Ceramic, 16V, X7R, 10%	603	Std	Std
1	1	1	C10	47 μ F	Capacitor, Ceramic, 6.3V, X5R, 20%	1206	Std	Std
2	2	2	C11, C12	1.0 μ F	Capacitor, Ceramic, 6.3V, X5R, 10%	402	Std	Std
2	2	2	D1, D2	LTST-C190GKT	Diode, LED, Green, 2.1-V, 20-mA, 6-mcd	603	LTST-C190GKT	Liteon
1	1	1	D3	BAT54C	Diode, Dual Schottky, 200-mA, 30-V	SOT23	BAT54C	Fairchild
10	10	10	J1, J3, J4, J5, J8, J9, J10, J12, J13, J15	PEC02SAAN	Header, Male 2-pin, 100mil spacing,	0.100 inch x 2	PEC02SAAN	Sullins
5	5	5	J2, J6, J7, J11, J14	ED555/2DS	Terminal Block, 2-pin, 6-A, 3.5mm	0.27 x 0.25	ED555/2DS	OST
0	1	1	J16	ED555/2DS	Terminal Block, 2-pin, 6-A, 3.5mm	0.27 x 0.25	ED555/2DS	OST
6	6	6	JP1, JP2, JP3, JP4, JP5, JP6	PEC03SAAN	Header, Male 3-pin, 100mil spacing,	0.100 inch x 3	PEC03SAAN	Sullins
1	1	1	L1	1.5 μ H	Inductor, SMT, 3.5A, 70 m Ω	4.1 x 4.4 mm	SPM4012T-1R5M Alternate: FDSD0415-H-1R5M	TDK Alternate: Toko
1	1	1	Q1	CSD25401Q3	MOSFET, PChan, -20V, 60A, 8.7 m Ω	chipscale3.3X3.3mm	CSD25401Q3	TI
1	1	1	R1	26.7k Ω	Resistor, Chip, 1/16W, 1%	603	Std	Std
1	1	1	R2	100 Ω	Resistor, Chip, 1/16W, 1%	402	Std	Std
1	1	1	R3	10k Ω	Resistor, Chip, 1/16W, 1%	603	Std	Std
0	1	1	R4	1870 Ω	Resistor, Chip, 1/16W, 1%	603	Std	Std
0	1	1	R5	4120 Ω	Resistor, Chip, 1/16W, 1%	603	Std	Std
1	1	1	R6	196 Ω	Resistor, Chip, 1/16W, 1%	402	Std	Std
2	2	2	R7, R8	1.50k Ω	Resistor, Chip, 1/16W, 1%	603	Std	Std
0	1	1	R9	50.0k Ω	Potentiometer, 3/8 Cermet, 12-Turn	0.25x0.17 inch	3266W-1-503LF	Bourns
2	0	0	R10, R11	0	Resistor, Chip, 1/16W	603	Std	Std
14	14	14	TP1, TP2, TP3, TP4, TP7, TP8, TP9, TP10, TP11, TP12, TP13, TP14, TP15, TP16	5002	Test Point, White, Thru Hole Color Keyed	0.100 x 0.100 inch	5002	Keystone
2	2	2	TP5, TP6	5001	Test Point, Black, Thru Hole Color Keyed	0.100 x 0.100 inch	5001	Keystone

Table 1. Bill of Materials - HPA741A (continued)

Count			RefDes	Value	Description	Size	Part Number	MFR
-001	-002	-003						
1	0	0	U1	BQ24165YFF	IC, 2.5A, Dual-Input, Single Cell Switch-mode Li-Ion BATTERY CHARGER with	BGA	BQ24165YFF	TI
0	1	0	U1	BQ24166YFF	IC, 2.5A, Dual-Input, Single Cell Switch-mode Li-Ion BATTERY CHARGER with	BGA	BQ24166YFF	TI
0	0	1	U1	BQ24167YFF	IC, 2.5A, Dual-Input, Single Cell Switch-mode Li-Ion BATTERY CHARGER with	BGA	BQ24167YFF	TI
6	6	6	--		Shunt, 100-mil, Black	0.100	929950-00	3M

4.2 Board Layout

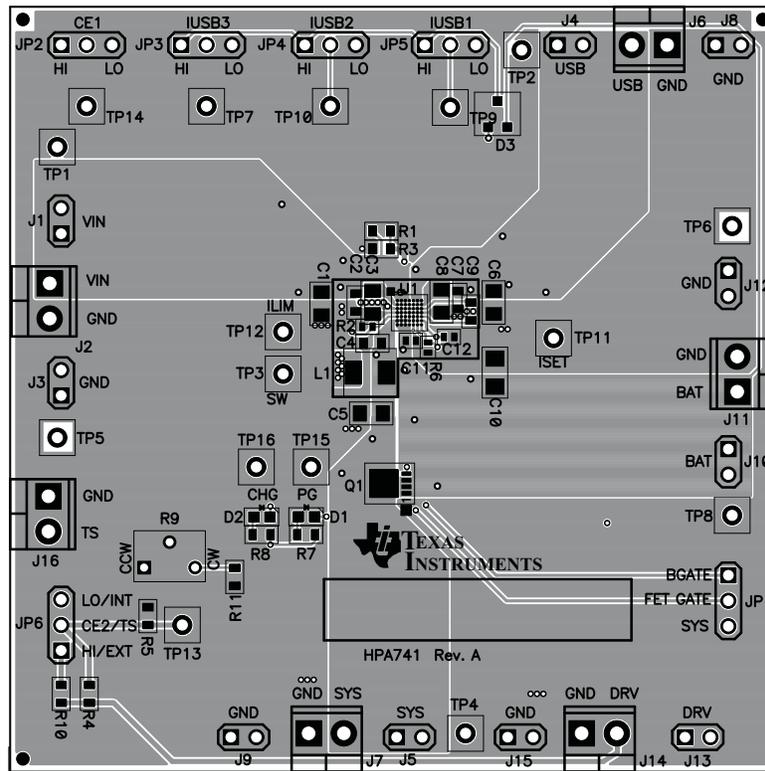


Figure 4. Top Assembly Layer

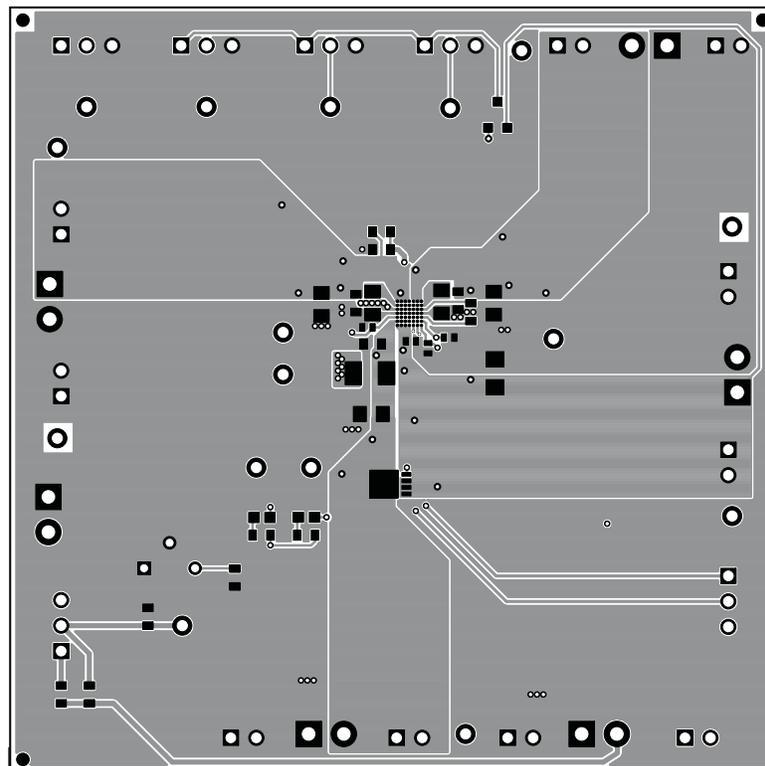


Figure 5. Top Layer

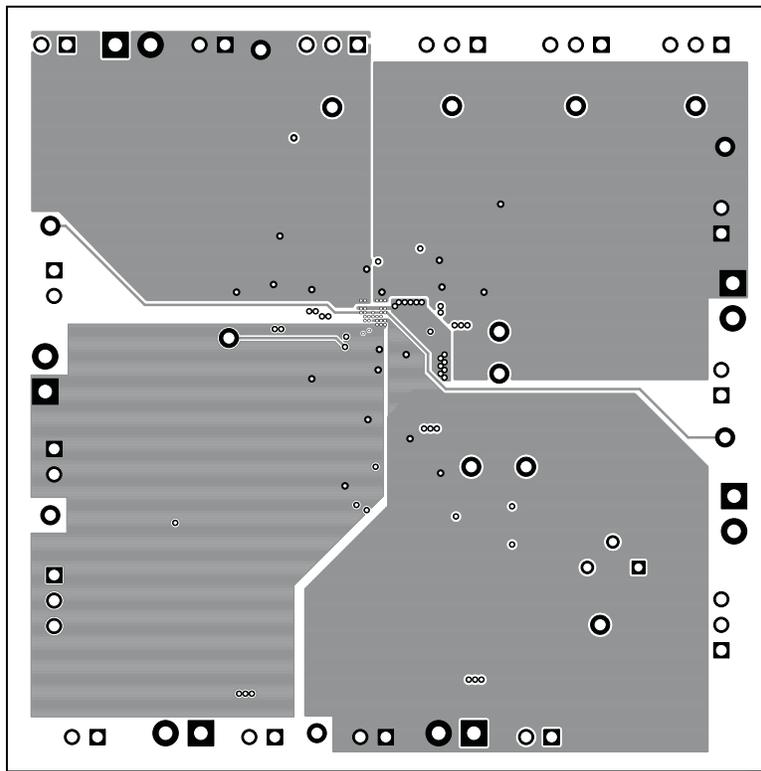


Figure 6. Bottom Layer

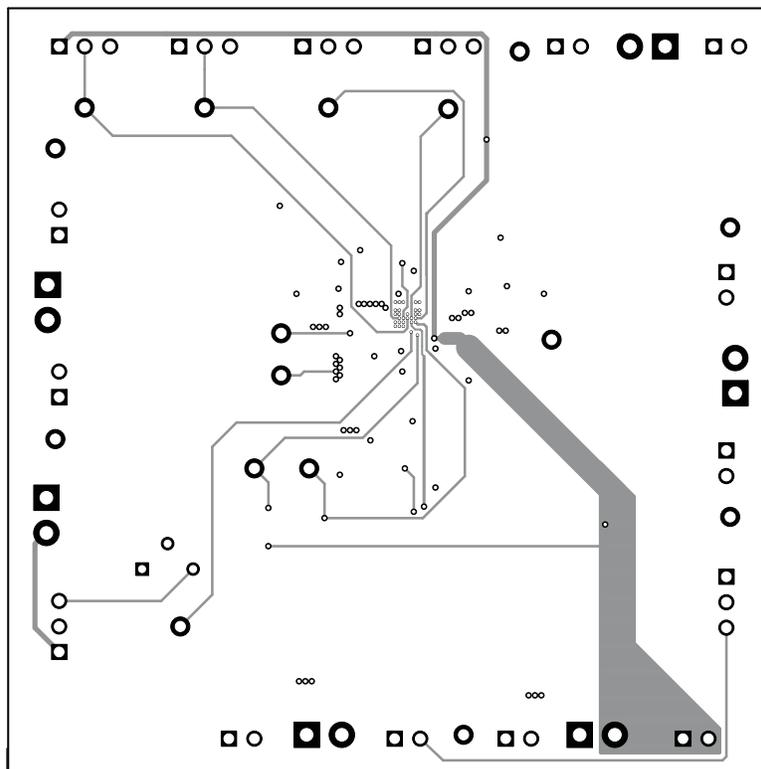


Figure 7. First Internal Layer

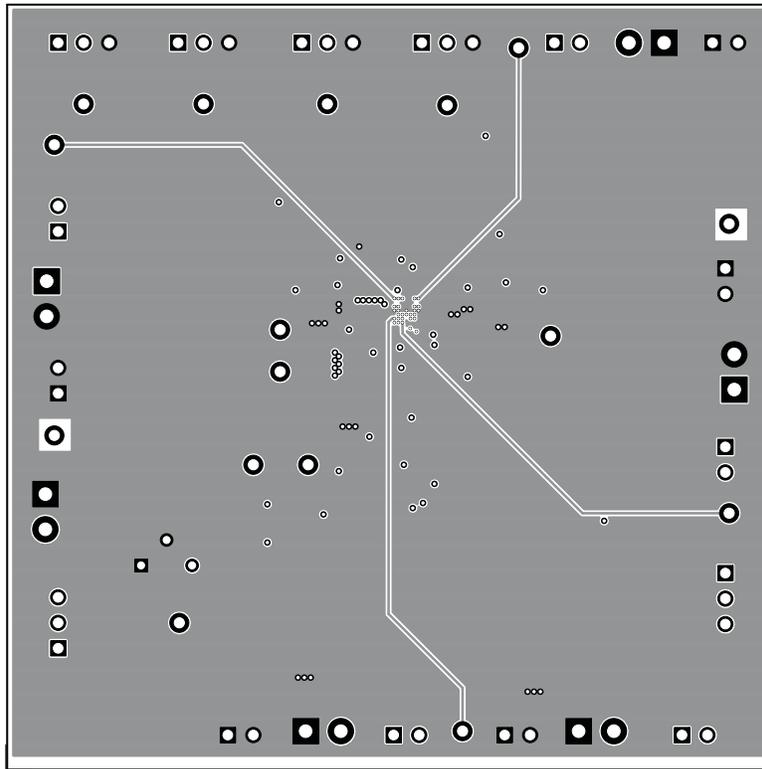


Figure 8. Second Internal Layer

EVALUATION BOARD/KIT/MODULE (EVM) ADDITIONAL TERMS

Texas Instruments (TI) provides the enclosed Evaluation Board/Kit/Module (EVM) under the following conditions:

The user assumes all responsibility and liability for proper and safe handling of the goods. Further, the user indemnifies TI from all claims arising from the handling or use of the goods.

Should this evaluation board/kit not meet the specifications indicated in the User's Guide, the board/kit may be returned within 30 days from the date of delivery for a full refund. THE FOREGOING LIMITED WARRANTY IS THE EXCLUSIVE WARRANTY MADE BY SELLER TO BUYER AND IS IN LIEU OF ALL OTHER WARRANTIES, EXPRESSED, IMPLIED, OR STATUTORY, INCLUDING ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR ANY PARTICULAR PURPOSE. EXCEPT TO THE EXTENT OF THE INDEMNITY SET FORTH ABOVE, NEITHER PARTY SHALL BE LIABLE TO THE OTHER FOR ANY INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES.

Please read the User's Guide and, specifically, the Warnings and Restrictions notice in the User's Guide prior to handling the product. This notice contains important safety information about temperatures and voltages. For additional information on TI's environmental and/or safety programs, please visit www.ti.com/esh or contact TI.

No license is granted under any patent right or other intellectual property right of TI covering or relating to any machine, process, or combination in which such TI products or services might be or are used. TI currently deals with a variety of customers for products, and therefore our arrangement with the user is not exclusive. TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein.

REGULATORY COMPLIANCE INFORMATION

As noted in the EVM User's Guide and/or EVM itself, this EVM and/or accompanying hardware may or may not be subject to the Federal Communications Commission (FCC) and Industry Canada (IC) rules.

For EVMs **not** subject to the above rules, this evaluation board/kit/module is intended for use for ENGINEERING DEVELOPMENT, DEMONSTRATION OR EVALUATION PURPOSES ONLY and is not considered by TI to be a finished end product fit for general consumer use. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to part 15 of FCC or ICES-003 rules, which are designed to provide reasonable protection against radio frequency interference. Operation of the equipment may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures may be required to correct this interference.

General Statement for EVMs including a radio

User Power/Frequency Use Obligations: This radio is intended for development/professional use only in legally allocated frequency and power limits. Any use of radio frequencies and/or power availability of this EVM and its development application(s) must comply with local laws governing radio spectrum allocation and power limits for this evaluation module. It is the user's sole responsibility to only operate this radio in legally acceptable frequency space and within legally mandated power limitations. Any exceptions to this are strictly prohibited and unauthorized by Texas Instruments unless user has obtained appropriate experimental/development licenses from local regulatory authorities, which is responsibility of user including its acceptable authorization.

For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant

Caution

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

For EVMs annotated as IC – INDUSTRY CANADA Compliant

This Class A or B digital apparatus complies with Canadian ICES-003.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

Concerning EVMs including radio transmitters

This device complies with Industry Canada licence-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concerning EVMs including detachable antennas

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication.

This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Cet appareil numérique de la classe A ou B est conforme à la norme NMB-003 du Canada.

Les changements ou les modifications pas expressément approuvés par la partie responsable de la conformité ont pu vider l'autorité de l'utilisateur pour actionner l'équipement.

Concernant les EVMs avec appareils radio

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes : (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante.

Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur.

【Important Notice for Users of this Product in Japan】

This development kit is NOT certified as Confirming to Technical Regulations of Radio Law of Japan

If you use this product in Japan, you are required by Radio Law of Japan to follow the instructions below with respect to this product:

1. Use this product in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use this product only after you obtained the license of Test Radio Station as provided in Radio Law of Japan with respect to this product, or
3. Use of this product only after you obtained the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to this product. Also, please do not transfer this product, unless you give the same notice above to the transferee. Please note that if you could not follow the instructions above, you will be subject to penalties of Radio Law of Japan.

Texas Instruments Japan Limited
(address) 24-1, Nishi-Shinjuku 6 chome, Shinjuku-ku, Tokyo, Japan

<http://www.tij.co.jp>

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日本テキサス・インスツルメンツ株式会社
東京都新宿区西新宿6丁目24番1号
西新宿三井ビル

<http://www.tij.co.jp>

EVALUATION BOARD/KIT/MODULE (EVM) WARNINGS, RESTRICTIONS AND DISCLAIMERS

For Feasibility Evaluation Only, in Laboratory/Development Environments. Unless otherwise indicated, this EVM is not a finished electrical equipment and not intended for consumer use. It is intended solely for use for preliminary feasibility evaluation in laboratory/development environments by technically qualified electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems and subsystems. It should not be used as all or part of a finished end product.

Your Sole Responsibility and Risk. You acknowledge, represent and agree that:

1. You have unique knowledge concerning Federal, State and local regulatory requirements (including but not limited to Food and Drug Administration regulations, if applicable) which relate to your products and which relate to your use (and/or that of your employees, affiliates, contractors or designees) of the EVM for evaluation, testing and other purposes.
2. You have full and exclusive responsibility to assure the safety and compliance of your products with all such laws and other applicable regulatory requirements, and also to assure the safety of any activities to be conducted by you and/or your employees, affiliates, contractors or designees, using the EVM. Further, you are responsible to assure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard.
3. You will employ reasonable safeguards to ensure that your use of the EVM will not result in any property damage, injury or death, even if the EVM should fail to perform as described or expected.
4. You will take care of proper disposal and recycling of the EVM's electronic components and packing materials.

Certain Instructions. It is important to operate this EVM within TI's recommended specifications and environmental considerations per the user guidelines. Exceeding the specified EVM ratings (including but not limited to input and output voltage, current, power, and environmental ranges) may cause property damage, personal injury or death. If there are questions concerning these ratings please contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, some circuit components may have case temperatures greater than 60°C as long as the input and output are maintained at a normal ambient operating temperature. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors which can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during normal operation, please be aware that these devices may be very warm to the touch. As with all electronic evaluation tools, only qualified personnel knowledgeable in electronic measurement and diagnostics normally found in development environments should use these EVMs.

Agreement to Defend, Indemnify and Hold Harmless. You agree to defend, indemnify and hold TI, its licensors and their representatives harmless from and against any and all claims, damages, losses, expenses, costs and liabilities (collectively, "Claims") arising out of or in connection with any use of the EVM that is not in accordance with the terms of the agreement. This obligation shall apply whether Claims arise under law of tort or contract or any other legal theory, and even if the EVM fails to perform as described or expected.

Safety-Critical or Life-Critical Applications. If you intend to evaluate the components for possible use in safety critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, such as devices which are classified as FDA Class III or similar classification, then you must specifically notify TI of such intent and enter into a separate Assurance and Indemnity Agreement.

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