Programmer's Guide

LMK3H2104A02 Configuration Guide

ABSTRACT

This document provides the configuration information for the LMK3H2104A02 device. For the default configuration of the LMK3H2104 device, see the *LMK3H2104 Register Map*.

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Trademarks

1 Configuration Overview

This section provides an overview of the critical device settings of the LMK3H2104A02 configuration.

1.1 LMK3H2104A02 Configuration Information

Table 1-1. LMK3H2104A02 Frequency Configuration

OTP Page	OUT0 (MHz)	OUT1 (MHz)	OUT2 (MHz)	OUT3 (MHz)	REF0 (MHz)	REF1 (MHz)
OTP Page 0	100	100	100	100	Disabled	Disabled
OTP Page 1	100	100	100	100	Disabled	Disabled
OTP Page 2	100	100	100	100	Disabled	Disabled
OTP Page 3	100	100	100	100	Disabled	Disabled

Table 1-2. LMK3H2108A02 I2C Configuration

OTP Page	I2C Configuration
OTP Page 0	I2C Address: 0x68 1 Byte Register Addressing
OTP Page 1	I2C Address: 0x68 1 Byte Register Addressing
OTP Page 2	I2C Address: 0x68 1 Byte Register Addressing
OTP Page 3	I2C Address: 0x68 1 Byte Register Addressing

OTP Page 0

Table 1-3. LMK3H2108A2 GPI Settings, OTP Page 0

GPI Pin	Pin Behavior	Polarity	Internal Pull-Down	Internal Pull-Up
GPI0	GPI	Normal	Enabled	Disabled
GPI1	GPI	Normal	Enabled	Disabled
GPI2	Alternative OE, Alternative OE Mapping 2	Normal	Enabled	Disabled

Table 1-4. LMK3H2108A2 GPIO Settings, OTP Page 0

GPIO Pin	Pin Behavior	Polarity	Internal Pull-Down	Internal Pull-Up
GPIO0	Alternative OE, Alternative OE Mapping 2	Normal	Enabled	Disabled
GPIO1	GPI	Normal	Enabled	Disabled

Table 1-5. LMK3H2108A02 Input Settings, OTP Page 0

Input	Powered Up/Down	Input Format	Input Termination
IN_0	Diabled	N/A (IN0 Unused)	None, DC

Table 1-6. LMKH2108A02 Output Settings, OTP Page 0

Output	Frequency (MHz)	Format	Clock Source	Output State	OE Group	SSC Behavior
OUT0	100	100Ω LPHCSL	PATH1	Enabled	No OE Group	Disabled
OUT1	100	100Ω LPHCSL	PATH1	Enabled	No OE Group	Disabled
OUT2	100	100Ω LPHCSL	PATH1	Enabled	No OE Group	Disabled
OUT3	100	100Ω LPHCSL	PATH1	Enabled	No OE Group	Disabled
REF0	Disabled	N/A	PATH1	Disabled	No OE Group	Disabled
REF1	Disabled	N/A	PATH1	Disabled	No OE Group	Disabled

OTP Page 1

Table 1-7. LMK3H2108A2 GPI Settings, OTP Page 1

GPI Pin	Pin Behavior	Polarity	Internal Pull-Down	Internal Pull-Up
GPI0	GPI	Normal	Enabled	Disabled
GPI1	GPI	Normal	Enabled	Disabled
GPI2	Alternate OE, ALternate OE Mapping 2	Normal	Enabled	Disabled

Table 1-8. LMK3H2108A02 GPIO Settings, OTP Page 1

GPIO Pin	Pin Behavior	Polarity	Internal Pull-Down	Internal Pull-Up
GPIO0	Alternate OE, Alternate OE Mapping 2	Normal	Enabled	Disabled
GPIO1	GPI	Normal	Enabled	Disabled

Table 1-9. LMK3H2108A2 Input Settings, OTP Page 1

Input	Powered Up/Down	Input Format	Input Termination
IN_0	Diabled	N/A (IN0 Unused)	None, DC

Table 1-10. LMK3H2108A2 Output Settings, OTP Page 1

Output	Frequency (MHz)	Format	Clock Source	Output State	OE Group	SSC Behavior
OUT0	100	100Ω LPHCSL	PATH1	Enabled	No OE Group	Enabled, -0.1% Down-spread
OUT1	100	100Ω LPHCSL	PATH1	Enabled	No OE Group	Enabled, -0.1% Down-spread
OUT2	100	100Ω LPHCSL	PATH1	Enabled	No OE Group	Enabled, -0.1% Down-spread
OUT3	100	100Ω LPHCSL	PATH1	Enabled	No OE Group	Enabled, -0.1% Down-spread
REF0	Disabled	N/A	PATH1	Disabled	No OE Group	Disabled
REF1	Disabled	N/A	PATH1	Disabled	No OE Group	Disabled

OTP Page 2

Table 1-11. LMK3H2108A02 GPI Settings, OTP Page 2

GPI Pin	Pin Behavior	Polarity	Internal Pull-Down	Internal Pull-Up
GPI0	GPI	Normal	Enabled	Disabled
GPI1	GPI	Normal	Enabled	Disabled
GPI2	Alternate OE, ALternate OE Mapping 2	Normal	Enabled	Disabled

Table 1-12. LMK3H2108A2 GPIO Settings, OTP Page 2

GPIO Pin	Pin Behavior	Polarity	Internal Pull-Down	Internal Pull-Up
GPIO0	Alternate OE, Alternate OE Mapping 2	Normal	Enabled	Disabled
GPIO1	GPI	Normal	Enabled	Disabled

Table 1-13. LMK3H2108A2 Input Settings, OTP Page 2

Input	Powered Up/Down	Input Format	Input Termination
IN_0	Diabled	N/A (IN0 Unused)	None, DC

Table 1-14. LMK3H2108A2 Output Settings, OTP Page 2

Output	Frequency (MHz)	Format	Clock Source	Output State	OE Group	SSC Behavior
OUT0	100	100Ω LPHCSL	PATH1	Enabled	No OE Group	Enabled, -0.3% Down-spread
OUT1	100	100Ω LPHCSL	PATH1	Enabled	No OE Group	Enabled, -0.3% Down-spread
OUT2	100	100Ω LPHCSL	PATH1	Enabled	No OE Group	Enabled, -0.3% Down-spread
OUT3	100	100Ω LPHCSL	PATH1	Enabled	No OE Group	Enabled, -0.3% Down-spread
REF0	Disabled	N/A	PATH1	Disabled	No OE Group	Disabled
REF1	Disabled	N/A	PATH1	Disabled	No OE Group	Disabled

OTP Page 3

Table 1-15. LMK3H2108A2 GPI Settings, OTP Page 3

GPI Pin	Pin Behavior	Polarity	Internal Pull-Down	Internal Pull-Up
GPI0	GPI	Normal	Enabled	Disabled
GPI1	GPI	Normal	Enabled	Disabled
GPI2	Alternate OE, ALternate OE Mapping 2	Normal	Enabled	Disabled

Table 1-16. LMK3H2108A02 GPIO Settings, OTP Page 3

GPIO Pin	Pin Behavior	Polarity	Internal Pull-Down	Internal Pull-Up
GPIO0	Alternate OE, Alternate OE Mapping 2	Normal	Enabled	Disabled
GPIO1	GPI	Normal	Enabled	Disabled

Table 1-17. LMK3H2108A2 Input Settings, OTP Page 3

Input	Powered Up/Down	Input Format	Input Termination
IN_0	Diabled	N/A (IN0 Unused)	None, DC

Table 1-18. LMK3H2108A02 Output Settings, OTP Page 3

Output	Frequency (MHz)	Format	Clock Source	Output State	OE Group	SSC Behavior
OUT0	100	100Ω LPHCSL	PATH1	Enabled	No OE Group	Enabled, -0.5% Down-spread
OUT1	100	100Ω LPHCSL	PATH1	Enabled	No OE Group	Enabled, -0.5% Down-spread
OUT2	100	100Ω LPHCSL	PATH1	Enabled	No OE Group	Enabled, -0.5% Down-spread
OUT3	100	100Ω LPHCSL	PATH1	Enabled	No OE Group	Enabled, -0.5% Down-spread
REF0	Disabled	N/A	PATH1	Disabled	No OE Group	Disabled
REF1	Disabled	N/A	PATH1	Disabled	No OE Group	Disabled

2 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
January 2026	*	Initial Release

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