Programmer's Guide

UCD9081 Programming Guide

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ABSTRACT

Operation of the UCD9081 is configured by programmable (flash) memory within the device. The memory can be written to and read from using a command protocol over a standard I2C bus interface. This document provides the hardware and software details necessary to program the UCD9081 with the configuration data.

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1 Introduction

The UCD9081 can be customized to each unique user application by creating the programming or configuration parameters file. The most efficient and preferred method for creating the configuration parameters file (either in *.par or *.hex format) is to use the UCD9081 evaluation module (EVM) graphical user interface (GUI) which is available on the TI Web site. This document provides supplemental information to that contained within the UCD9081 data sheet.

2 Hardware

2.1 Package: RHB (S-PQFP-N32), 32-Pin Plastic Quad Flatpack

2.2 Hardware and Pinout

Pin Number	Pin Name	Connection or Description
1	V_{SS}	Ground
2	NC	NC
3	XIN	Vcc
4, 17, 20, 31	NC(1)	Vss
5	$\overline{\text{RST}}$	Device reset
6	MON1	NC
7	MON2	NC
8	MON3	NC
9	MON6	NC
10	EN4	NC
11	EN3	NC
12	EN5	NC
13	EN6	NC
14	EN7	NC
15	MON7	NC
16	MON8	NC
18	MON4	NC
19	MON5	NC
21	SDA	I^2C data
22	SCL	I^2C clock
23	EN1	NC
24	EN2	NC
25	EN8/ADDR1/GPO1	Vss
26	ADDR2/GPO2	Vss
27	ADDR3/GPO3	Vss
28	ADDR4/GPO4	Vss
29	TEST	Vss
30	V_{CC}	3.3 V
32	ROSC	100K to Vcc, or 1.75 V

(1) No Connect

2.3 Detailed Pin Descriptions

2.3.1 $\overline{\text{RST}}$

Device reset input: Apply an active-low level with a minimum pulse width of 2 µs to reset the UCD9081. A delay follows the negation of $\overline{\text{RST}}$ before the UCD9081 can process commands on the I2C bus. See Section 5.2.1 for more detail.

2.3.2 SDA

I2C Serial Data Input/Output: SDA complies with the specification for an I2C Slave device. An external pullup resistor is required on this pin.

2.3.3 SCL

I2C Serial Clock Input/Output: SCL complies with the specification for an I2C Slave device. An external pullup resistor is required on this pin. The UCD9081 can hold or stretch SCL (clock stretching) at any time. During an erase, the UCD9081 stretches SCL for a longer time. See Section 5.2.2 for more detail. SCL has a minimum frequency of 10 kHz and a maximum frequency of 100 kHz.

2.3.4 ADDRx

Device Address Inputs: Shortly after the $\overline{\text{RST}}$ is negated, ADDR1-ADDR4 are sampled by the UCD9081 and define the 4 LSBs for device address on the I2C bus. The upper 3 bits of address are hardcoded at 0x6 giving an addressable range of 0x60-0x6F. These addresses are selected using pullup or pulldown resistors on the ADDRx inputs. Connecting ADDR1-ADDR4 to VSS locates the device at I2C address of 0x60; connecting ADDR1-ADDR4 to VCC locates the device at the I2C address of 0x6F. Once the ADDRx pins are sampled, they then function as EN/GPIO, and they are driven to their default inactive state as defined by the device configuration.

2.3.5 ROSC

Oscillator input: This pin controls the device operating speed. A 100K pullup to Vcc is recommended but 1.75 V can be applied to this pin as well.

3 Software

The UCD9081 EVM GUI provides the optimum development mechanism for creating the configuration parameters file. Two user's guides are available: *Advanced Sequencing and Monitoring Using the UCD9081* and *UCD9081 Power Supply Sequencer and Monitor EVM* containing installation and user instructions for the UCD9081 GUI.

Once the final configuration parameters file has been created, follow the procedures outlined in the UCD9081 data sheet (and emphasized in this document) to configure only the memory areas described in Section 3.1.

Note

NOTE: Use only the UCD9081EVM GUI with UCD9081 devices. Do not use UCD9080EVM GUI with UCD9081 devices because this corrupts the resulting configuration parameters file.

3.1 Data File Format

The configuration data is supplied in standard Intel format. Beginning at address 0x1080, 128 bytes of data are programmed, and beginning at address 0xE000, 512 bytes of data are programmed. Section 3.5 presents a sample configuration data file.

3.2 I2C Transactions

Programming the device with the configuration data requires I2C Write transactions. Reading the configuration data from the device requires I2C Write transactions and I2C Read transactions. Reading the configuration data can be used to verify the correct programming of the data following a write data operation. Section 3.6 presents the format of the I2C Write and Read transactions. Section 3.7 presents the set of pseudo I2C transactions necessary to write and read the sample configuration data presented in Section 3.5.

Note

The I2C write and read data transactions presented in Section 3.6 assume a maximum data transfer block size of 32 bytes. Each block is preceded by the target address. The UCD9081 supports blocks sized from 2 bytes to 512 bytes, in multiples of two bytes (a 16-bit word). When writing data, it is critical that all 128 bytes of the data beginning at address 0x1080 be written, and that all 512 bytes of data beginning at address 0xE000 be written (it is not permitted to do a partial write of a data area).

3.3 Device Version

An I2C Read transaction can be used to read register 0x27; a value of 0x55 indicates that the UCD9081 device version is 5.5.

3.4 Checksum

The UCD9081 EVM GUI automatically calculates and inserts the checksum bytes at address 0xE1FE and 0xE1FF. These are shown in **bold type** in the sample files shown in Section 3.5.

3.5 Sample Configuration Data File

3.5.1 Factory Default

```
:20108000FFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFF70
:2010A000FFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFF50
:2010C000FFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFF30
:2010E000FFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFF10
:20E00000000000000000000000000000000000000000000000000000000000000000000000
:20E020000000000000000000000000000000000000000000000000000000000000000000E0
:20E040000000000000000000FFFF0000000000000000000000000000FF0000000000C00201
:20E060000000000F00020002000058000000000000000020000000000000000000A800105D
:20E08000101112131415161700090A0B00010203040506070000000005000A000E00140079
:20E0A00019001E00230000000000000000000000FF7FFF7FFF7FFF7FFF7FFF7FFF7FFF7F16
:20E0C0000000000000000000000000000000000000000000000000000000000000000000040
:20E0E0000000000000000000000000000000000000000000000000000000000000000000020
:20E100000000000000000000000000000000000000000000000000000000000000000000FF
:20E1200000040004000400040004000400040004A00FA00FA00FA00FA00FA00FA00FA00F47
:20E140001000100010001000100010001000100000C000C000C000C000C000C000C000C03F
:20E16000000000C000C000C0042008200418021808181018201810200020202040208020CD
:20E1800000000004D402F208100105C05500FF0805FF000000000000000000000000000075
:20E1A00000000000000000000000000000000000000000000000000000000000000000005F
:20E1C00000000000000000000000000000000000000000000000000000000000000000003F
:20E1E0000000000000000000000000000000000000000000000000000000000000006E347D
```

3.5.2 EVM Default Configuration

```
:201080002020202020202020202020202020202020202020202020202020202020202020050
:2010A0002020202020202020202020202020202020202020202020202020202020202020030
:2010C0002020202020202020202020202020202020202020202020202020202020202020010
:2010E00020202020202020202020202020202020202020202020202020202020202020200F0
:20E00000000000000000000000000000000000000000000000000000000000000000000000
:20E020000000000000000000000000000000000000000000000000000000000000000000E0
:20E04000000000000000000000000FFF0000000000000000000000000000FF0000000000C002F1
:20E060000000000F00020002FF0058000000000000000020000000000000000000A800105E
:20E080005051525354555657000090A0B000000000000000000000000000000000000000000C6
:20E0A0000000000000000000000000000000000000FF7FFF7FFF7FFF7FFF7FFF7FFF7FFF7F70
:20E0C0000000000000000000000000000000000000000000000000000000000000000000040
:20E0E0000000000000000000000000000000000000000000000000000000000000000000020
:20E100000000000000000000000000000000000000000000000000000000000000000000FF
:20E1200000040004000400040004000400040004A00FA00FA00FA00FA00FA00FA00FA00F47
:20E1400010001000100010001000100010001000000000000000000000000000000000003F
:20E16000000000C000C000C0042008200418021808181018201810200020202040208020CD
:20E1800000000004D402F208100105C05500050005FF000000000000000000000000000077
:20E1A00000000000000000000000000000000000000000000000000000000000000000005F
:20E1C00000000000000000000000000000000000000000000000000000000000000000003F
:20E1E000000000000000000000000000000000000000000000000000000000000000003CE3
```

3.6 I2C Write and Read Transaction Formats

3.6.1 I2C Write Transaction

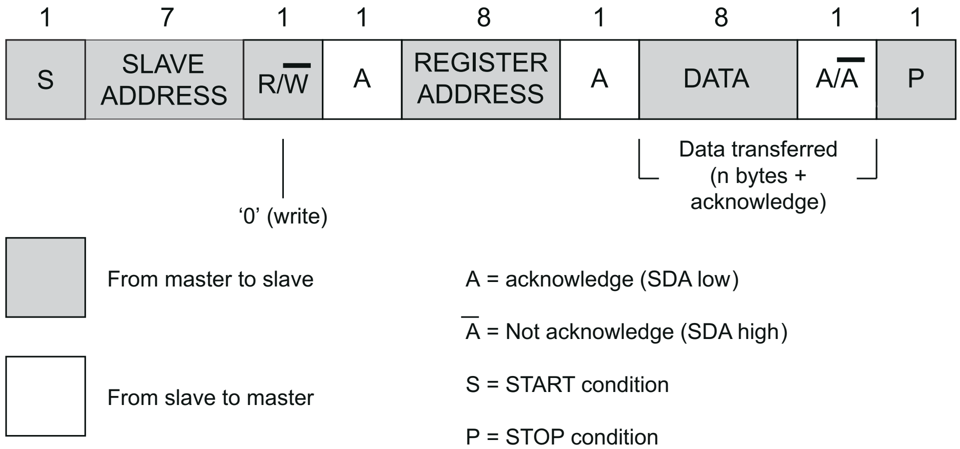

Figure 3-1. Write

3.6.2 I2C Read Transaction

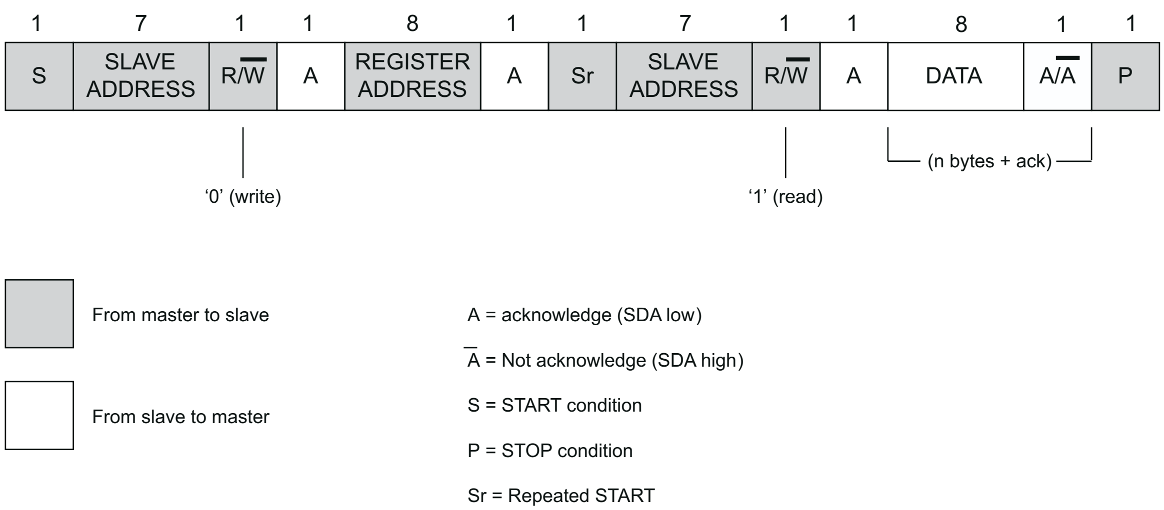

Figure 3-2. Read

3.7 Pseudo I2C Write and Read Transactions

Section 3.7.1 and Section 3.7.2 present pseudo I2C transaction code, which was generated using the UCD9081EVM GUI (Save I2C Transactions feature). Note that in the following pseudo I2C transactions, a Data Length is specified. This value is not directly part of the I2C transaction; rather, its value is used within the Master to count the data transferred. At data transfer completion, the Master can generate "no-acknowledge" (NACK) to the Slave to end the transaction.

3.7.1 UCD9081 I2C Transactions for Writing User Data and PARAMS

I2C Write (Open the FLASH).

Device Address: 0x6F
Register Address: 0x2E
Data Length: 1
Data: 0x02

I2C Write (Base address: 0x1080)

Device Address: 0x6F
Register Address: 0x30
Data Length: 2
Data: 0x80 0x10

I2C Write (Unlock and erase the FLASH)
--------- Device Address: 0x6F
Register Address: 0x32
Data Length: 2
Data: 0xDC 0xBA

I2C Write (Data address: 0x1080)

Device Address: 0x6F
Register Address: 0x30
Data Length: 2
Data: 0x80 0x10

I2C Write (Data)

Device Address: 0x6F
Register Address: 0x32
Data Length: 32
Data: 0x55 0x73 0x65 0x72 0x20 0x64 0x61 0x74 0x61 0x20 0x66 0x6F 0x72 0x20 0x45 0x56 0x4D 0x20 0x63 0x6F 0x6E 0x66 0x69 0x67 0x75 0x72 0x61 0x74 0x69 0x6F 0x6E 0x00

I2C Write (Data address: 0x10A0)

Device Address: 0x6F
Register Address: 0x30
Data Length: 2
Data: 0xA0 0x10

I2C Write (Data)

Device Address: 0x6F
Data Length: 32
Data: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00

I2C Write (Data address: 0x10C0)

Device Address: 0x6F
Register Address: 0x30
Data Length: 2 Data: 0xC0 0x10

I2C Write (Data)

Device Address: 0x6F
Register Address: 0x32
Data Length: 32 Data: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00

I2C Write (Data address: 0x10E0)

Device Address: 0x6F
Register Address: 0x30
Data Length: 2
Data: 0xE0 0x10

```
I2C Write (Data)
---------
Device Address: 0x6F
Register Address: 0x32
Data Length: 32
Data: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00

I2C Write (Base address: 0xE000)
---------
Device Address: 0x6F
Register Address: 0x30
Data Length: 2
Data: 0x00 0xE0

I2C Write (Unlock and erase the FLASH)
---------
Device Address: 0x6F
Register Address: 0x32
Data Length: 2
Data: 0xDC 0xBA

I2C Write (Data address: 0xE000)
---------
Device Address: 0x6F
Register Address: 0x30
Data Length: 2
Data: 0x00 0xE0

I2C Write (Data)
---------
Device Address: 0x6F
Register Address: 0x32
Data Length: 32
Data: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00

I2C Write (Data address: 0xE020)
---------
Device Address: 0x6F
Register Address: 0x30
Data Length: 2
Data: 0x20 0xE0
```

I2C Write (Data)

Device Address: 0x6F
Register Address: 0x32
Data Length: 32
Data: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00

I2C Write (Data address: 0xE040)

Device Address: 0x6F
Register Address: 0x30
Data Length: 2
Data: 0x40 0xE0

I2C Write (Data)

Device Address: 0x6F
Register Address: 0x32
Data Length: 32
Data: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x0F 0xFF 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0xFF 0x00 0x00 0x00 0x00 0x00 0xC0 0x02

I2C Write (Data address: 0xE060)

Device Address: 0x6F
Register Address: 0x30
Data Length: 2
Data: 0x60 0xE0

I2C Write (Data)

Device Address: 0x6F
Register Address: 0x32
Data Length: 32
Data: 0x00 0x00 0x00 0x0F 0x00 0x02 0x00 0x02 0xFF 0x00 0x00 0x58 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x20 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0xA8 0x00 0x10

I2C Write (Data address: 0xE080)

Device Address: 0x6F
Register Address: 0x30
Data Length: 2
Data: 0x80 0xE0

I2C Write (Data)

Device Address: 0x6F
Register Address: 0x32
Data Length: 32
Data: 0x50 0x51 0x52 0x53 0x54 0x55 0x56 0x57 0x00 0x09 0x0A 0x0B 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00

I2C Write (Data address: 0xE0A0)

Device Address: 0x6F
Register Address: 0x30
Data Length: 2
Data: 0xA0 0xE0

I2C Write (Data)

```
---------
Device Address: 0x6F
Register Address: 0x32
Data Length: 32
Data: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0xFF 0x7F 0xFF
0x7F 0xFF 0x7F 0xFF 0x7F 0xFF 0x7F 0xFF 0x7F 0xFF 0x7F 0xFF 0x7F

I2C Write (Data address: 0xE0C0)
---------
Device Address: 0x6F
Register Address: 0x30
Data Length: 2
Data: 0xC0 0xE0

I2C Write (Data)
---------
Device Address: 0x6F
Register Address: 0x32
Data Length: 32
Data: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00

I2C Write (Data address: 0xE0E0)
---------
Device Address: 0x6F
Register Address: 0x30
Data Length: 2
Data: 0xE0 0xE0

I2C Write (Data)
---------
Device Address: 0x6F
Register Address: 0x32
Data Length: 32
Data: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00

I2C Write (Data address: 0xE100)
---------
Device Address: 0x6F
Register Address: 0x30
Data Length: 2
Data: 0x00 0xE1

I2C Write (Data)
---------
Device Address: 0x6F
Register Address: 0x32
Data Length: 32
Data: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00

I2C Write (Data address: 0xE120)
---------
Device Address: 0x6F
Register Address: 0x30
Data Length: 2
Data: 0x20 0xE1
```

I2C Write (Data)

Device Address: 0x6F
Register Address: 0x32
Data Length: 32
Data: 0x00 0x04 0x00 0x04 0x00 0x04 0x00 0x04 0x00 0x04 0x00 0x04 0x00 0x04 0x00 0x04 0xA0 0x0F 0xA0 0x0F 0xA0 0x0F 0xA0 0x0F 0xA0 0x0F 0xA0 0x0F 0xA0 0x0F 0xA0 0x0F

I2C Write (Data address: 0xE140)

Device Address: 0x6F
Register Address: 0x30
Data Length: 2
Data: 0x40 0xE1

I2C Write (Data)

Device Address: 0x6F
Register Address: 0x32
Data Length: 32
Data: 0x10 0x00 0x10 0x00 0x10 0x00 0x10 0x00 0x10 0x00 0x10 0x00 0x10 0x00 0x10 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00

I2C Write (Data address: 0xE160)

Device Address: 0x6F
Register Address: 0x30
Data Length: 2
Data: 0x60 0xE1

I2C Write (Data)

Device Address: 0x6F
Register Address: 0x32
Data Length: 32
Data: 0x00 0x00 0x00 0xC0 0x00 0xC0 0x00 0xC0 0x04 0x20 0x08 0x20 0x04 0x18 0x02 0x18 0x08 0x18 0x10 0x18 0x20 0x18 0x10 0x20 0x00 0x20 0x20 0x20 0x40 0x20 0x80 0x20

I2C Write (Data address: 0xE180)

Device Address: 0x6F
Register Address: 0x30
Data Length: 2
Data: 0x80 0xE1

I2C Write (Data)

Device Address: 0x6F
Register Address: 0x32
Data Length: 32
Data: 0x00 0x00 0x00 0x04 0xD4 0x02 0xF2 0x08 0x10 0x01 0x05 0xC0 0x55 0x00 0x05 0x00 0x05 0xFF 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00

I2C Write (Data address: 0xE1A0)

Device Address: 0x6F
Register Address: 0x30
Data Length: 2
Data: 0xA0 0xE1

```
I2C Write (Data)
---------
Device Address: 0x6F
Register Address: 0x32
Data Length: 32
Data: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00

I2C Write (Data address: 0xE1C0)
---------
Device Address: 0x6F
Register Address: 0x30
Data Length: 2
Data: 0xC0 0xE1

I2C Write (Data)
---------
Device Address: 0x6F
Register Address: 0x32
Data Length: 32
Data: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00

I2C Write (Data address: 0xE1E0)
---------
Device Address: 0x6F
Register Address: 0x30
Data Length: 2
Data: 0xE0 0xE1

I2C Write (Data)
---------
Device Address: 0x6F
Register Address: 0x32
Data Length: 32
Data: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x3C

I2C Write (Lock and close the FLASH)
---------
Device Address: 0x6F
Register Address: 0x2E
Data Length: 1
Data: 0x00
```

3.7.2 UCD9081 I2C Transactions for Reading User Data and PARAMS

I2C Write (Data address: 0x1080)

Device Address: 0x6F
Register Address: 0x30
Data Length: 2
Data: 0x80 0x10

I2C Read (Data)

Device Address: 0x6F
Register Address: 0x32
Data Length: 32

I2C Write (Data address: 0x10A0)

Device Address: 0x6F
Register Address: 0x30
Data Length: 2
Data: 0xA0 0x10

I2C Read (Data)

Device Address: 0x6F
Register Address: 0x32
Data Length: 32

I2C Write (Data address: 0x10C0)

Device Address: 0x6F
Register Address: 0x30
Data Length: 2
Data: 0xC0 0x10

I2C Read (Data)

Device Address: 0x6F
Register Address: 0x32
Data Length: 32

I2C Write (Data address: 0x10E0)

Device Address: 0x6F
Register Address: 0x30
Data Length: 2
Data: 0xE0 0x10

I2C Read (Data)

Device Address: 0x6F
Register Address: 0x32
Data Length: 32

I2C Write (Data address: 0xE000)

Device Address: 0x6F
Register Address: 0x30
Data Length: 2
Data: 0x00 0xE0

```
I2C Read (Data)
--------
Device Address: 0x6F
Register Address: 0x32
Data Length: 32

I2C Write (Data address: 0xE020)
---------
Device Address: 0x6F
Register Address: 0x30
Data Length: 2
Data: 0x20 0xE0

I2C Read (Data)
--------
Device Address: 0x6F
Register Address: 0x32
Data Length: 32

I2C Write (Data address: 0xE040)
---------
Device Address: 0x6F
Register Address: 0x30
Data Length: 2
Data: 0x40 0xE0

I2C Read (Data)
--------
Device Address: 0x6F
Register Address: 0x32
Data Length: 32

I2C Write (Data address: 0xE060)
---------
Device Address: 0x6F
Register Address: 0x30
Data Length: 2
Data: 0x60 0xE0

I2C Read (Data)
--------
Device Address: 0x6F
Register Address: 0x32
Data Length: 32

I2C Write (Data address: 0xE080)
---------
Device Address: 0x6F
Register Address: 0x30
Data Length: 2
Data: 0x80 0xE0

I2C Read (Data)
--------
Device Address: 0x6F
Register Address: 0x32
Data Length: 32

I2C Write (Data address: 0xE0A0)
---------
Device Address: 0x6F
```

```
Register Address: 0x30
Data Length: 2
Data: 0xA0 0xE0

I2C Read (Data)
--------
Device Address: 0x6F
Register Address: 0x32
Data Length: 32

I2C Write (Data address: 0xE0C0)
---------
Device Address: 0x6F
Register Address: 0x30
Data Length: 2
Data: 0xC0 0xE0

I2C Read (Data)
--------
Device Address: 0x6F
Register Address: 0x32
Data Length: 32

I2C Write (Data address: 0xE0E0)
---------
Device Address: 0x6F
Register Address: 0x30
Data Length: 2
Data: 0xE0 0xE0

I2C Read (Data)
--------
Device Address: 0x6F
Register Address: 0x32
Data Length: 32

I2C Write (Data address: 0xE100)
---------
Device Address: 0x6F
Register Address: 0x30
Data Length: 2
Data: 0x00 0xE1

I2C Read (Data)
--------
Device Address: 0x6F
Register Address: 0x32
Data Length: 32

I2C Write (Data address: 0xE120)
---------
Device Address: 0x6F
Register Address: 0x30
Data Length: 2
Data: 0x20 0xE1

I2C Read (Data)
--------
Device Address: 0x6F
Register Address: 0x32
Data Length: 32
```

I2C Write (Data address: 0xE140)

Device Address: 0x6F
Register Address: 0x30
Data Length: 2
Data: 0x40 0xE1

I2C Read (Data)

Device Address: 0x6F
Register Address: 0x32
Data Length: 32

I2C Write (Data address: 0xE160)
--------- Device Address: 0x6F
Register Address: 0x30
Data Length: 2
Data: 0x60 0xE1

I2C Read (Data)

Device Address: 0x6F
Register Address: 0x32
Data Length: 32

I2C Write (Data address: 0xE180)

Device Address: 0x6F
Register Address: 0x30
Data Length: 2
Data: 0x80 0xE1

I2C Read (Data)

Device Address: 0x6F
Register Address: 0x32
Data Length: 32

I2C Write (Data address: 0xE1A0)

Device Address: 0x6F
Register Address: 0x30
Data Length: 2
Data: 0xA0 0xE1

I2C Read (Data)

Device Address: 0x6F
Register Address: 0x32
Data Length: 32

I2C Write (Data address: 0xE1C0)

Device Address: 0x6F
Register Address: 0x30
Data Length: 2
Data: 0xC0 0xE1

I2C Read (Data)

Device Address: 0x6F

Register Address: 0x32
Data Length: 32

I2C Write (Data address: 0xE1E0)

Device Address: 0x6F
Register Address: 0x30
Data Length: 2
Data: 0xE0 0xE1

I2C Read (Data)

Device Address: 0x6F
Register Address: 0x32
Data Length: 32

4 User Configuration

4.1 Configuration Parameter Memory Map

Table 4-1 shows the 512-byte configuration parameters memory map. User-configurable bytes in bold are described in the Section 4.2; adjacent groups of user-configurable bytes are distinguished in the table by alternating use of italics. Other bytes must remain exactly as shown in Table 4-1.

Table 4-1. Configuration Parameters Memory Map

Address	+0	+1	+2	+3	+4	+5	+6	+7	+8	+9	+A	+B	+C	+D	+E	+F
E000	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
E010	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
E020	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
E030	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
E040	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	**0xFF**	**0xFF**	**0x00**	**0x00**	0x00	0x00	0x00	0x00
E050	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0xFF	0x00	0x00	0x00	0x00	0x00	0xC0	0x02
E060	0x00	0x00	0x00	0x0F	0x00	0x02	0x00	0x02	**0x00**	**0x00**	**0x00**	0x58	0x00	0x00	0x00	0x00
E070	0x00	0x00	0x00	0x20	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0xA8	0x00	0x10
E080	***0x10***	***0x11***	***0x12***	***0x13***	***0x14***	***0x15***	***0x16***	***0x17***	***0x00***	***0x09***	***0x0A***	***0x0B***	**0x00**	**0x01**	**0x02**	**0x03**
E090	**0x04**	**0x05**	**0x06**	**0x07**	**0x00**	**0x00**	**0x00**	**0x00**	***0x05***	***0x00***	***0x0A***	***0x00***	***0x0E***	***0x00***	***0x14***	***0x00***
E0A0	***0x19***	***0x00***	***0x1E***	***0x00***	***0x23***	***0x00***	***0x00***	***0x00***	***0x00***	***0x00***	***0x00***	***0x00***	***0x00***	***0x00***	***0x00***	***0x00***
E0B0	0xFF	0x7F	0xFF	0x7F	0xFF	0x7F	0xFF	0x7F	0xFF	0x7F	0xFF	0x7F	0xFF	0x7F	0xFF	0x7F
E0C0	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
E0D0	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
E0E0	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
E0F0	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
E100	**0x00**	**0x00**	**0x00**	**0x00**	**0x00**	**0x00**	**0x00**	**0x00**	**0x00**	**0x00**	**0x00**	**0x00**	**0x00**	**0x00**	**0x00**	**0x00**
E110	***0x00***	***0x00***	***0x00***	***0x00***	***0x00***	***0x00***	***0x00***	***0x00***	***0x00***	***0x00***	***0x00***	***0x00***	***0x00***	***0x00***	***0x00***	***0x00***
E120	**0x00**	**0x04**	**0x00**	**0x04**	**0x00**	**0x04**	**0x00**	**0x04**	**0x00**	**0x04**	**0x00**	**0x04**	**0x00**	**0x04**	**0x00**	**0x04**
E130	***0xA0***	***0x0F***	***0xA0***	***0x0F***	***0xA0***	***0x0F***	***0xA0***	***0x0F***	***0xA0***	***0x0F***	***0xA0***	***0x0F***	***0xA0***	***0x0F***	***0xA0***	***0x0F***
E140	**0x10**	**0x00**	**0x10**	**0x00**	**0x10**	**0x00**	**0x10**	**0x00**	**0x10**	**0x00**	**0x10**	**0x00**	**0x10**	**0x00**	**0x10**	**0x00**
E150	***0x00***	***0xC0***	***0x00***	***0xC0***	***0x00***	***0xC0***	***0x00***	***0xC0***	***0x00***	***0xC0***	***0x00***	***0xC0***	***0x00***	***0xC0***	***0x00***	***0xC0***
E160	***0x00***	***0x00***	***0x00***	***0xC0***	***0x00***	***0xC0***	***0x00***	***0xC0***	**0x04**	**0x20**	**0x08**	**0x20**	**0x04**	**0x18**	**0x02**	**0x18**
E170	**0x08**	**0x18**	**0x10**	**0x18**	**0x20**	**0x18**	**0x10**	**0x20**	**0x00**	**0x20**	**0x20**	**0x20**	**0x40**	**0x20**	**0x80**	**0x20**
E180	***0x00***	***0x00***	0x00	0x04	0xD4	0x02	**0xF2**	**0x08**	0x10	0x01	0x05	0xC0	0x55	0x00	***0xFF***	***0x08***
E190	0x05	**0xFF**	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
E1A0	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
E1B0	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
E1C0	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
E1D0	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
E1E0	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
E1F0	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	***0x6E***	***0x34***

4.2 Configuration Parameter Detail

4.2.1 GpDir

The GpDir field in the configuration parameters specifies the direction (input or output) of RAILn or GPOn. This should correspond with the desired enable settings. If a RAIL or GPO is enabled, it should also be set as an output. The register contents are as follows:

Address	Size	Default Value	Description
0xE048	2	0xFFFF	Input / Output parameters for GPOn and RAILn

The format of the register is as follows:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	**0**	**0**	**0**	**GPO4**	**GPO3**	**GPO2**	**GPO1**	**RAIL8**	**RAIL7**	**RAIL6**	**RAIL5**	**RAIL4**	**RAIL3**	**RAIL2**	**RAIL1**

RAILn or GPOn	Meaning
0	Set the RAILn or GPOn to output (enable)
1	Set the RAILn or GPOn to input (disable)

4.2.2 NegateEnablePolarity

The NegateEnablePolarity field in the configuration parameters allows for the selection of enable signal for RAILn and GPOn to be active high or active low. These values should align with bit 16 of the **EnablePolarity** registers (R[0xE168] to R[0xE17E]) (see Section 4.2.13). If the RAIL or GPO is set as enable active-low (value = 0b), the corresponding NegateEnablePolarity bit value should also be set 1b. The register contents are as follows:

Address	Size	Default Value	Description
0xE04A	2	0x0000	NegateEnable signal parameters for Railn and GPOn

The format of the register is as follows:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	**0**	**0**	**0**	**GPO4**	**GPO3**	**GPO2**	**GPO1**	**RAIL8**	**RAIL7**	**RAIL6**	**RAIL5**	**RAIL4**	**RAIL3**	**RAIL2**	**RAIL1**

RAILn or GPOn	Meaning
0	Enable signal set as active-high (1b) for RAILn or GPOn in R[0xE168]:R[0xE17E], bit[16]
1	Enable signal set as active-low (0b) for RAILn or GPOn in R[0xE168]:R[0xE17E], bit[16]

4.2.3 SeqEventPending

The SeqEventPending field in the configuration parameters determines if the RAILn or GPOn will be enabled or disabled for sequencing. These values should align with **SequenceEventParameter** (see Section 4.2.4), if RAILn/GPOn is not disabled, it should also not be disabled in these parameters.

Address	Size	Default Value	Description
0xE068	2	0x0000	Sequencing parameters for GPOn and RAILn

The format of the register is as follows:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	**0**	**0**	**0**	**GPO4**	**GPO3**	**GPO2**	**GPO1**	**RAIL8**	**RAIL7**	**RAIL6**	**RAIL5**	**RAIL4**	**RAIL3**	**RAIL2**	**RAIL1**

RAILn or GPOn	Meaning
0	Disable sequencing on RAILn or GPOn
1	Enable sequencing on RAILn or GPOn

4.2.4 SequenceEventParameters

The SequenceEventParameters field in the configuration parameters specifies the rail identification, monitoring status, and sequencing options for each rail. The address map for these registers is as follows:

Address	Size	Default Value	Description
0xE080	1	0x50	Rail 1 identification, monitoring status and sequencing options
0xE081	1	0x51	Rail 2 identification, monitoring status, and sequencing options
0xE082	1	0x52	Rail 3 identification, monitoring status, and sequencing options
0xE083	1	0x53	Rail 4 identification, monitoring status, and sequencing options
0xE084	1	0x54	Rail 5 identification, monitoring status, and sequencing options
0xE085	1	0x55	Rail 6 identification, monitoring status, and sequencing options
0xE086	1	0x56	Rail 7 identification, monitoring status, and sequencing options
0xE087	1	0x57	Rail 8 identification, monitoring status, and sequencing options
0xE088	1	0x00	GPO1 identification, sequencing options
0xE089	1	0x49	GPO2 identification, sequencing options
0xE08A	1	0x4A	GPO3 identification, sequencing options
0xE08B	1	0x4B	GPO4 identification, sequencing options

The format of each register is as follows:

7	6	5	4	3	2	1	0
ENABLE		0	MON	RAIL/GPO			

RAIL

Rail #(n) – 1, RAIL = 0 through 7

GPO

GPO #(n) + 7, GPO = 8, 9, 0xA, 0xB

MON	Meaning
0	Do not monitor rail status (for event sequencing of GPOs)
1	Monitor rail status

ENABLE	Meaning
00	Sequence is disabled
01	Sequence is triggered after delay after sequence event
10	Sequence is triggered after parent rail achieves voltage level
11	Sequence is triggered after delay after parent rail achieves voltage regulation

4.2.5 SequenceEventLink

The SequenceEventLink field allows a parent rail (monitored input) to be specified for each ENx and GPOx output. The RESEQ bit (sequence after shutdown) allows an enable or GPO to be marked to sequence the system (as defined by the current sequencer configuration) after it has been shut down. The address map for these registers is as follows:

Address	Size	Default Value	Description
0xE08C	1	0x01	Rail 1 parent rail identifier and resequence indicator
0xE08D	1	0x00	Rail 2 parent rail identifier and resequence indicator
0xE08E	1	0x01	Rail 3 parent rail identifier and resequence indicator
0xE08F	1	0x04	Rail 4 parent rail identifier and resequence indicator
0xE090	1	0x01	Rail 5 parent rail identifier and resequence indicator
0xE091	1	0x04	Rail 6 parent rail identifier and resequence indicator
0xE092	1	0x05	Rail 7 parent rail identifier and resequence indicator
0xE093	1	0x06	Rail 8 parent rail identifier and resequence indicator
0xE094	1	0x00	GPO1 parent rail identifier and resequence indicator
0xE095	1	0x00	GPO2 parent rail identifier and resequence indicator
0xE096	1	0x00	GPO3 parent rail identifier and resequence indicator
0xE097	1	0x00	GPO4 parent rail identifier and resequence indicator

The format of each register is as follows:

7	6	5	4	3	2	1	0
0	**RESEQ**	**0**	**0**	**PARENTRAIL**			

RESEQ	Meaning
0	Do not sequence after shutdown.
1	Sequence after shutdown.

PARENTRAIL	Meaning
0x0000	Sequence is dependent on RAIL1 achieving the specified event.
0x0001	Sequence is dependent on RAIL2 achieving the specified event.
0x0010	Sequence is dependent on RAIL3 achieving the specified event.
0x0011	Sequence is dependent on RAIL4 achieving the specified event.
0x0100	Sequence is dependent on RAIL5 achieving the specified event.
0x0101	Sequence is dependent on RAIL6 achieving the specified event.
0x0110	Sequence is dependent on RAIL7 achieving the specified event.
0x0111	Sequence is dependent on RAIL8 achieving the specified event.

4.2.6 SequenceEventData

The SequenceEventData field in the configuration parameters specifies the rail and GPO sequencing and shutdown parameters. The address map for these registers is as follows:

Address	Size	Default Value	Description
0xE098	2	0xE005	Rail 1 sequencing and shutdown parameters
0xE09A	2	0xA005	Rail 2 sequencing and shutdown parameters
0xE09C	2	0xE032	Rail 3 sequencing and shutdown parameters
0xE09E	2	0xE033	Rail 4 sequencing and shutdown parameters
0xE0A0	2	0xE033	Rail 5 sequencing and shutdown parameters
0xE0A2	2	0xE035	Rail 6 sequencing and shutdown parameters
0xE0A4	2	0xE035	Rail 7 sequencing and shutdown parameters
0xE0A6	2	0x0000	Rail 8 sequencing and shutdown parameters
0xE0A8	2	0x0000	GPO1 sequencing and shutdown parameters
0xE0AA	2	0x0000	GPO2 sequencing and shutdown parameters
0xE0AC	2	0x0000	GPO3 sequencing and shutdown parameters
0xE0AE	2	0x0000	GPO4 sequencing and shutdown parameters

The format for each register is as follows. The value in the ENABLE field of the SequenceEventParameters register determines the measure represented by the value in the RAILDATA field of the SequenceEventData register.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEQPARAM			0	RAILDATA											

SEQPARAM	Meaning
000	Log only
001	Sequence
010	Reserved
011	Reserved
100	Reserved
101	Retry 1 times
110	Retry 0 times
111	Reserved

ENABLE (SequenceEventParameters)	RAILDATA Meaning
01	Delay (in units of ms)
10	Voltage (in units of Vref/1024 volts)
11	Delay (in units of ms)

4.2.7 DependencyMasks

The DependencyMasks field in the configuration parameters defines the rail dependency masks used for rail and GPO shutdown. This mask represents the set of other rails and GPOs that must be shut down when this rail shuts down. Note that because only rails are monitored, the table only has entries for the shutdown of rails. In the dependency mask itself, there are bits that allow for GPO shutdown.

The address map for these registers is as follows:

Address	Size	Default Value	Description
0xE100	2	0x007F	Dependency mask for rail 1
0xE102	2	0x0001	Dependency mask for rail 2
0xE104	2	0x0002	Dependency mask for rail 3
0xE106	2	0x0004	Dependency mask for rail 4
0xE108	2	0x0008	Dependency mask for rail 5
0xE10A	2	0x0010	Dependency mask for rail 6
0xE10C	2	0x0020	Dependency mask for rail 7
0xE10E	2	0x0040	Dependency mask for rail 8

The format for each register is as follows:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	**0**	**0**	**0**	**GPO4**	**GPO3**	**GPO2**	**GPO1**	**RAIL8**	**RAIL7**	**RAIL6**	**RAIL5**	**RAIL4**	**RAIL3**	**RAIL2**	**RAIL1**

RAILn or GPOn	Meaning
0	Shutdown of this rail does not shut down RAILn or GPOn.
1	Shutdown of this rail shuts down RAILn or GPOn.

4.2.8 UnderVoltageThresholds

The UnderVoltageThresholds field in the configuration parameters specifies each rail undervoltage threshold that is used when monitoring this rail. The address map for these registers is as follows:

Address	Size	Default Value	Description
0xE110	2	0x0000	Undervoltage threshold for rail 8
0xE112	2	0x0000	Undervoltage threshold for rail 7
0xE114	2	0x0000	Undervoltage threshold for rail 6
0xE116	2	0x0000	Undervoltage threshold for rail 5
0xE118	2	0x0000	Undervoltage threshold for rail 4
0xE11A	2	0x0000	Undervoltage threshold for rail 3
0xE11C	2	0x0000	Undervoltage threshold for rail 2
0xE11E	2	0x0000	Undervoltage threshold for rail 1

The format for each register is as follows:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	**0**	**0**	**0**	**0**	**Vraw**										

The voltage conversion depends on the configured voltage reference, and the pullup/pulldown resistors used on the board for each rail. The voltage reference is selected as either 2.5 V (internal) or V_{CC} (external). The formula to convert the desired rail UnderVoltageThreshold to Vraw follows:

Without external rail voltage divider:

$$\text{Vraw} = \frac{1024 \times V_{RAILUV}}{V_{REF}} \tag{1}$$

With external rail voltage divider:

$$\text{Vraw} = \frac{1024 \times V_{RAILUV}}{V_{REF}} \times \frac{R_{PULLDOWN}}{R_{PULLDOWN} + R_{PULLUP}} \tag{2}$$

4.2.9 OverVoltageThresholds

The OverVoltageThresholds field in the configuration parameters specifies each rail overvoltage threshold that is used when monitoring this rail. The address map for these registers is as follows:

Address	Size	Default Value	Description
0xE120	2	0x0400	Overvoltage threshold for rail 8
0xE122	2	0x0400	Overvoltage threshold for rail 7
0xE124	2	0x0400	Overvoltage threshold for rail 6
0xE126	2	0x0400	Overvoltage threshold for rail 5
0xE128	2	0x0400	Overvoltage threshold for rail 4
0xE12A	2	0x0400	Overvoltage threshold for rail 3
0xE12C	2	0x0400	Overvoltage threshold for rail 2
0xE12E	2	0x0400	Overvoltage threshold for rail 1

The format for each register is as follows:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	**0**	**0**	**0**	**0**	**Vraw**										

The voltage conversion depends on the configured voltage reference, and the pullup/pulldown resistors used on the board for each rail. The voltage reference is selected as either 2.5 V (internal) or V_{CC} (external). The formula to convert the desired rail OverVoltageThreshold to Vraw follows:

Without external rail voltage divider:

$$\text{Vraw} = \frac{1024 \times V_{RAILOV}}{V_{REF}} \tag{3}$$

With external voltage divider:

$$\text{Vraw} = \frac{1024 \times V_{RAILOV}}{V_{REF}} \times \frac{R_{PULLDOWN}}{R_{PULLDOWN} + R_{PULLUP}} \tag{4}$$

4.2.10 RampTime

The RampTime field in the configuration parameters specifies the maximum amount of time for each rail to achieve regulation. The address map for these registers is as follows:

Address	Size	Default Value	Description
0xE130	2	0x0FA0	Maximum voltage ramp time for rail 1
0xE132	2	0x0FA0	Maximum voltage ramp time for rail 2
0xE134	2	0x0FA0	Maximum voltage ramp time for rail 3
0xE136	2	0x0FA0	Maximum voltage ramp time for rail 4
0xE138	2	0x0FA0	Maximum voltage ramp time for rail 5
0xE13A	2	0x0FA0	Maximum voltage ramp time for rail 6
0xE13C	2	0x0FA0	Maximum voltage ramp time for rail 7
0xE13E	2	0x0FA0	Maximum voltage ramp time for rail 8

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	RAMPTIME											

RAMPTIME = RAILn RailTime (in units of ms).

4.2.11 OutOfRegulationWidth

The OutOfRegulationWidth field in the configuration parameters specifies the maximum amount of time that the rail is allowed to be out of regulation before an error is declared (glitch duration). The address map for these registers is as follows:

Address	Size	Default Value	Description
0xE140	2	0x0010	The out-of-regulation duration permissible without flagging error for rail 1
0xE142	2	0x0010	The out-of-regulation duration permissible without flagging error for rail 2
0xE144	2	0x0010	The out-of-regulation duration permissible without flagging error for rail 3
0xE146	2	0x0010	The out-of-regulation duration permissible without flagging error for rail 4
0xE148	2	0x0010	The out-of-regulation duration permissible without flagging error for rail 5
0xE14A	2	0x0010	The out-of-regulation duration permissible without flagging error for rail 6
0xE14C	2	0x0010	The out-of-regulation duration permissible without flagging error for rail 7
0xE14E	2	0x0010	The out-of-regulation duration permissible without flagging error for rail 8

The contents of this register are as follows:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	OORW											

OORW = RAILn out-of-regulation glitch width (in units of 1/10 ms).

4.2.12 UnsequenceTime

The UnsequenceTime field in the configuration parameters specifies the amount of time that each rail must delay before unsequencing. The address map for these registers is as follows:

Address	Size	Default Value	Description
0xE150	2	0xC0FF	Unsequence delay for rail 1
0xE152	2	0xC1FF	Unsequence delay for rail 2
0xE154	2	0xC2FF	Unsequence delay for rail 3
0xE156	2	0xC3FF	Unsequence delay for rail 4
0xE158	2	0xC4FF	Unsequence delay for rail 5
0xE15A	2	0xC5FF	Unsequence delay for rail 6
0xE15C	2	0xC6FF	Unsequence delay for rail 7
0xE15E	2	0xC7FF	Unsequence delay for rail 8
0xE160	2	0x0000	Unsequence delay for GPO1
0xE162	2	0xC000	Unsequence delay for GPO2
0xE164	2	0xC000	Unsequence delay for GPO3
0xE166	2	0xC000	Unsequence delay for GPO4

The contents of this register are as follows:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COPYSEQPARAM			0	USTIME											

COPYSEQPARAM = Copy SEQPARAM bit value (bits 15:13) in SequenceEvent Data register

USTIME = RAILn UnsequenceTime (in units of ms).

4.2.13 EnablePolarity

The EnablePolarity field in the configuration parameters specifies whether each power-supply enable or GPO is to be configured active-high or active-low. The address map for these registers is as follows:

Address	Size	Default Value	Description
0xE168	2	0x2004	Polarity for rail 1 enable
0xE16A	2	0x2008	Polarity for rail 2 enable
0xE16C	2	0x1804	Polarity for rail 3 enable
0xE16E	2	0x1802	Polarity for rail 4 enable
0xE170	2	0x1808	Polarity for rail 5 enable
0xE172	2	0x1810	Polarity for rail 6 enable
0xE174	2	0x1820	Polarity for rail 7 enable
0xE176	2	0x2010	Polarity for rail 8 enable
0xE178	2	0x2000	Polarity for GPO1
0xE17A	2	0x2020	Polarity for GPO2
0xE17C	2	0x2040	Polarity for GPO3
0xE17E	2	0x2080	Polarity for GPO4

The contents of this register are as follows:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
POL	DEFAULT VALUES as specified previously														

POL	Meaning
0	Rail enable or GPO is active-low.
1	Rail enable or GPO is active-high.

4.2.14 SaveRailLog

The SaveRailLog field in the configuration parameters specifies whether each rail is marked to write the error log to flash upon rail failure. If the rail is marked this way, then a shutdown of this rail is logged info non-volatile memory. In this case, the NVERRLOG bit (STATUS register) is set to 1 upon device initialization and must be cleared before normal sequencer operation is restored. See the section titled *Resetting the Flash Error Logs* for detailed instructions.

The contents of this register are as follows:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	RAIL8	RAIL7	RAIL6	RAIL5	RAIL4	RAIL3	RAIL2	RAIL1

RAILn	Meaning
0	Shutdown of this rail will not log this event.
1	Shutdown of this rail will log this event.

The default value for this register is 0x0000.

4.2.15 ReferenceSelect

The ReferenceSelect field in the configuration parameters specifies which voltage reference is used on the UCD9080. The selected reference can be internal (2.5-V), or external via V_{CC} (3.3 V). The register address is 0xE186 and contents are as follows:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SELREF			**0**	**0x8F2**											

SELREF	Meaning
000	External reference selected (VCC)
001	Internal reference selected (2.5 V)

The default value for this register is 0x08F2, which selects the external reference.

4.2.16 LastUnusedSeq

The LastUnusedSeq field in the configuration parameters specifies the amount of time for the last rail to be shut down without creating an error. The register address is 0xE18E and contents are as follows:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LUTIME															

LUTIME = Maximum value USTIME + 255 (in units of ms)

The default value for this register is 0x08FF.

4.2.17 IgnoreGlitchAlarms

The IgnoreGlitchAlarms field in the configuration parameters can be used to suppress glitches from being logged. Refer to the Voltage Monitoring section in SLVS813 for a full description. The register address is E06A and contents are as follows:

7	6	5	4	3	2	1	0
R8	R7	R6	R5	R4	R3	R2	R1

Rx = Rail #
Default = 0x00
Write 1 to bit location to suppress glitch alarms

4.2.18 IgnoreFlashErrorLog

The IgnoreFlashErrorLog bit in the configuration parameters can be used to allow sequencing when entries are present in the flash error log (NVERRLOG bit is set to 1). Refer to the Resetting the Flash Error Log section in SLVS813 for a full description. The register address is E191 and contents are as follows:

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	IFEL

IFEL = Ignore flash error log
Default = 0x00
Write 1 to bit 0 location to ignore flash error log

4.2.19 Checksum

The Checksum word is the 1's complement of the sum of the words from 0xE000 to 0xE1FD in the configuration parameters. The checksum is stored in the last word of the device parameter section (0xE1FF is high byte and 0xE1FE is the low byte). The area check-summed (and the checksum) is stored low-byte/high-byte ("Little Endian") format.

5 Additional Considerations

5.1 Embedded Application

Because the UCD9081 exhibits much control over a typical power system, the embedded application is not suspended or delayed while waiting for I2C commands. The embedded application provides mechanisms to always prioritize local sequencing and monitoring when I2C communication is interrupted. These mechanisms are primarily timers. Generally, if the timers expire, then the I2C master sees a NACK and must re-issue the command.

5.2 Timing

The internal timing reference for the UCD9081 can vary as much as ±20% over process, temperature, and supply voltage. Delay time values used in the following sections are listed as nominal, and the user must apply an appropriate timing guard band.

5.2.1 UCD9081 Startup

I2C communication with the UCD9081 cannot be established immediately after power is applied. On power up, the UCD9081 performs several operations on the contents of the user parameter section. A RESET delay is incurred during this operation, and the digital I/O pins are in a high-impedance state. At the end of this operation, the sequencer application starts and I2C communication may commence.

The startup delay can vary based on the cases that follow;

- Normal case: The UCD9081 performs a checksum test on the contents of the user parameter section. If the test passes, then the UCD9081 compares the contents of the user parameters section to the contents of the application (or last-known-good configuration) parameters section to see if the parameters have changed. If the two areas match, then the sequencer application starts. This nominally takes 35 ms as shown in Figure 5-1

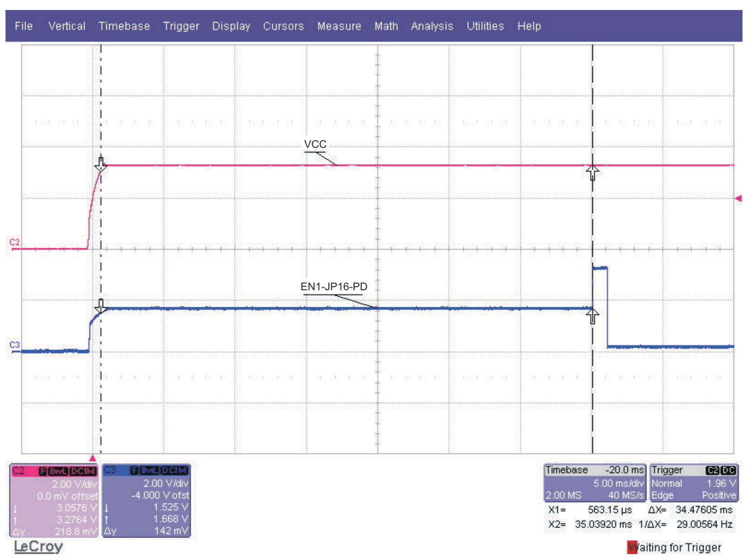

Figure 5-1. Power-Up Delay, no Parameter Change

- Configuration change-pass checksum case: If the user parameter area has been updated but the device has not been RESET (see UCD9081 data sheet RESET description) then the user and application parameter areas do not match. After the next RESET, the checksum test occurs. If the test passes, then the UCD9081 copies the user parameters to the application parameters area. This nominally takes 102 ms as shown in Figure 5-2. Subsequent power ups (with unchanged user parameters) fall into the normal category.
- Configuration change-fail checksum case: If the checksum test fails, then the UCD9081 copies the application parameters back to the user parameters area. This nominally takes 102 ms as shown in Figure 5-2.

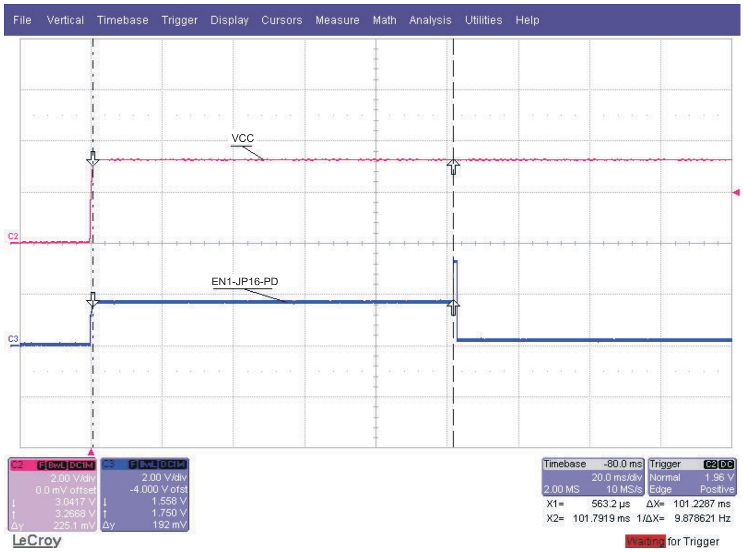

Figure 5-2. Power-Up Delay, With Parameter Change

5.2.2 Clock Stretching After Flash Erase

During three command operations, the UCD9081 holds SCL low while an erase is being performed. The UCD9081 performs an erase just after the WDATA register is written with 0xBADC. See the following UCD9081 data sheet sections for detailed explanation of when the WDATA register is written with 0xBADC.

- RESETTING THE FLASH ERROR LOG
- CONFIGURING THE UCD9081
- USER DATA

After an erase, the I2C master may either wait for SCL to be released or wait approximately 12 ms before issuing another transaction.

5.2.3 Bit Timeout

The UCD9081 enforces a maximum bit timeout period of $1/f_{SCL(MIN)}$ (100 µs) for the bit cases described in the following list. This bit period must be met or else the UCD9081 may exit a transaction, causing a NACK to occur. For the bit cases not described in the following list, the byte timeout applies as described in Section 5.2.4.

- START bit (Figure 5-3): SCL must fall within 100 µs of SDA falling.

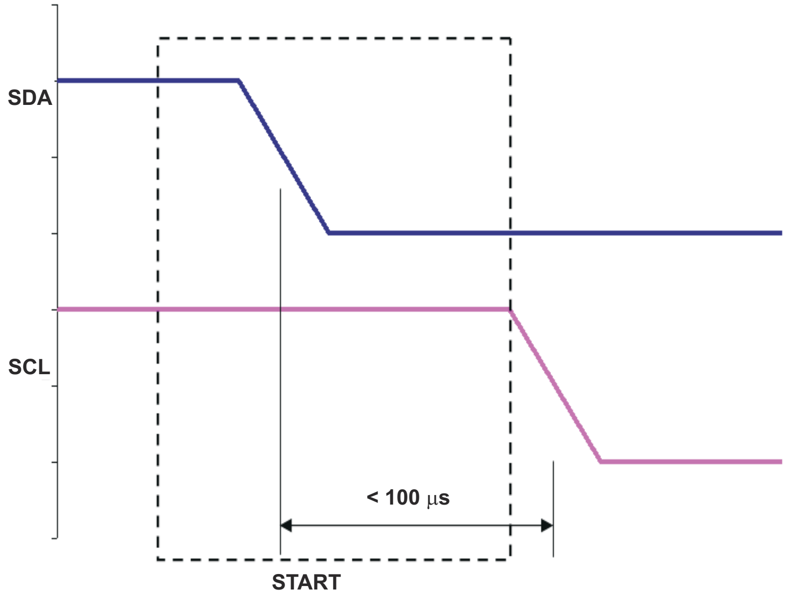

Figure 5-3. START Bit Requirement

- Eighth data bit of write command (Figure 5-4): SCL must fall within 100 µs of SCL rising.

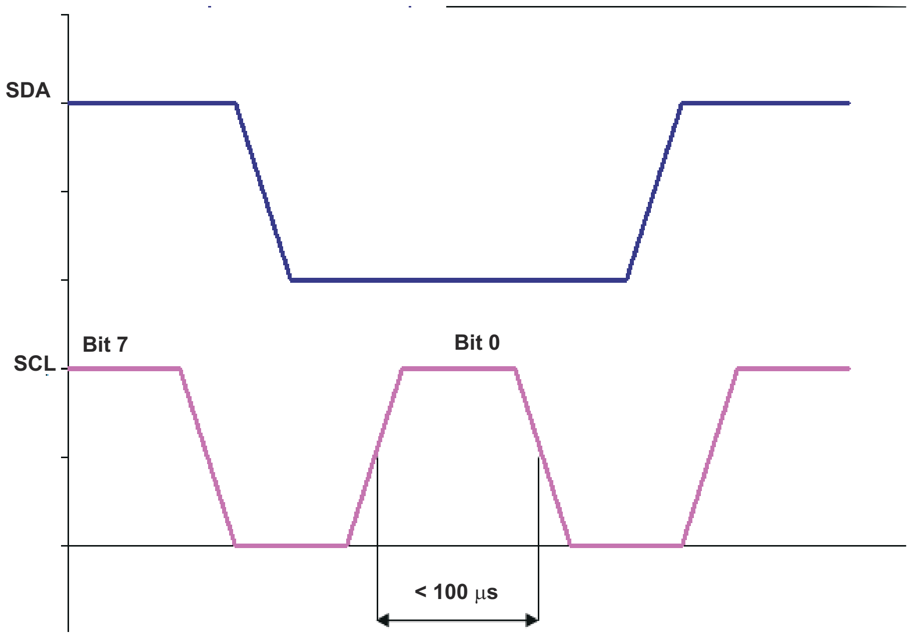

Figure 5-4. Eighth Bit of Write Command Requirements

- Read/write bit of slave address command (Figure 5-5): SCL must fall within 100 µs of SCL rising.

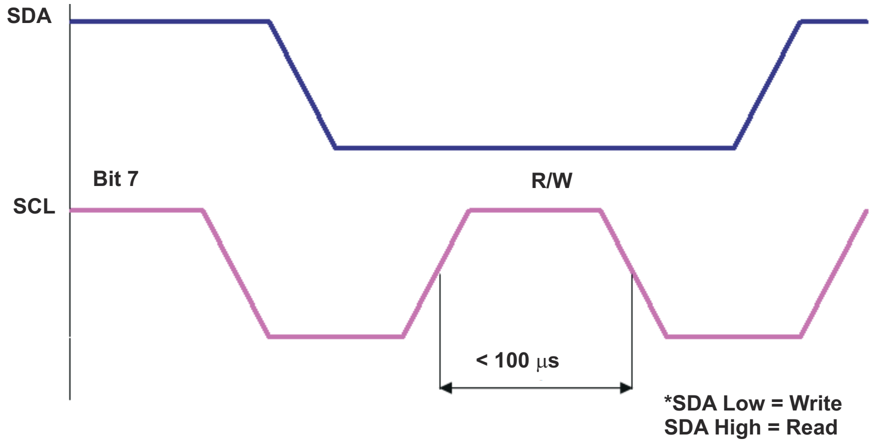

Figure 5-5. Read/Write Bit Requirements

- Acknowledge bit (Figure 5-6): Acknowledge (ACK) or no-acknowledge (NACK) occurs on the ninth rising edge of SCL during each byte. After ACK or NACK, SCL must fall within 100 µs of SCL rising.

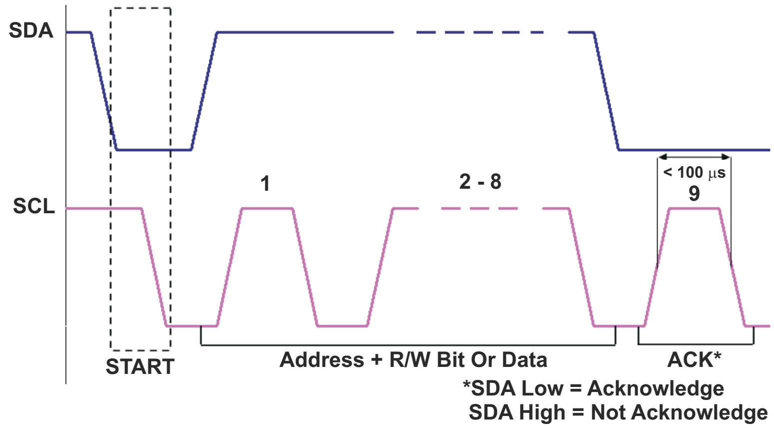

Figure 5-6. Acknowledge Bit Requirements

5.2.4 Byte or Transaction Timeout

The UCD9081 enforces a maximum byte or transaction timeout period of approximately 5 ms on the I2C master. This time is measured from the previous bytes falling SDA (during START, or repeated START) to the current bytes falling SDA (during START, or repeated START). See Figure 5-7. This timeout is not enforced for the cases when the UCD9081 holds SCL low (see Section 5.2.2) to insert additional wait states (that is, the byte timer is reset and does not expire during the stretch period).

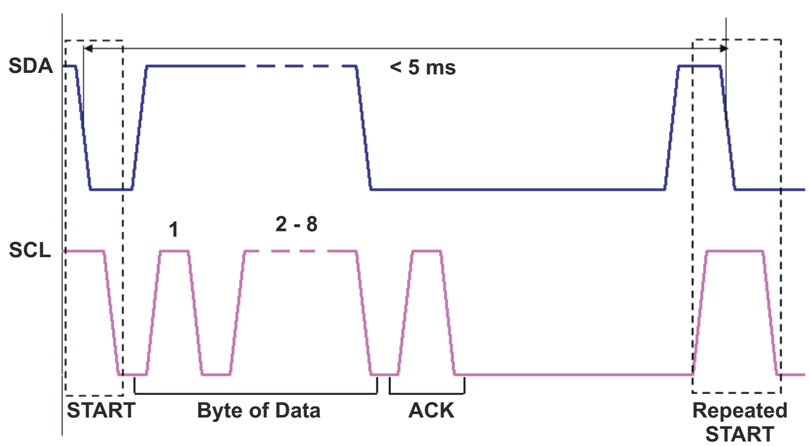

Figure 5-7. Byte Timeout Requirements

Additionally, the byte timeout period is reset when a new bit (rising edge of SCL) arrives. So, excluding the four exceptions described in Section 5.2.3, the byte timeout period applies.

6 References

1. *UCD9081, 8-Channel Power Supply Sequencer and Monitor With Error Logging* data sheet
2. *UCD9081 Power Supply Sequencer and Monitor EVM* user's guide
3. *Advanced Sequencing and Monitoring Using the UCD9081* user's guide

7 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (November 2010) to Revision C (May 2023)	Page
• Updated the numbering format for tables, figures, and cross references throughout the document	1
• Added bold on address rows E040 and E060	17
• Added Section 4.2.1 *GpDir*	18
• Added Section 4.2.2 *NegateEnablePolarity*	18
• Added Section 4.2.3 *SeqEventPending*	18