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Analog Dimming With the TPS61500 Using an Analog Input Signal

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PMP - DC/DC Low-Power Converters

ABSTRACT

Although designed to perform analog white LED dimming from a PWM input signal, the TPS61500 also can perform analog dimming from an analog input signal such as a digital-to-analog converter, for example.

Figure 1 shows how to configure the TPS61500 to perform analog dimming from an analog input signal.

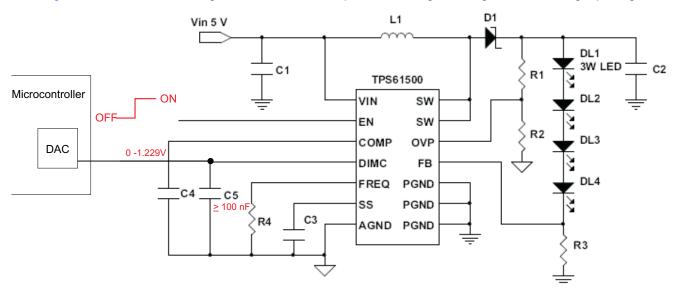


Figure 1. Circuit for the TPS61500 to Perform Analog Dimming Using an Injected Analog Signal

The analog input signal can come from the digital-to-analog converter (DAC) output of a microcontroller or a stand-alone DAC. The input analog signal (V_{DAC}) range must be from 0 to 1.229 V. This externally applied voltage overrides the internal voltage to which the DIMC pin is internally pulled up. Equation 1 gives the regulated WLED current

$$I_{LED} = \frac{V_{FBmax}}{R3} \times \frac{V_{DAC}}{1.229V}$$

(1)

1

In order for the IC to properly configure itself for analog dimming instead of PWM dimming, a capacitor of 100 nF or higher must still be connected to the DIMC pin and no external voltage higher than 0 \pm 50 mV can be applied to the DIMC pin until 200 μ s after EN is pulled high. In the event that the DAC cannot be programmed to provide 0 V when the TPS61500 is enabled, a FET with RC turnon delay circuit (shown in Figure 2) can be inserted between the DAC and DIMC pin to isolate the DAC from the DIMC until the IC has configured itself for analog dimming.



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(2)

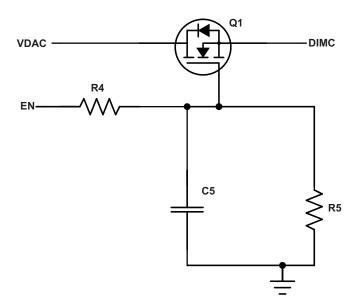


Figure 2. Isolation Circuit With RC Delayed Turnon

Equation 2 and Equation 3 show how to size the delay circuit's resistors and capacitor: $3 \times C5 \times \frac{R4 \times R5}{R4 + R5} \ge 200 \ \mu s$

1.229 V + V_{THmin} < V_{EN} ×
$$\frac{R5}{R4 + R5}$$
 < V_{GSmax} (3)

where V_{THmin} is Q1's minimum threshold voltage and V_{GSmax} is Q1's maximum gate-to-source voltage. Because low current flows through it, Q1 can be a low-cost NFET, such as the 2N7002.

Figure 3 shows the analog dimming linearity as a function of duty cycle and V_{DAC} .

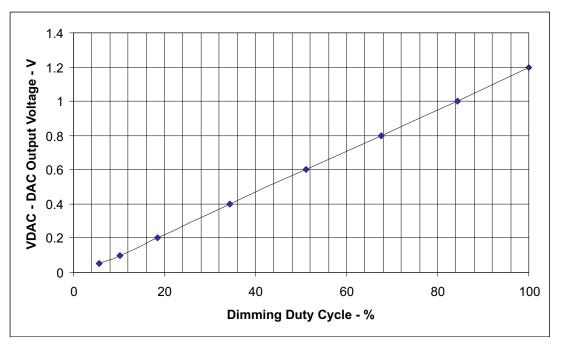


Figure 3. Analog Dimming Linearity



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Figure 4 shows the output voltage and LED current from the TPS61500EVM-369 when a 0.61-V signal is applied directly to the DIMC pin and R3 = 0.39 Ω . As expected, the regulated WLED current is 0.2 V $\times \frac{0.61 \text{ V}}{1.229 \text{ V}} = 0.254 \text{ A}$ 0.39 Ω (4) Vdac Vout C3 1<u>LED</u> C4 Measure P1:mean(C1) P2:---P3:mean(C4) P4:---P5:---P6:---541 mV 250.0 mA value status BWL DC1M Timebase -360 µs Trigger C4 DC C4 BWLIDC 28 m/ Positiva

Figure 4. Output Voltage and LED Current With $V_{IN} = 5$ V and $V_{DAC} = 0.61$ V

Note that the output voltage shows no output voltage ripple, other than the expected switching noise, on V_{OUT} when an analog signal is injected to perform analog dimming as compared to a PWM signal as shown in Figure 10 of the data sheet (SLVS893).

500 mV offset

0.0 mV offse

100 M

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