# Application Report

# TPD3S714-Q1 Functional Safety FIT Rate and Failure Mode Distribution



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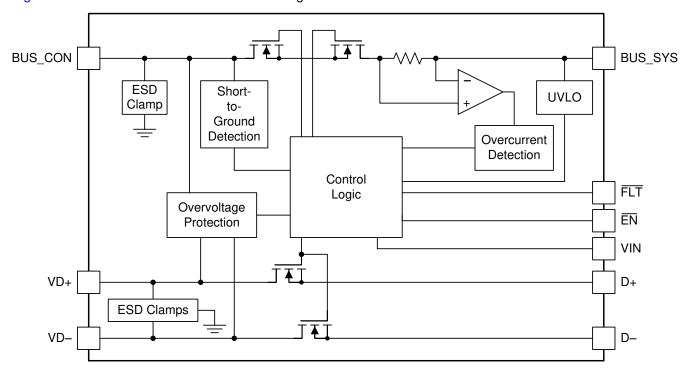
Overview www.ti.com

#### 1 Overview

This document contains information for TPD3S714-Q1 (SSOP package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- · Component failure modes and their distribution (FMD) based on the primary function of the device

Figure 1-1 shows the device functional block diagram for reference.



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Figure 1-1. Functional Block Diagram

TPD3S714-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.



### 2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for TPD3S714-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10 <sup>9</sup> Hours)		
Total FIT Rate	13		
Die FIT Rate	4		
Package FIT Rate	9		

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

· Mission Profile: Motor Control from Table 11

· Power dissipation: 250 mW

Climate type: World-wide Table 8Package factor (lambda 3): Table 17b

Substrate Material: FR4

· EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T <sub>J</sub>	
5	Digital, Analog, Mixed	20 FIT	55°C	

The Reference FIT Rate and Reference Virtual T<sub>J</sub> (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.



## 3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for TPD3S714-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)		
BUS_CON no output	25%		
BUS_CON not in specification – voltage or timing	20%		
VD+/D+, VD-/D- no output	25%		
VD+/D+, VD-/D- not in specification – voltage or timing	20%		
FLT false trip or fails to trip	5%		
Short circuit any two pins	5%		



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4	Rev	ision	Histo	rv

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from March 28,	2020 to July 20,	2020 (from	Revision *	(March 2020) to	Revision A
(July 2020))					

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