*Application Brief*

# *Space-Grade, 100-krad, –2.5-V, Discrete Negative LDO Linear Regulator Circuit*

*Nigel Smith*

## Design Goals

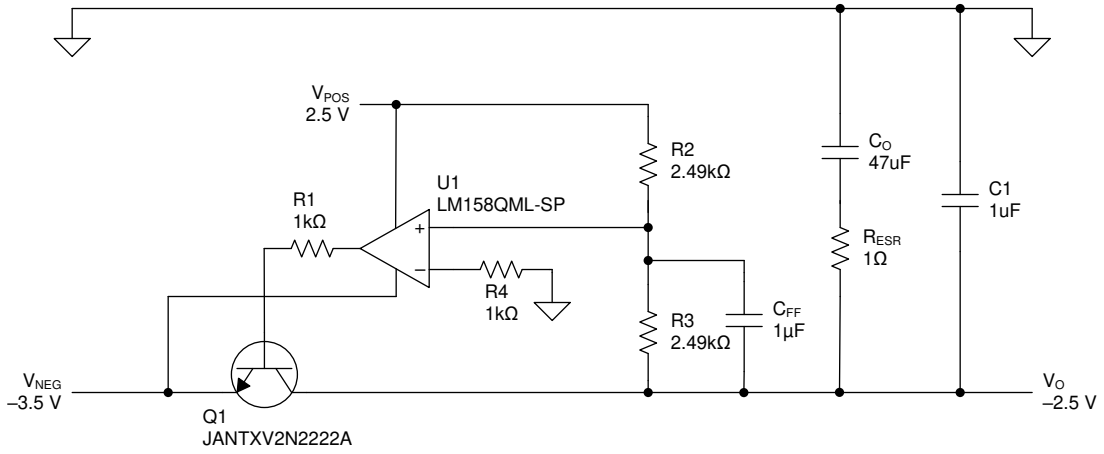
| Parameter | Design Goal |
|---|---|
| **Input voltage range** | –4 V to –3 V |
| **Output voltage** | –2.5 V |
| **Output current range** | 0 mA to 100 mA |
| **Total ionizing dose** | 100 krad (Si) |
| **Single-event latch-up immunity** | 75 MeV-cm$^2$/mg |

## Design Description

The vast majority of electronic circuits operate from one or more positive supply voltages, which is why there are many more positive voltage regulators on the market than negative ones. The dearth of negative voltage regulators is even more pronounced in the space market, where there is a very limited number of such devices. There are times, however, when a particular device or application circuit requires a negative voltage regulator.

The following figure shows a 100-mA negative low-dropout (LDO) voltage regulator circuit that that was developed to provide the negative supply voltage for a LMH5401-SP fully-differential amplifier. The circuit uses a conventional LDO architecture but uses the positive supply as its reference instead of a separate bandgap device. For applications like powering an amplifier, the absolute accuracy of the supply voltage is not critical, and using the positive supply is a simple and cost-effective way to achieve the required performance.

Note that the feedback network is connected to the *non-inverting* input of the op-amp because of the signal inversion caused by Q1.



## Design Notes

The power dissipation and junction temperature in pass transistor Q1 must not exceed the maximum values allowed by the device and by your application. In space applications, the maximum allowed power dissipation in a transistor may be significantly less than the rating of the device. For example, the European Space Agency (ESA) recommends a derating factor of 65%. Similarly, although Q1 is specified with a maximum junction temperature of 200°C, ESA recommends a junction temperature not greater than 110°C. In applications with a large voltage drop across the negative regulator, the power dissipation in Q1 might exceed the maximum allowed. However, in such applications there no need for an LDO regulator and a standard type with larger dropout such as the LM137QML-SP can be used.

The op-amp used in this circuit must have an output stage capable of operating close to the negative supply rail of the op amp. The LM158QML-SP was chosen for this circuit because it meets this criterion, has a long space heritage, and withstands a total ionizing dose up to 100 krad (Si). Other op amps can be used, but the feedback stabilization may need to be adjusted to suit the frequency response of the op amp.

## Design Steps

- Choose R2 so that the current flowing through the feedback network is approximately 1 mA.

$$R2 = \frac{V_{POS}}{1\ mA} = \frac{2.5\ V}{1\ mA} = 2.5\ k\Omega$$

- Choose R3 to set the output voltage to the desired value.

$$R3 = -\frac{V_O \times R2}{V_{POS}} = -\frac{-2.5\ V \times 2.5\ k\Omega}{2.5\ V} = 2.5\ k\Omega$$

- Choose a product of output capacitance $C_O$ and equivalent series resistance $R_{ESR}$ to generate a zero below 10 kHz (lower is generally better). The frequency of the ESR zero is given by:

$$f_{z(ESR)} = \frac{1}{2\pi R_{ESR} C_O} = \frac{1}{2\pi(1)(47 \times 10^{-6})} = 3.39\ kHz$$

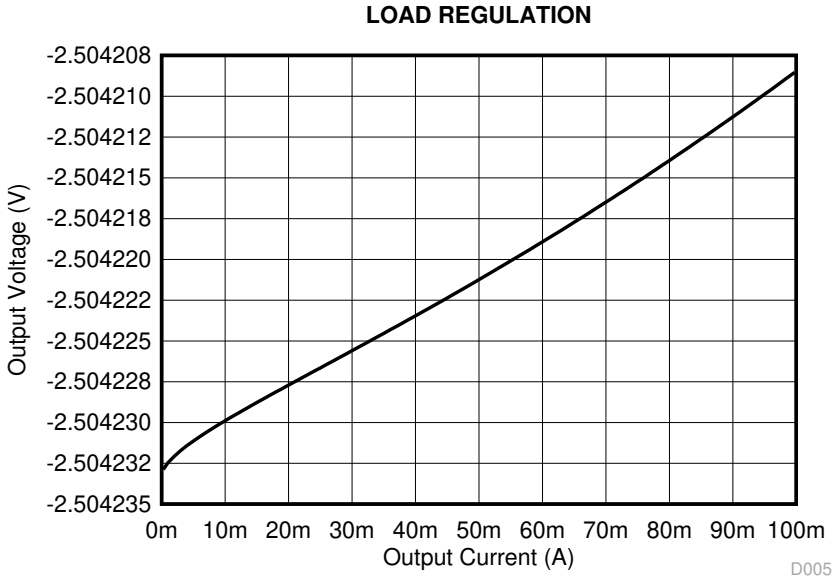
  $R_{ESR}$ can be either inherent in the capacitor used or included separately in series with a low-ESR capacitor (as it was in this case).
- An optional feedforward capacitor $C_{FF}$ across the feedback network provides an additional zero that improves transient response. The value of $C_{FF}$ is best selected experimentally. Note that $C_{FF}$ cannot be used on its own to stabilize the loop. This is because the pole and the zero formed by R2, R3, and $C_{FF}$ are too close to each other in the frequency domain to stabilize the loop over the whole range of output currents.
- An additional capacitor, C1, reduces the initial voltage step response caused by the relatively high value of $R_{ESR}$. The value of C1 is low compared to $C_O$ and does not significantly affect stability.

## Design Simulations

### DC Simulation Results

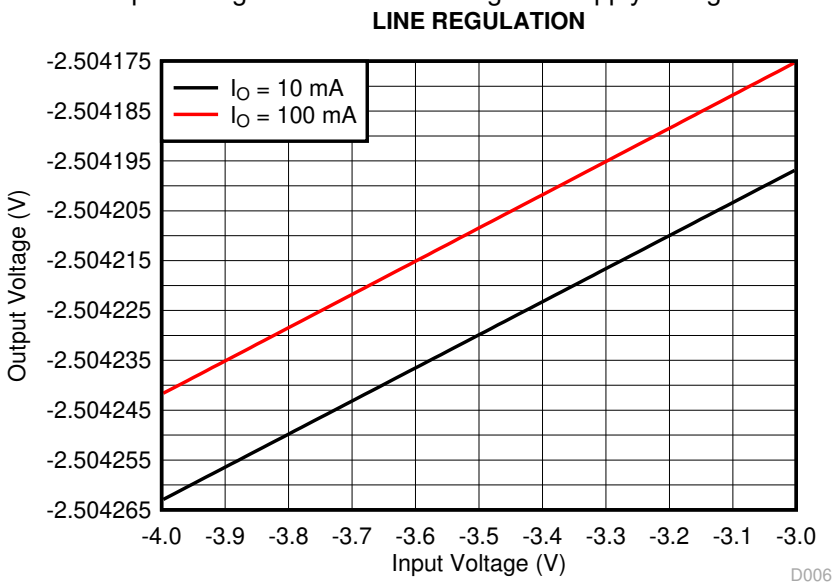
#### Load Regulation

The following plot shows the output voltage variation as the output current varies from 0 mA to 100 mA.



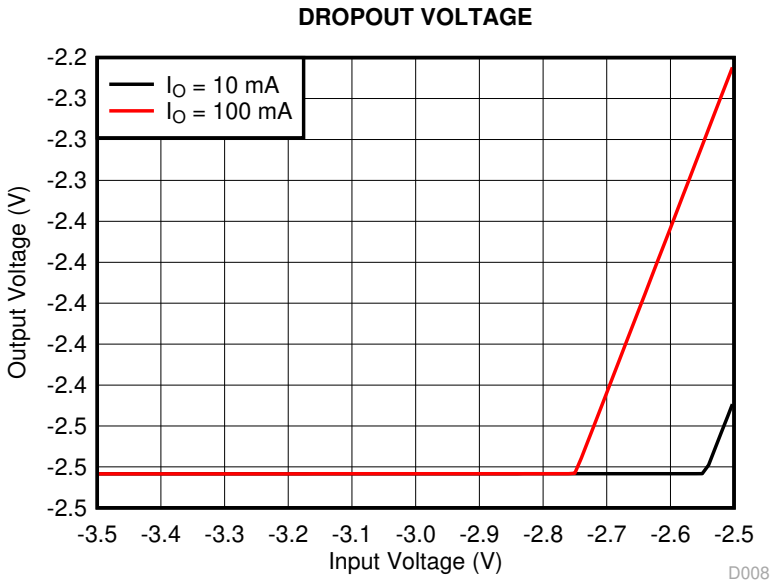

#### Line Regulation

The following plot shows the output voltage variation as the negative supply voltage varies from –4 V to –2 V.



### Dropout Voltage

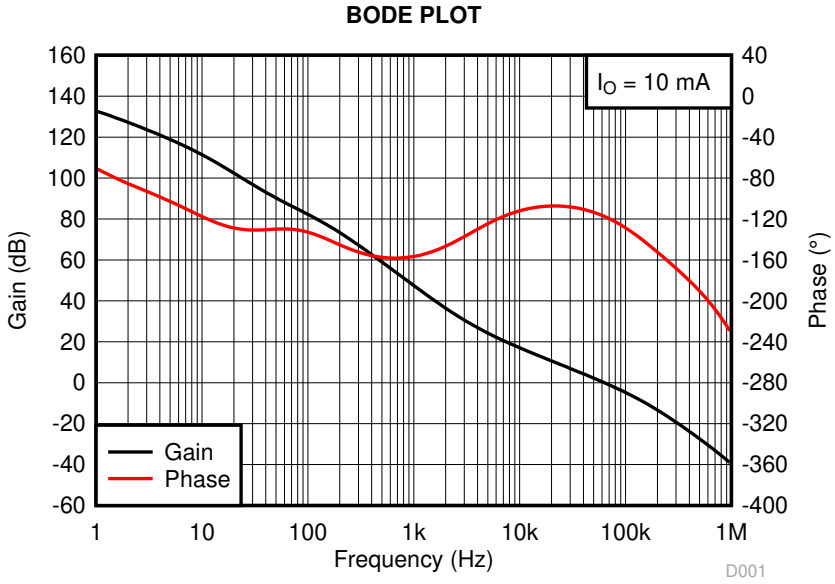
The following plot shows the dropout voltage for load currents of 10 mA and 100 mA.



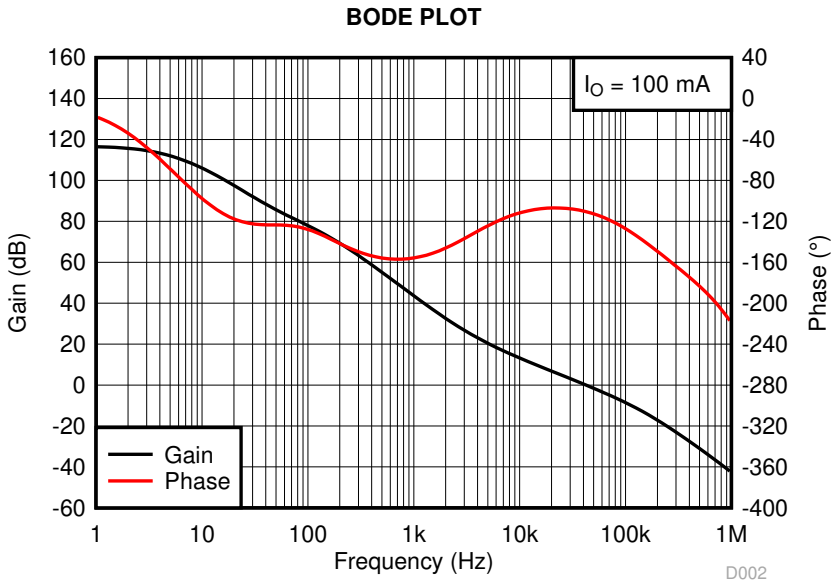

### AC Simulation Results

### Stability

The following plot shows the frequency response of the circuit with an output current of 10 mA.

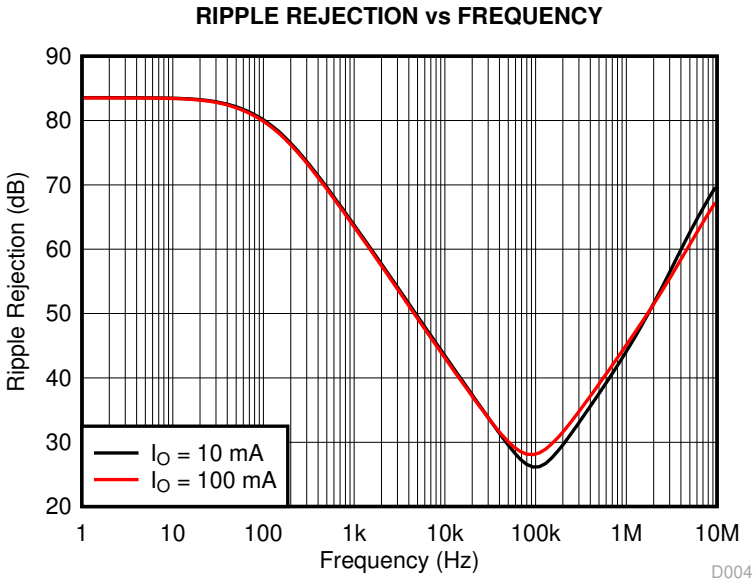


The following plot shows the frequency response of the circuit with an output current of 100 mA.




## Ripple Rejection

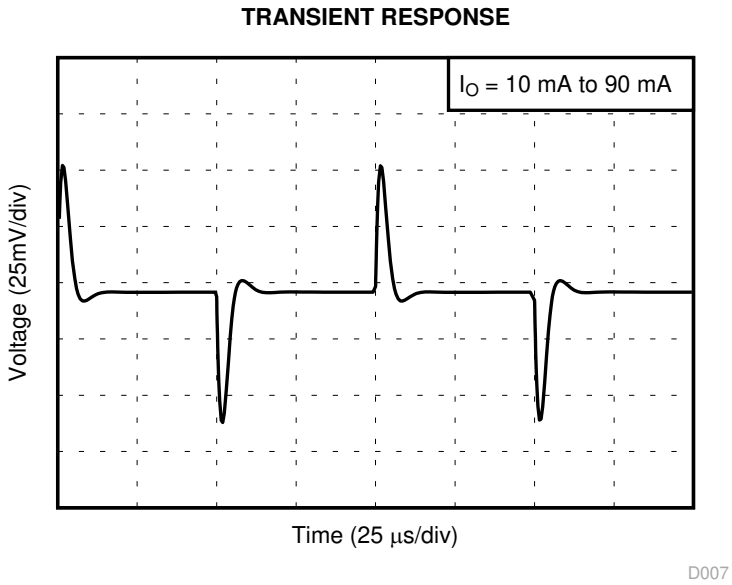
The following plot shows the simulated ripple rejection of the circuit.



## Transient Simulation Results

### Load Transient Response

The following scope plot shows the transient response of the circuit to a 10-mA to 90-mA load step.




## Design References

Texas Instruments, *AN-1482 LDO Regulator Stability Using Ceramic Output Capacitors Application Report*

## Design Featured Op Amp

| LM158QML-SP | |
|---|---|
| **Supply voltage range** | 3 V to 32 V |
| **Supply current per channel (typical)** | 0.35 mA |
| **Input common-mode voltage range** | 0 V to $V_{CC}$ – 1.5 V |
| **Output voltage range** | 0 V to $V_{CC}$ – 1.5 V |
| **Input offset voltage (max @ 25°C)** | 2 mV |
| **Input bias current (max)** | 50 nA |
| **Unity-gain bandwidth (typ)** | 0.7 MHz |
| **Slew rate** | 0.5 V/µs |
| **#Channels** | 2 |
| **Total ionizing dose** | 100 krad (Si) |
| **Single-event latch-up immunity** | N/A (bipolar) |
| www.ti.com/product/lm158qml-sp | |

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265