*Application Note*

# *Parallel Operation of Two TPS61287 Boost Converters*

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**ABSTRACT**

In most use cases such as Bluetooth speakers and USB Type-C power delivery, the input is Li-battery and output power reaches 90W or more. One converter is hard to output enough power and paralleled models are commonly used.

Usually, with device variations at the worst condition, the output current of one device can only be 50% of the other one, which greatly reduces the tolerable output load. Additionally, battery systems are sensitive to input current ripple, and the converters' inductor current overlap in phase is not conducive to the systems.

This application note demonstrates a method that connect two TPS61287 devices in parallel to support higher output power. This method is to connect the VIN, VOUT, FB and COMP pin of the two devices together, also uses the synchronization function of TPS61287 to achieve current sharing and phase-shift control.

The synchronization delay can be estimated and customers can select either a DRV signal or SW signal as the synchronization signal through a RC divider. In most cases,using SW signal as the synchronzation input makes a phase shift of about 50% switching period and is good for parallel working.

Bench test results shows that the method can realize the interlaced parallel output of two boost converters, significantly reducing the current input ripple and maximizing the output power.

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# 1 Introduction

## 1.1 Introduction of TPS61287

The TPS61287 is a high-power density, synchronous boost converter that integrates high side synchronous rectifier MOSFET and uses an external low side MOSFET to provide a high efficiency and small size. The TPS61287 has wide input voltage range from 2V to 23V and the output voltage covers up to 25V with 20A switching valley current capability.

The TPS61287 uses adaptive constant on-time valley current control topology to regulate the output voltage and supports stackable multiphase operation. Up to four pieces of TPS61287 can be configured for multi-phase operation at the same switching frequency to support higher power and input current balancing.

## 1.2 Design with the Paralleled TPS61287

Figure 1-1 shows the schematic of two TPS61287s working in parallel. The VIN, VOUT, FB and COMP pins of the two devices are connected together.

The M/SYNC of the host device is connected to ground. The M/SYNC of the subordinate device can either connect to the DRV pin or the SW of the host device through a RC divider. TI recommends using forced PWM mode for a better current balance and reliable phase shifting.

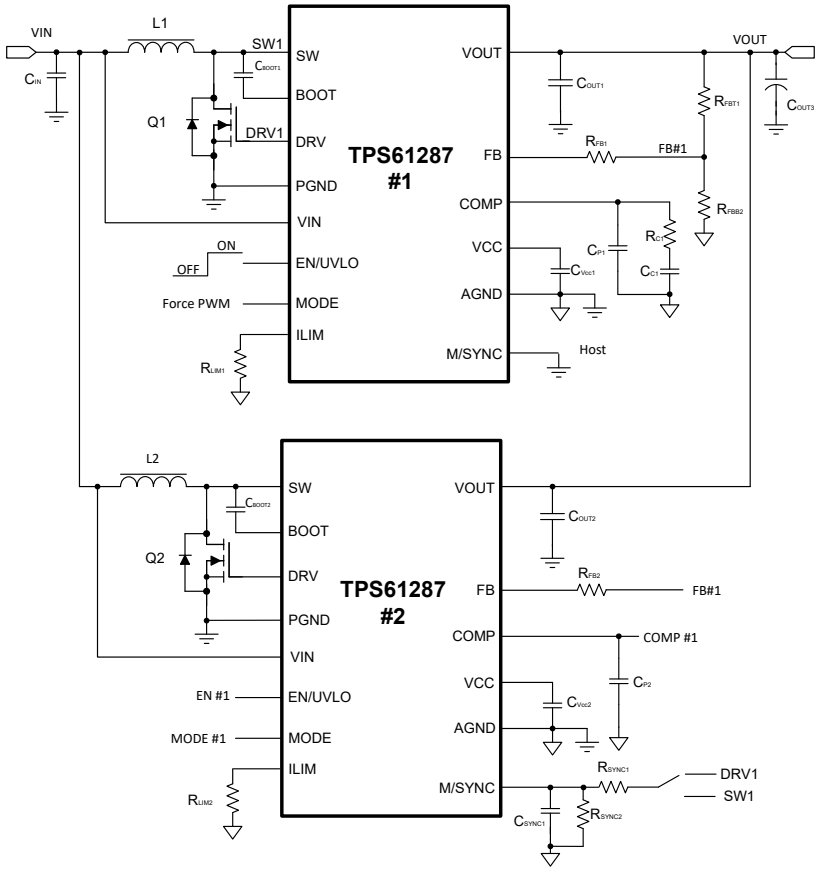


**Figure 1-1. TPS61287 Paralleled Schematic for High Power Application**



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## 1.3 Synchronization Function

The synchronization function block diagram of TPS61287 is shown in Figure 1-2.

When an external clock signal is applied to the M/SYNC pin, the synchronization circuit generates a synchronized saw-tooth wave signal to modulate the Ton time; this synchronizes the switching frequency to the external clock.

The external clock frequency must be within ±20% of default the switching frequency of 320kHz. The external clock on the M/SYNC pin must have a low-level voltage less than 0.4V and a high-level voltage greater than 1.2V. A valid synchronous clock signal must be greater than 50ns wide and have a minimum of four consecutive clocks prior to synchronization.

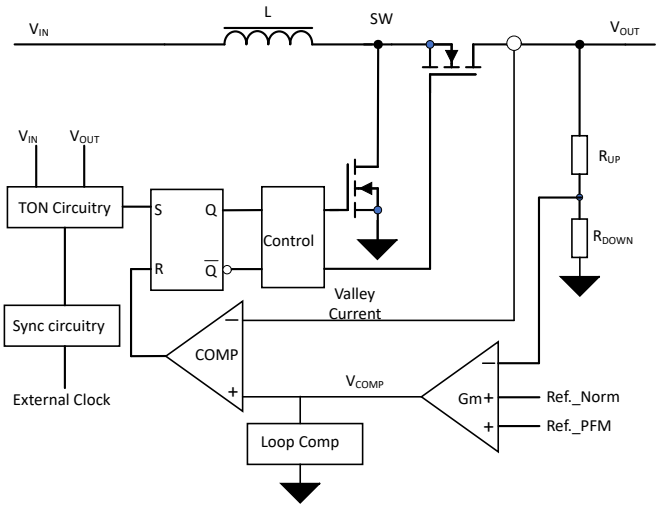


**Figure 1-2. TPS61287 External Synchronization Function Block Diagram**

When using muti-phase TPS61287, the M/SYNC of the subordinate device can either connect to the DRV or the SW of the host device through an RC divider.

Figure 1-3 shows the waveforms when using DRV signal as the sync input. The DRV voltage is within the voltage derating of the M/SYNC pin, so, the resistor divider is usually not required. The RC filter can be added to generate additional time delay to adjust the phase shift. The total phase shift between two devices is the delay phase added by the duty cycle.

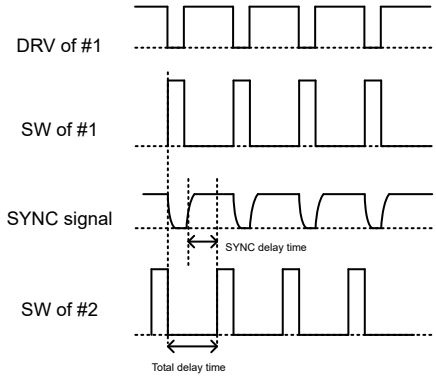


**Figure 1-3. Use DRV as the SYNC Input**

Figure 1-4 shows the waveforms when using SW signal as the sync input. Usually the SW signal voltage is much higher than the derating of M/SYNC pin, and a resistor divide is needed. The actual phase shift is just the sync delay.


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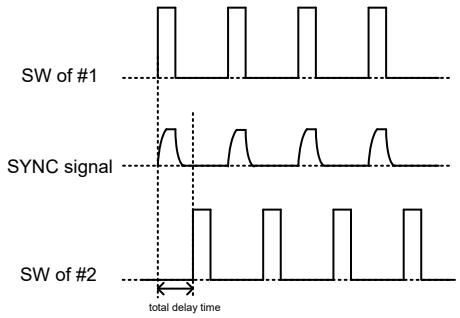


**Figure 1-4. Use SW as the SYNC Input**

## 1.4 Phase Delay Details

The synchronization delay time is defined as the time delay between rising edge of the synchronization signal and the rising edge of the generated SW rising edge.

**Table 1-1. Delay Time and Phase Related with Duty Cycle**

| Duty Cycle | delay time | delay phase |
|---|---|---|
| 10% | 2.01us | 64.3% |
| 20% | 1.89us | 60.5% |
| 30% | 1.78us | 57.0% |
| 40% | 1.71us | 54.7% |
| 50% | 1.66us | 53.1% |
| 60% | 1.68us | 53.8% |
| 70% | 1.66us | 53.1% |
| 80% | 1.65us | 52.8% |
| 90% | 1.64us | 52.5% |

Table 1-1 lists the estimated typical delay time and delay phase related with the duty cycle. TPS61287 has carefully designed to make about 50% of the phase delay in most cases.

In this design, SW signal voltage is used as the SYNC signal with a resistor divide. The actual phase shift is just around 50%.



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# 2 Bench Performance of TPS61287 in Parallel

This chapter describes the bench tested performance of two TPS61287 devices working in parallel. Thermal performance, switching waveforms, output ripple and efficiency result are included. Output ripple waveforms without synchronization function are also attached in comparison.

Figure 2-1 shows the top view of the TPS61287 dual-phase EVM.

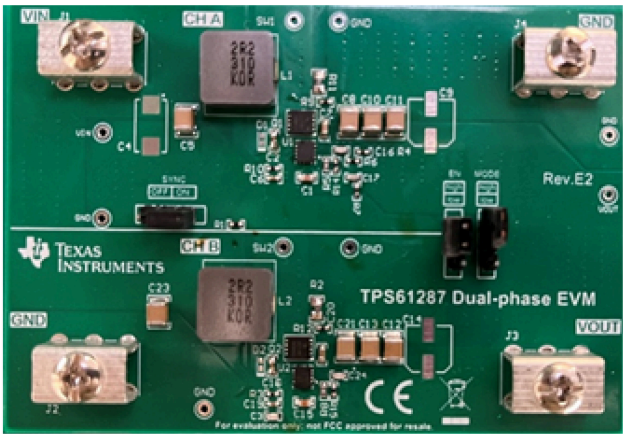


**Figure 2-1. TPS61287 Dual-Phase EVM Top View**

Table 2-1 lists the desired performance of paralleled TPS61287.

**Table 2-1. Design Parameters**

| Design Parameters | Example Values |
|---|---|
| Input voltage range | 3.3V to 4.2V |
| Output voltage | 18V |
| Output voltage ripple | 200mV peak-to-peak |
| Output current rating | 6A |

## 2.1 Thermal Performance

The EVM is a 4 layer PCB, 2oz copper for the outer layer, and 1oz copper for the inner layer. Better thermal performance can be achieved with a thicker copper PCB. The two thermal images Figure 2-2 and Figure 2-3 show the thermal conditions at input voltages of 3.3V and 4.2V. For higher input voltage, the thermal performance is better.

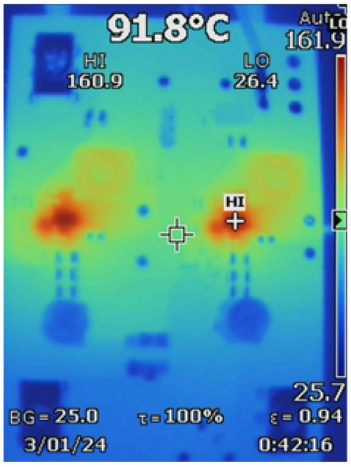


**Figure 2-2. Thermal Image of $V_{IN}$= 3.3V, $V_{OUT}$ = 18V**

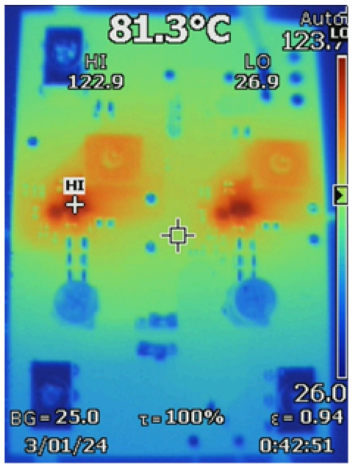


**Figure 2-3. Thermal Image of $V_{IN}$= 4.2V, $V_{OUT}$ = 18V**


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## 2.2 Switching Waveform

Figure 2-4 to Figure 2-9 show the waveforms of switching node and inductor current at different input voltages under no-load and full-load conditions. SW is used as the synchronization signal and phase shift is about 50% of the switching period. The waveforms shows improved switching phase shift and current balance.

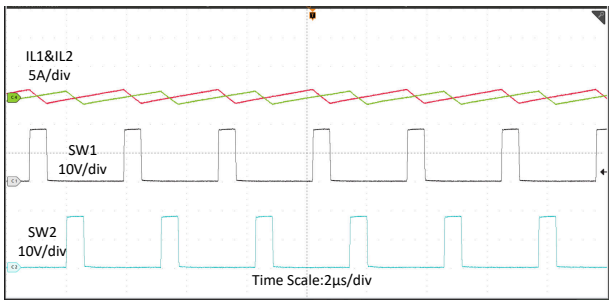


**Figure 2-4. Switching Waveforms in 0A Load**

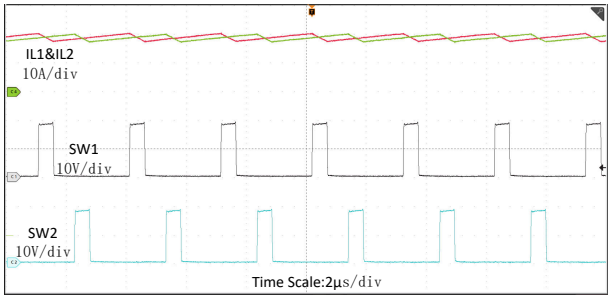


**Figure 2-5. Switching Waveforms in 6A Load**

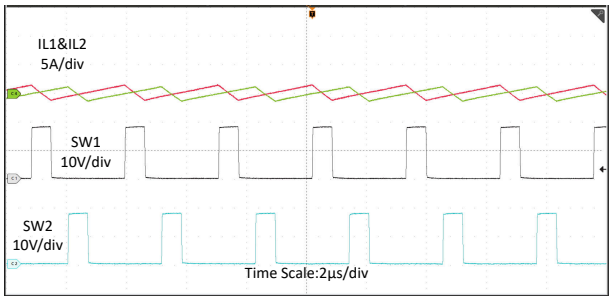


**Figure 2-6. Switching Waveforms in 0A Load**

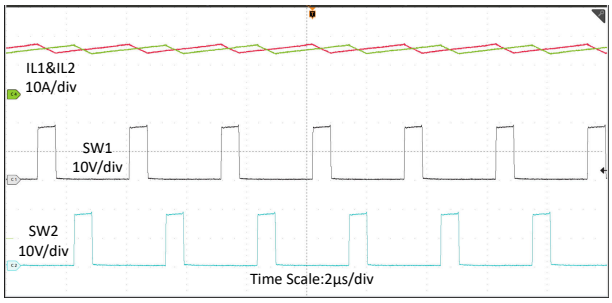


**Figure 2-7. Switching Waveforms in 6A Load**

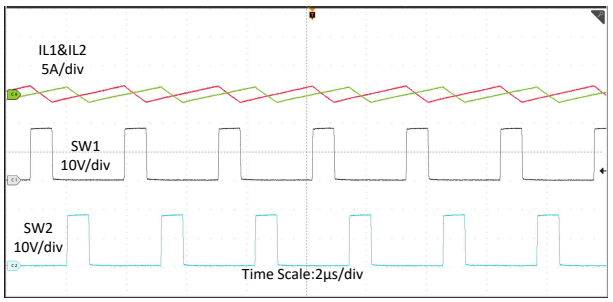


**Figure 2-8. Switching Waveforms in 0A Load**

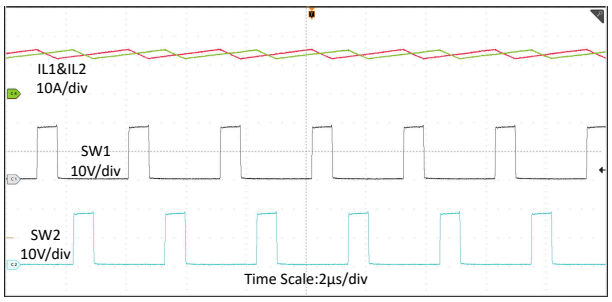


**Figure 2-9. Switching Waveforms in 6A load**



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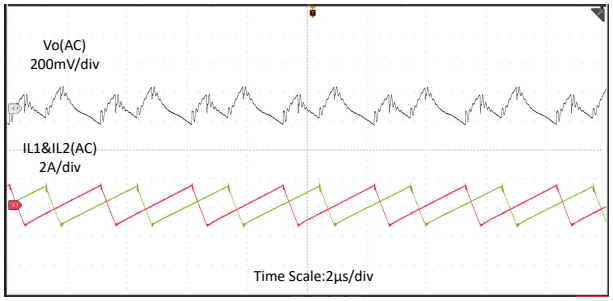
## 2.3 Ripple Waveform

The waveforms of output AC ripples are shown in this section. Figure 2-10 and Figure 2-11 shows the output ripple waveforms with different input voltage with synchronization functions. The output voltage ripple is within 200mV.

Figure 2-12 to Figure 2-15 show the output ripple AC ripples of two TPS61287 devices in parallel without using the synchronization function. The switching moments of the two devices cannot be simultaneous, causing the peak-to-peak values of the inductor current to overlap, which increases the output voltage ripple and beating frequency. The output voltage ripple reaches 400mV.




$V_{IN}$ = 3.3V $V_{OUT}$ = 18V $I_{OUT}$ = 6A

**Figure 2-10. Output Voltage Ripple and Inductor Current with Synchronization Function**

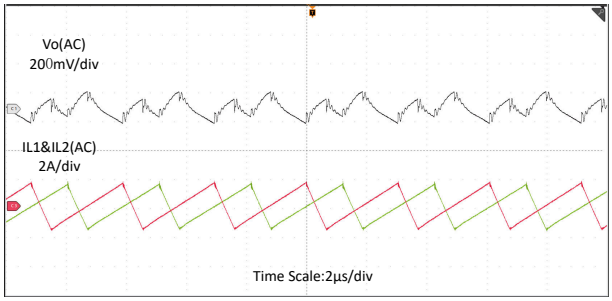



**Figure 2-11. Output Voltage Ripple and Inductor Current with Synchronization Function**

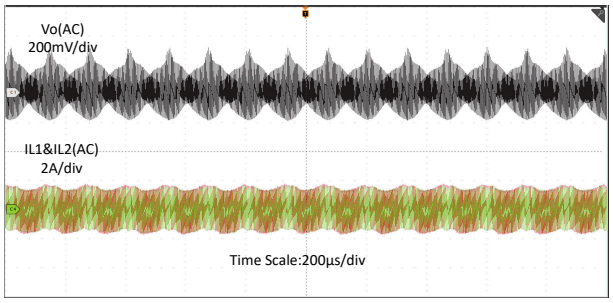



**Figure 2-12. Output Voltage Ripple and Inductor Current without Synchronization Function**

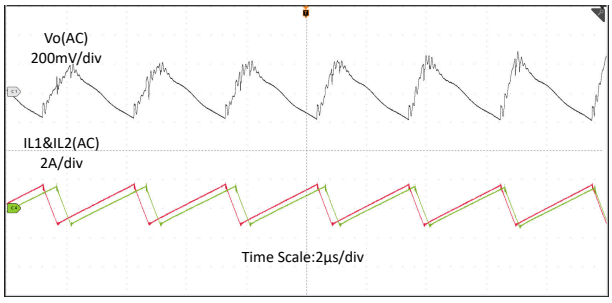



**Figure 2-13. Output Voltage Ripple and Inductor Current without Synchronization Function Zoom in**

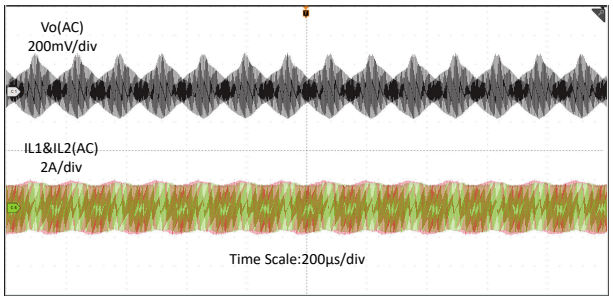



**Figure 2-14. Output Voltage Ripple and Inductor Current without Synchronization Function**

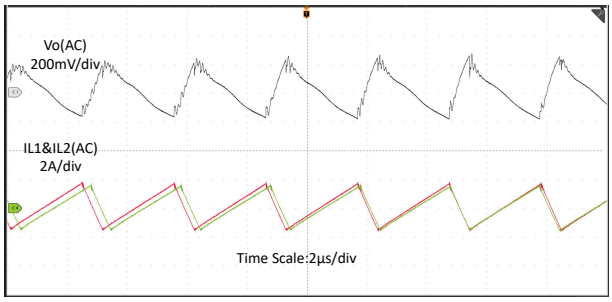



**Figure 2-15. Output Voltage Ripple and Inductor Current without Synchronization Function Zoom in**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## 2.4 Efficiency

Figure 2-16 shows the efficiency curves of loads from 0.1A to 6A under different input voltages at 18V output.

The highest efficiency reaches 94.5% at 4.2V input and 18V 3A output.

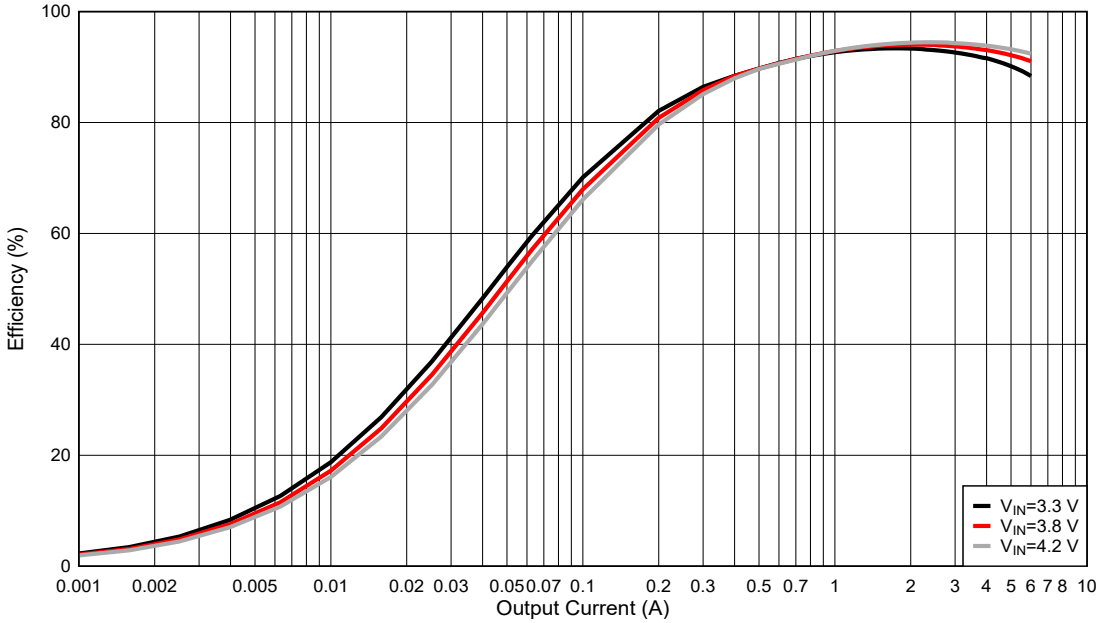


**Figure 2-16. Efficiency vs Output Current**

$V_{IN}$ = 3.3V; 3.8V; 4.2V $V_{OUT}$ = 18V



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## 3 Summary

This application note demonstrates a method that connects two TPS61287 devices in parallel to support higher output power. This method is to connect the VIN, VOUT, FB and COMP pins of the two devices together. This method also uses the synchronization function of TPS61287 to achieve current sharing and phase-shift control. The bench test result shows that the method can realize the interlaced parallel output of two boost converters, significantly reducing the current input ripple and maximizing the output power.

## 4 References

1. Texas Instruments, *TPS61287 23VIN, 25VOUT, 20A Synchronous Boost Converter with Stackable Multi-Phase Function*, datasheet.



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