PR419
TMS320VC550x Design 2

FEATURES:

- Provides sequenced core and I/O voltages from input voltages from 1.2 V to 3.0 V.
- /RESET delay fixed at 80 ms minimum, 120ms typical.
- Capable of single cell operation
- The current draw on the input power supply is minimized by sequencing the core rail first and then the I/O rail.

IMPORTANT WEB LINKS:

- Link to the TI power management home page at http://power.ti.com then select the TI DSP Solutions link for more information and other reference designs.
- Link to datasheets at:
  - http://focus.ti.com/lit/ds/symlink/tps70202.pdf
  - http://focus.ti.com/lit/ds/symlink/tps61020.pdf
  - http://focus.ti.com/lit/ds/symlink/tps3103k33.pdf

- Link to application note SLVA118 http://focus.ti.com/lit/an/slva118/slva118.pdf to explore the thermal considerations in using linear regulators.

THEORY OF OPERATION:

PR419 consists of a cascaded TPS61020 boost converter and a TPS70202 dual linear regulator. The circuit uses the TPS61020 to boost the input voltage up to a regulated 3.6 V. The 3.6 V is used as the input voltage to the TPS70202 dual linear regulator which regulates the 3.6 V down to the 3.3 V I/O voltage and the selected Core voltage.

CIRCUIT LIMITATIONS AND CAPABILITIES:

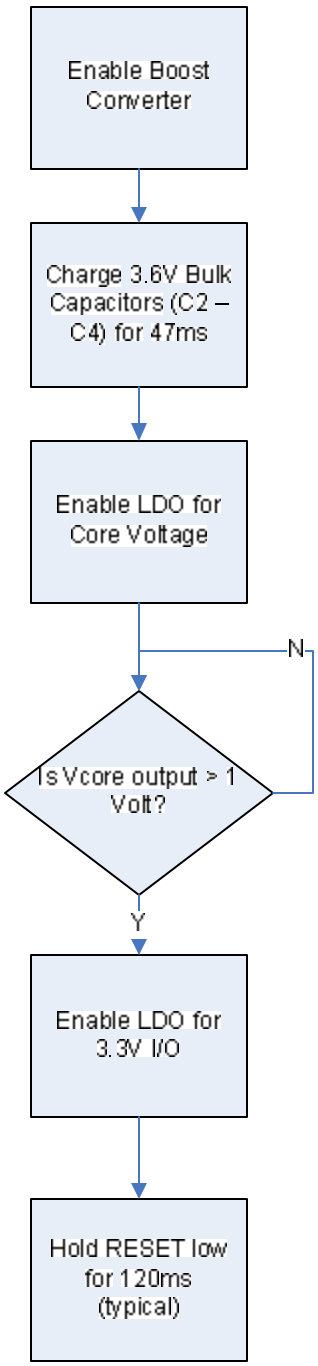
The TPS61020 is capable of supplying about 350 mA of current with an input voltage of 1.8 V. Since the TPS61020 supplies both the I/O and Core LDO inputs, the sum of these currents can not exceed 350 mA. This limit should be checked against the application. For the current capability at other input voltages, refer to Figure 1 of the TPS61020 datasheet. Higher input voltages allow for higher output current from the TPS61020.

Though not preferred, the TPS61020 is also capable of regulating from input voltages higher than the output voltage. TPS61020 operates like a linear regulator once the input voltage is higher than 3.3 V. Therefore, the TPS61020 will still produce a regulated 3.6 V for the TPS70202 with up to 5.5 V on the input. Since the TPS61020 is a linear regulator at higher input voltages, its efficiency will decrease substantially and its power

dissipation will increase significantly. Close attention should be paid to the thermal performance of the TPS61020 operating in this condition.

The TPS70202 is capable of supplying up to 500 mA of core current and 250 mA of I/O current, assuming the TPS61020 can provide the sum of the core and I/O currents based on the input voltage. Since the TPS61020 provides a constant 3.6 V input to the TPS70202, the power dissipation of the TPS70202 is a maximum of 1.075 Watts. This dissipation is low enough to allow the TPS70202 to operate over the full temperature range.

POWER UP SEQUENCING:



The circuit will apply the I/O voltage immediately after the core voltage is above about 1.0 volt. This 1.0V point will vary with the characteristics of the small signal transistors being used in the sequencing circuit. Some applications may require a longer time delay between the core and I/O voltage applications. A capacitor can be added between the

base of Q1 and ground to slow the turn on of the I/O voltage. The turn on time would be delayed by the RC time constant created by R4 and the added capacitor.

The sequencing circuit, consisting of components R3, R4 and Q1, can be removed if sequencing is not required. The I/O rail LDO enable (EN2) would then be tied to the EN1. This will not effect the minimum duration of the RESET signal.

IMPLEMENTATION NOTES:

- **Component selection:**
  - If different capacitors are used for C6 and C7 than recommended per the BOM, they must meet the ESR requirements per the TPS70202 datasheet.

WAVEFORMS:

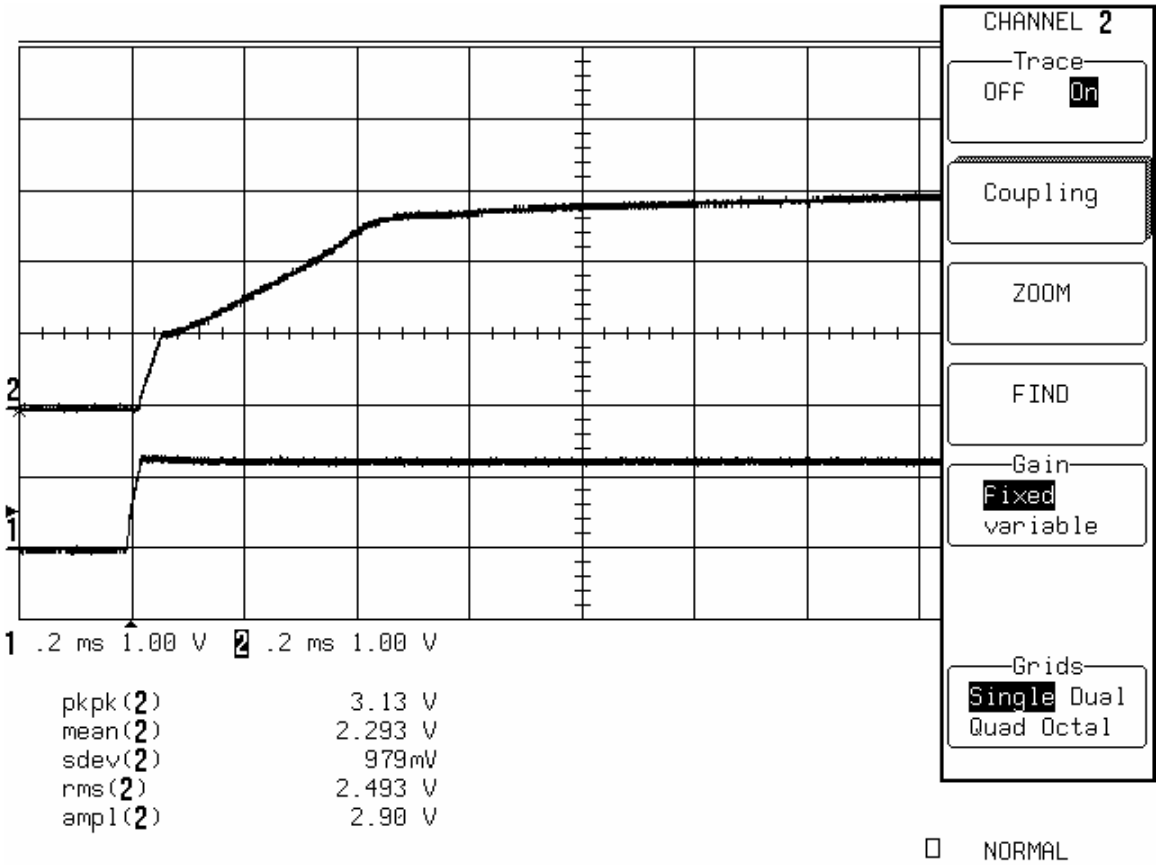


Figure 1 - Power up with V_{IN} = 1.2 V, Vcore=1.2 V @ 110 mA, Vi/o = 3.3 V @ 50 mA

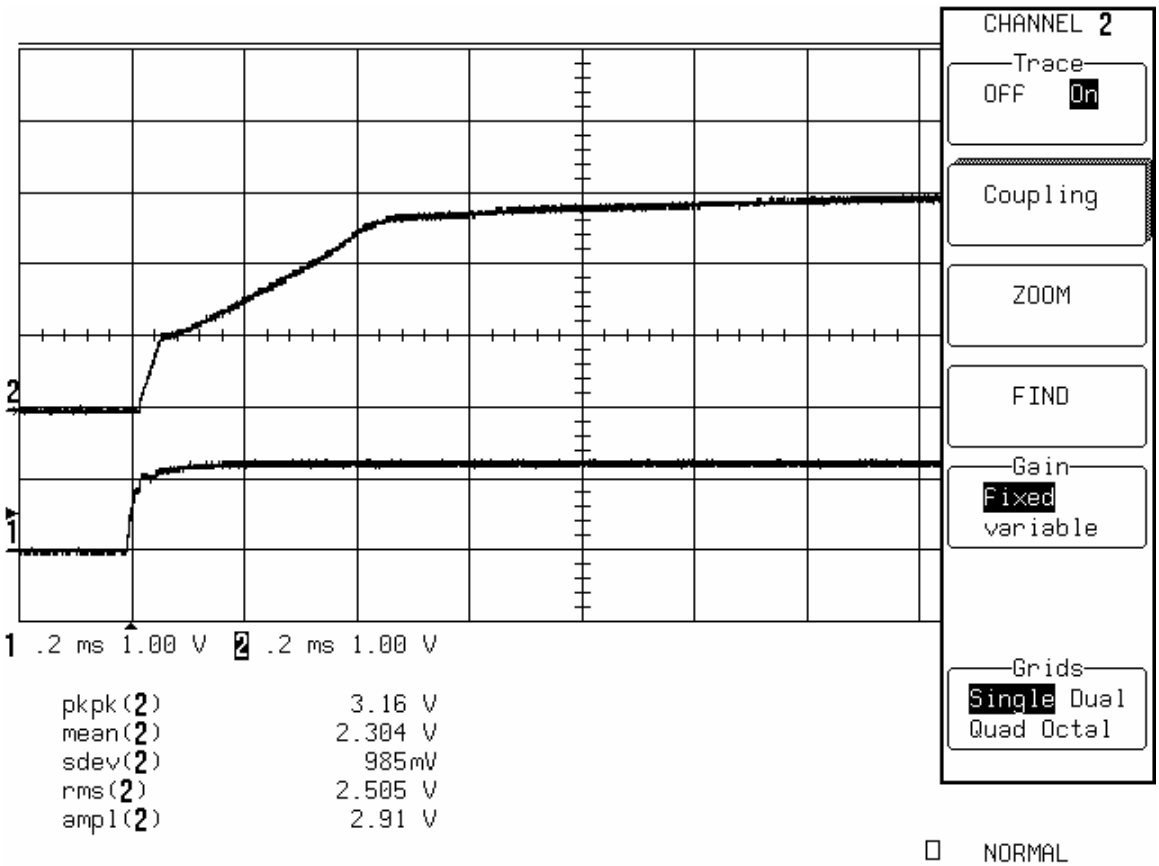


Figure 2 - Power up from Enable when V_{IN} = 1.2 V, Vcore=1.2 V@ 110 mA, Vi/o = 3.3 V @ 50 mA

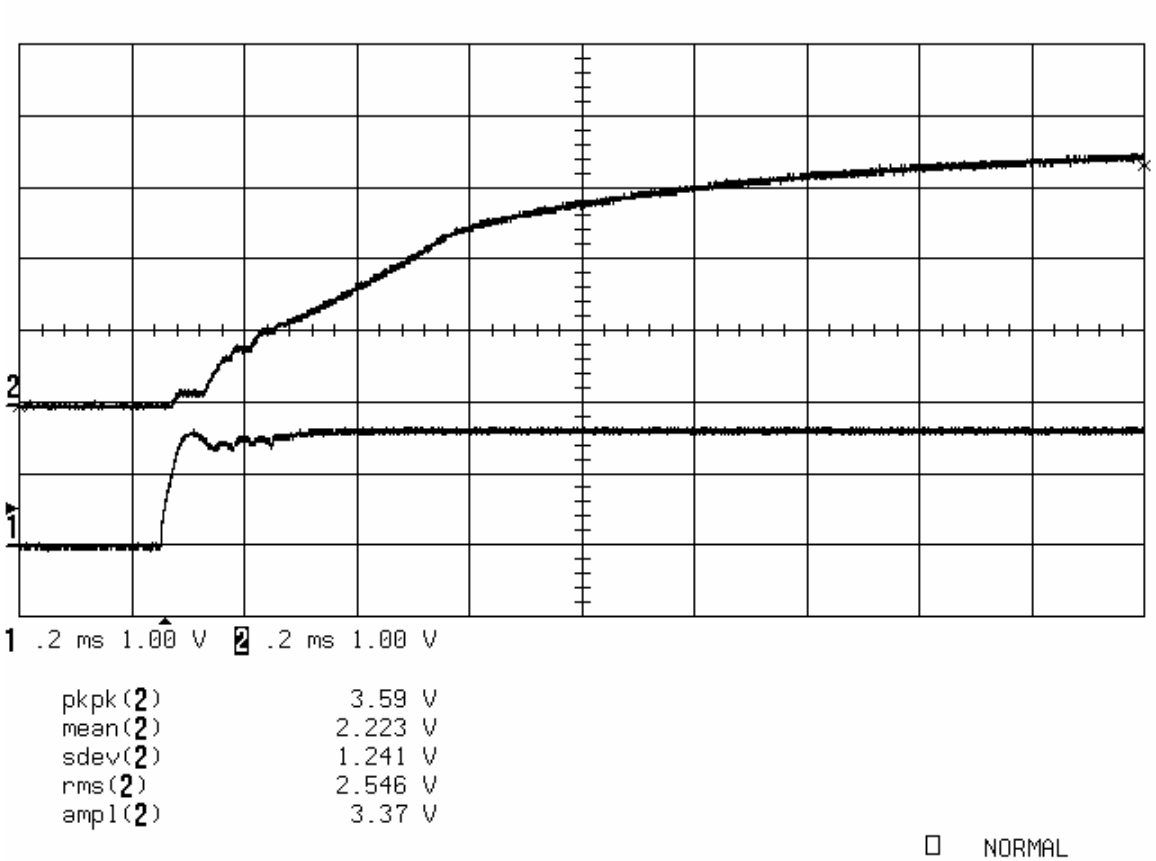


Figure 3 - Power up with V_{IN} = 1.5 V, Vcore=1.6 V@ 267 mA, Vi/o = 3.3 V @ 70 mA

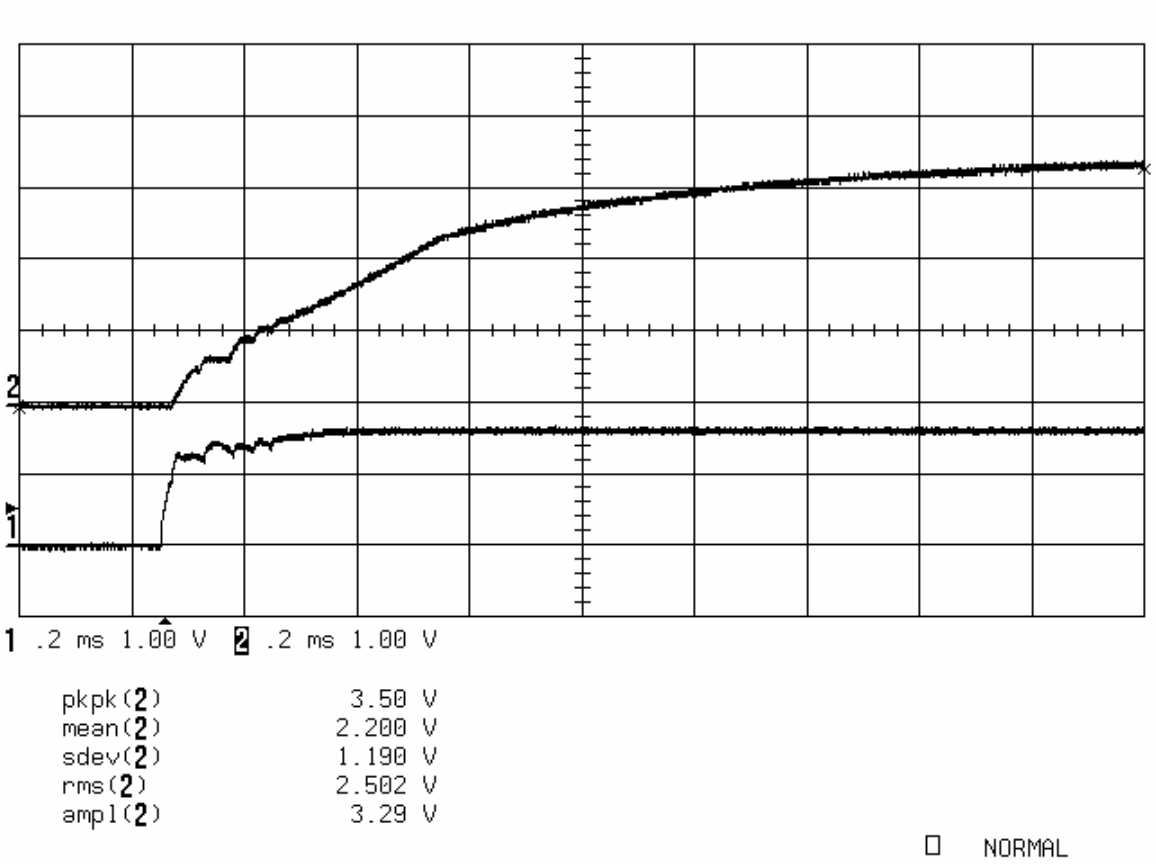


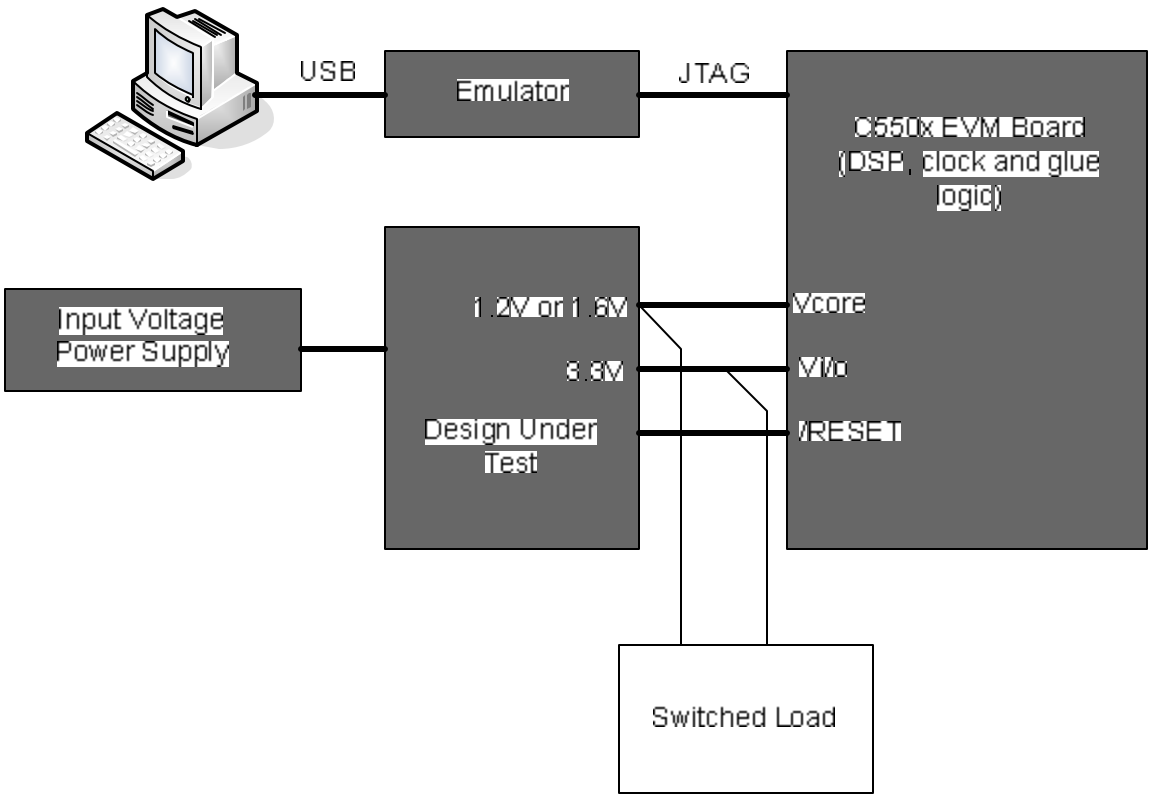
Figure 4 - Power up from Enable when V_{IN} = 1.5 V, Vcore=1.6 A @ 267 mA, Vi/o = 3.3 V @ 70 mA

TESTING METHOD:

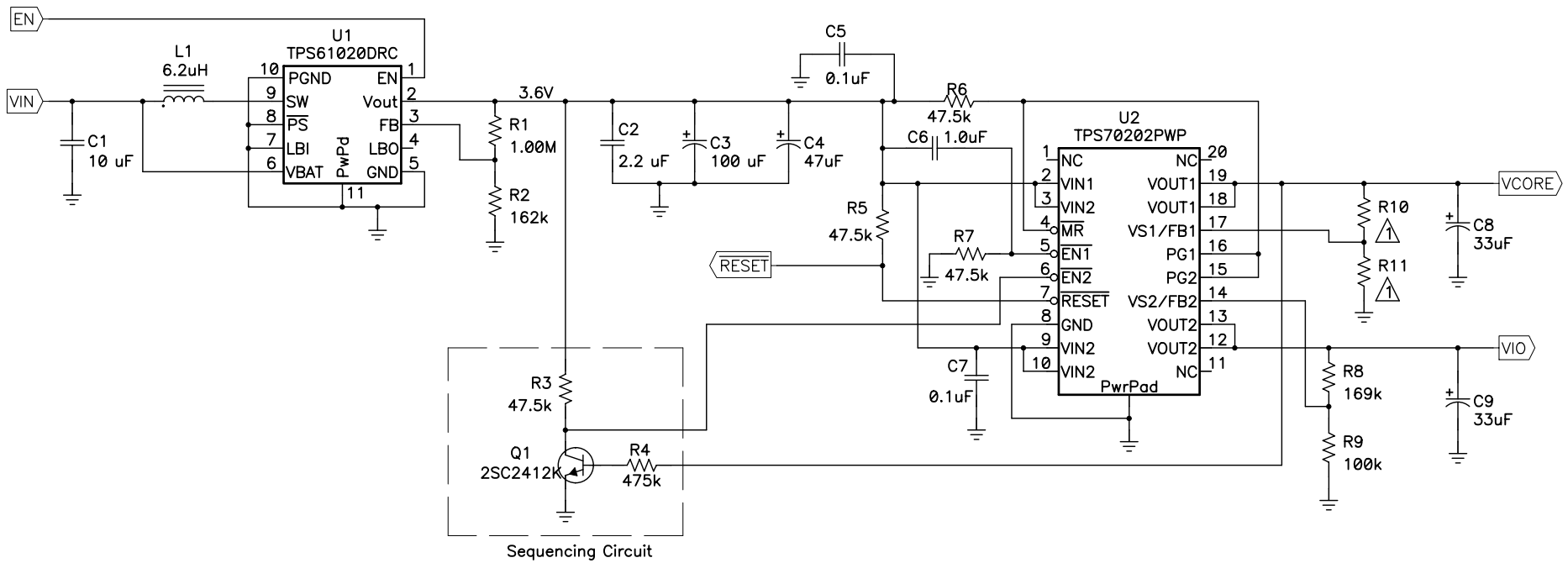
The solution was tested on the bench and in an actual DSP circuit. Bench testing included start up into full DSP load, switched load from no load to full DSP load, and power up sequencing. The full DSP load is defined as the current draw a C550x DSP would present to the power supply under worst operating conditions. This full DSP load current is heavily dependent on board layout, firmware configurations, DSP clock speed, and core voltage. For testing purposes, the following values were assumed to be the full DSP load current.

Voltage (V)	Function	Full load current (mA)
1.2	Core	110
1.6	Core	256
3.3	I/O	70

The solution was also tested in an active DSP board. The following test setup was used for this testing:


USB
Emulator
JTAG
C6550x EVM Board
(DSP, clock and glue
logic)
Input Voltage
Power Supply
1.2V or 1.5V
3.3V
Design Under
Test
Vcore
Vio
/RESET
Switched Load

Send an email to mailto:**dsppower@list.ti.com**



1

Voltage	R10	R11
1.2V	0	Open
1.6V	10.2k	33.2k

Title	C5000 DSP Attach Design 2 for 1.2 < Vin < 3.0V	
Size B	Number PR419	Rev
Date 02/14/05		Drawn by
Filename pr419.sch		Sheet of

Filename: PR419_bom.xls

Date: 02/14/2005

PR419 BOM

COUNT						
-001	-002	RefDes	DESCRIPTION	SIZE	Part Number	MFR
1	1	C1	Capacitor, Ceramic, 10-uF, 6.3-V, X5R, 10%	0805	GRM21BR60J106KE01	muRata
1	1	C2	Capacitor, Ceramic, 2.2-uF, 6.3-V, X5R, 10%	0805	GRM21BR60J225KC01B	muRata
1	1	C3	Capacitor, Tantalum, 100-uF, 10-V, 100-milliohm, 20%	7343(D)	TPSD107M010R100	AVX
1	1	C4	Capacitor, Tantalum, 47-uF, 16-V, 110-milliohm, 20%	6032 (C)	594D476X0016C2T	Vishay
2	2	C5, C7	Capacitor, Ceramic, 0.1-uF, 25-V, X7R, 10%	0603	GRM188R71E104KA01	muRata
1	1	C6	Capacitor, Ceramic, 1.0-uF, 10-V, X5R, 10%	0603	GRM188R61A105KA61	muRata
2	2	C8, C9	Capacitor, POSCAP, 33-uF, 8-V, 70-milliohm, 20%	6032 (C)	8TPC33M	Sanyo
1	1	L1	Inductor, SM Toroid, 6.2uH, 1.8-A, 43-milliohms	74480	CDRH5D28-6R2	Sumida
1	1	Q1	Transistor, NPN General Purpose, VCE 50V, VCB 60V, VEB 7V, IC 0.15A	SOT-23	2SC2412K	ROHM
1	1	R1	Resistor, Chip, 1.00M-Ohms, 1/16-W, 1%	0603	Std	Std
1	0	R10	Resistor, Chip, 0-Ohms, 1/16-W, 1%	0603	Std	Std
0	1		Resistor, Chip, 10.2k-Ohms, 1/16-W, 1%	0603	Std	Std
1	1	R2	Resistor, Chip, 162k-Ohms, 1/16-W, 1%	0603	Std	Std
4	4	R3, R5, R6, R7	Resistor, Chip, 47.5k-Ohms, 1/16-W, 1%	0603	Std	Std
1	1	R4	Resistor, Chip, 475k-Ohms, 1/16-W, 1%	0603	Std	Std
1	1	R8	Resistor, Chip, 169k-Ohms, 1/16-W, 1%	0603	Std	Std
1	1	R9	Resistor, Chip, 100k-Ohms, 1/16-W, 1%	0603	Std	Std
0	0	R11	Resistor, Chip, xx-Ohms, 1/16-W, 1%	0603		
0	1		Resistor, Chip, 33.2k-Ohms, 1/16-W, 1%	0603	Std	Std
1	1	U1	IC, Synchronous Boost Converter, Adj V	DRC10	TPS61020DRC	TI
1	1	U2	IC, Dual-output LDO Regulator w/SVS	PWP20	TPS70202PWP	TI

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