

PR421  
TMS320VC550x Design 4

**FEATURES:**

- Provides sequenced core and I/O voltages from input voltages from 2.4 V to 3.0 V.
- /RESET delay fixed at 65 ms minimum, 130ms typical.
- All switching regulators for high efficiency operation.
- Suitable for two cell operation
- The current draw on the input power supply is minimized by sequencing the core rail first and then the I/O rail.

**IMPORTANT WEB LINKS:**

- Link to the TI power management home page at <http://power.ti.com> then select the TI DSP Solutions link for more information and other reference designs.
- Link to datasheets at:
  - o <http://focus.ti.com/lit/ds/symlink/tps62000.pdf>
  - o <http://focus.ti.com/lit/ds/symlink/tps61020.pdf>
  - o <http://focus.ti.com/lit/ds/symlink/tps3103k33.pdf>

**THEORY OF OPERATION:**

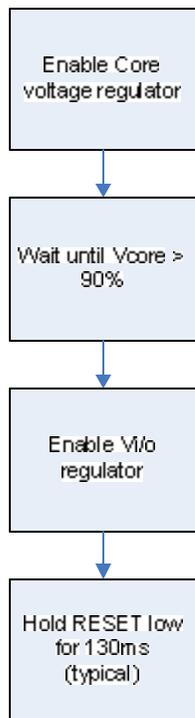
PR421 consists of a TPS61020 boost converter for the I/O voltage and a TPS62000 buck regulator for the core voltage. The TPS61020 boosts the input voltage to a regulated 3.3 Volts for the I/O voltage. The TPS2000 buck regulator regulates the input voltage down to the core voltage.

**CIRCUIT LIMITATIONS AND CAPABILITIES:**

The TPS61020 is capable of supplying about 600 mA of I/O current with an input voltage of 2.0 V. See Figure 1 of the TPS61020 datasheet for the current capability at other input voltages. Higher input voltages allow for higher output current from the TPS61020. The TPS62000 is capable of supplying 600 mA of core current.

Though not preferred, the TPS61020 is also capable of regulating from input voltages higher than the output voltage. TPS61020 will start to operate like a linear regulator once the input voltage is higher than 3.3 V. Therefore, the TPS61020 will still produce a regulated 3.3 V for I/O voltage with up to 5.5 V on the input. Since the TPS61020 is a linear regulator at higher input voltages, its efficiency will decrease substantially and its power dissipation will increase significantly. Close attention should be paid to the thermal performance of the TPS61020 operating in this condition.

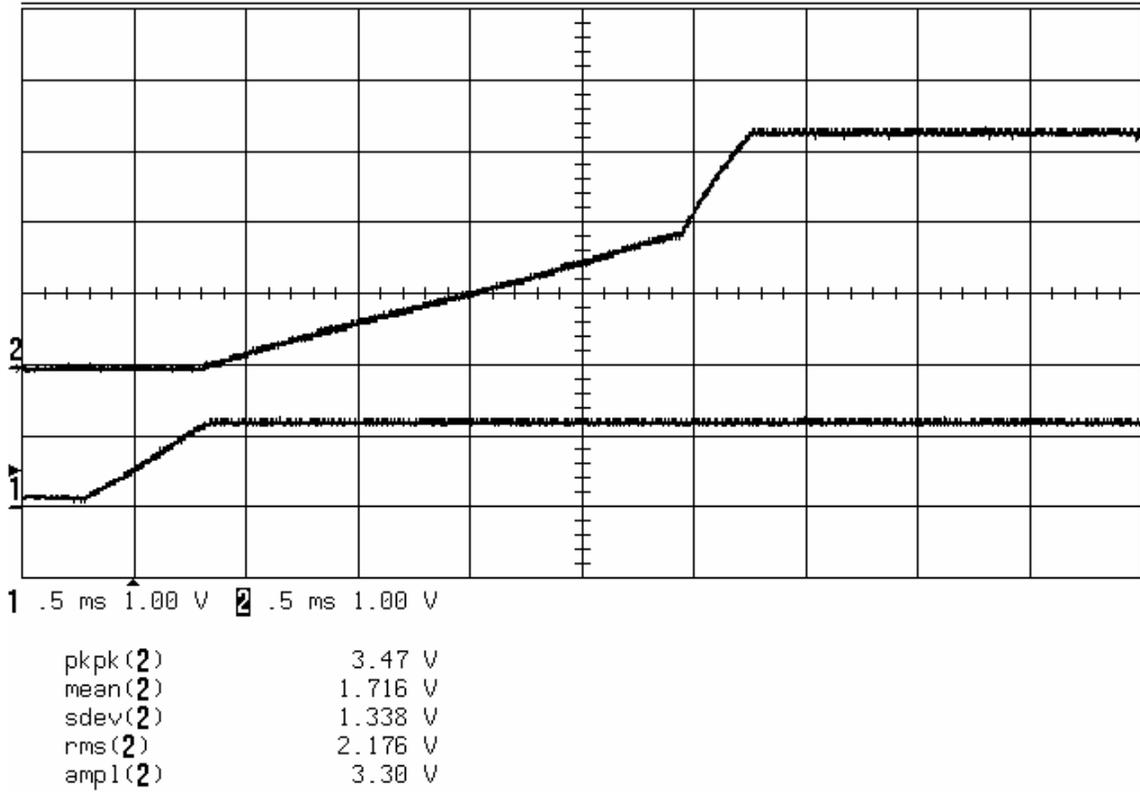
**POWER UP SEQUENCING:**



The circuit will start to ramp up the I/O voltage immediately after the core voltage is above 90% of its nominal value. Some systems may require a longer time delay between the core and I/O voltage applications. A capacitor can be added between pin 4 of U1 and ground to slow the turn on of the I/O voltage. The turn on time would be delayed by the RC time constant created by R1 and the added capacitor.

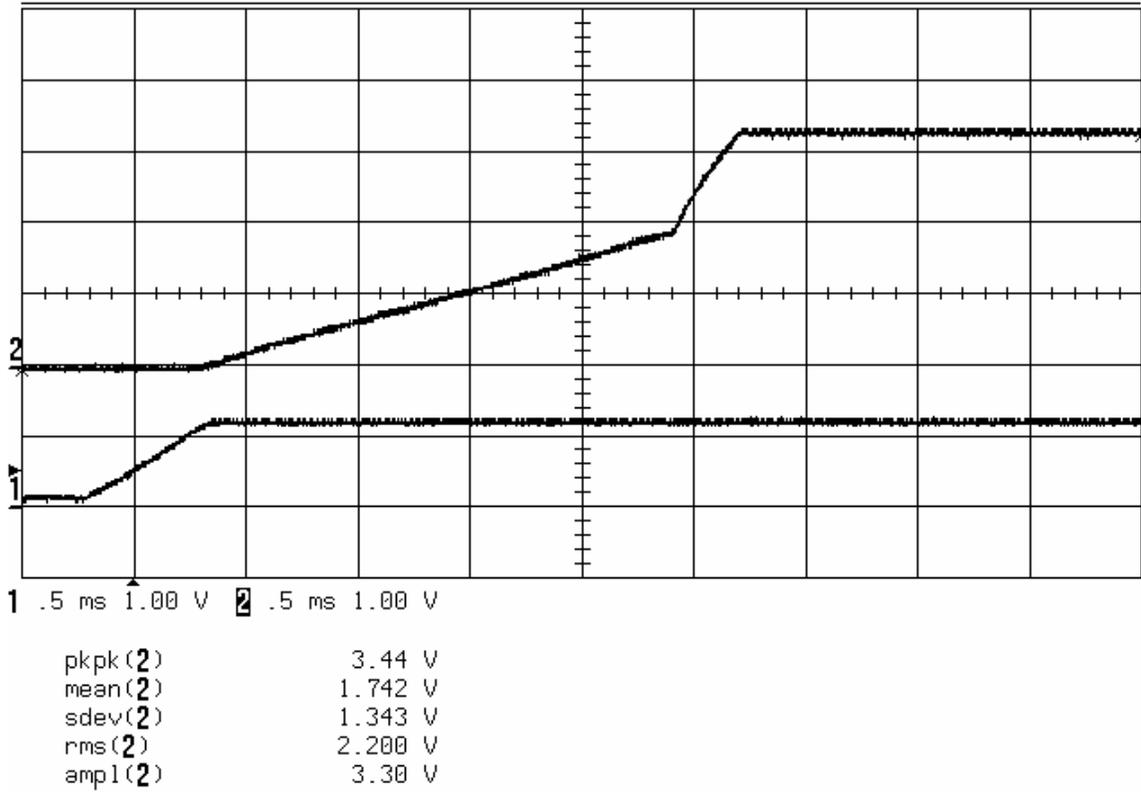
The sequencing circuits can be removed if sequencing is not required. Components R1 and D1 can be removed and the enable pins of both regulators tied together. This will not effect the minimum duration of the RESET signal.

#### **WAVEFORMS:**



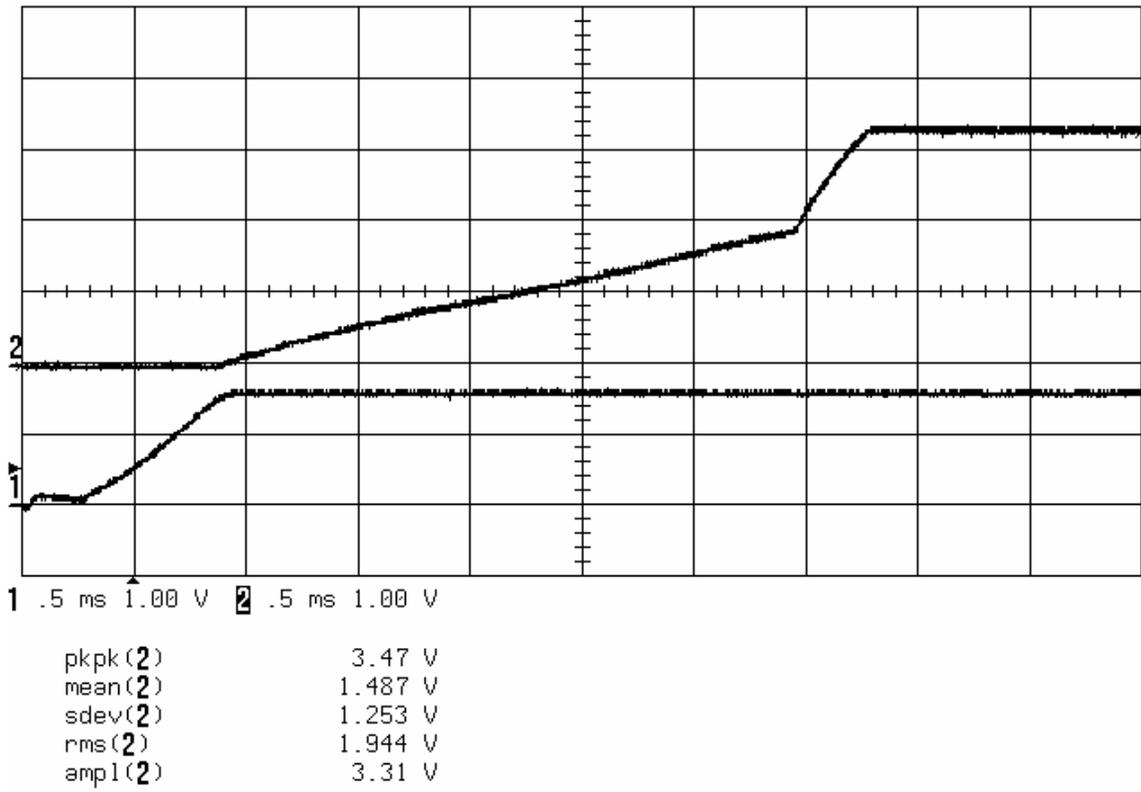
□ NORMAL

Figure 1 - Power up with  $V_{IN} = 2.0\text{ V}$ ,  $V_{core} = 1.2\text{ V}$  @  $110\text{ mA}$ ,  $V_{i/o} = 3.3\text{ V}$  @  $50\text{ mA}$



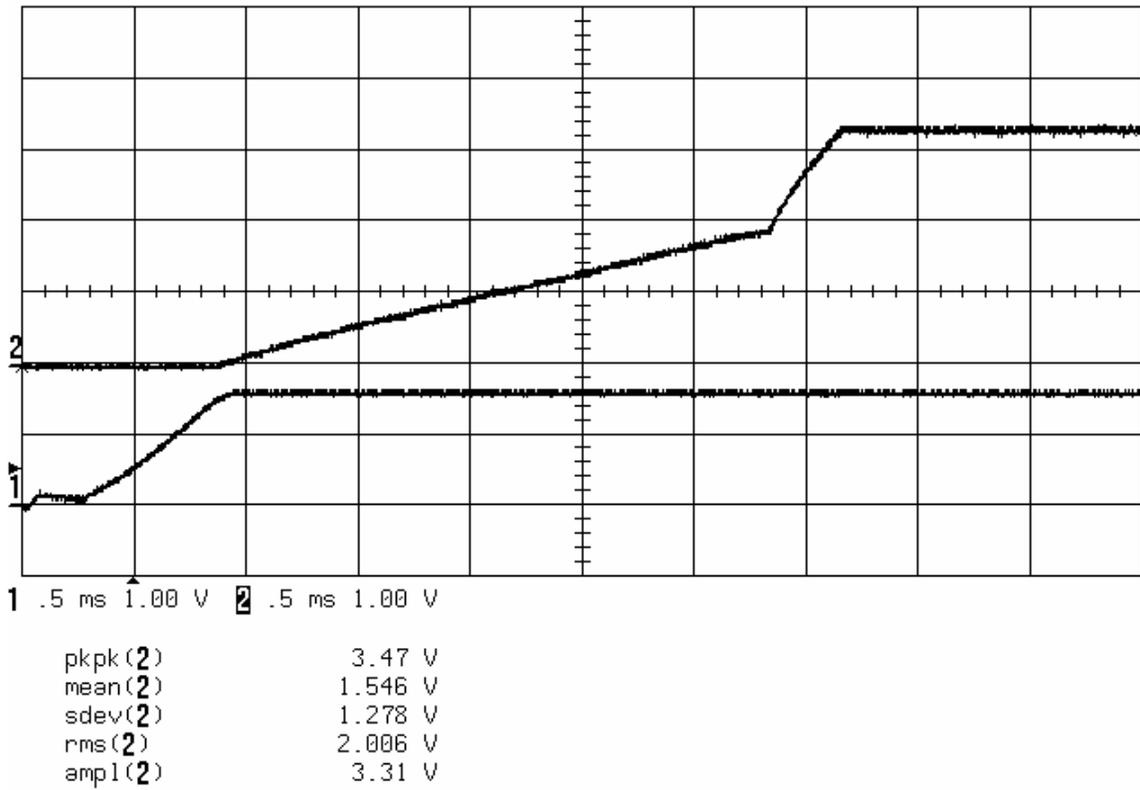
□ NORMAL

Figure 2 - Power up from Enable when  $V_{IN} = 2.0$  V,  $V_{core} = 1.2$  V @ 110 mA,  $V_{i/o} = 3.3$  V @ 50 mA



□ NORMAL

Figure 3 - Power up with  $V_{IN} = 2.0$  V,  $V_{core} = 1.6$  V @ 250 mA,  $V_{i/o} = 3.3$  V @ 70 mA



□ NORMAL

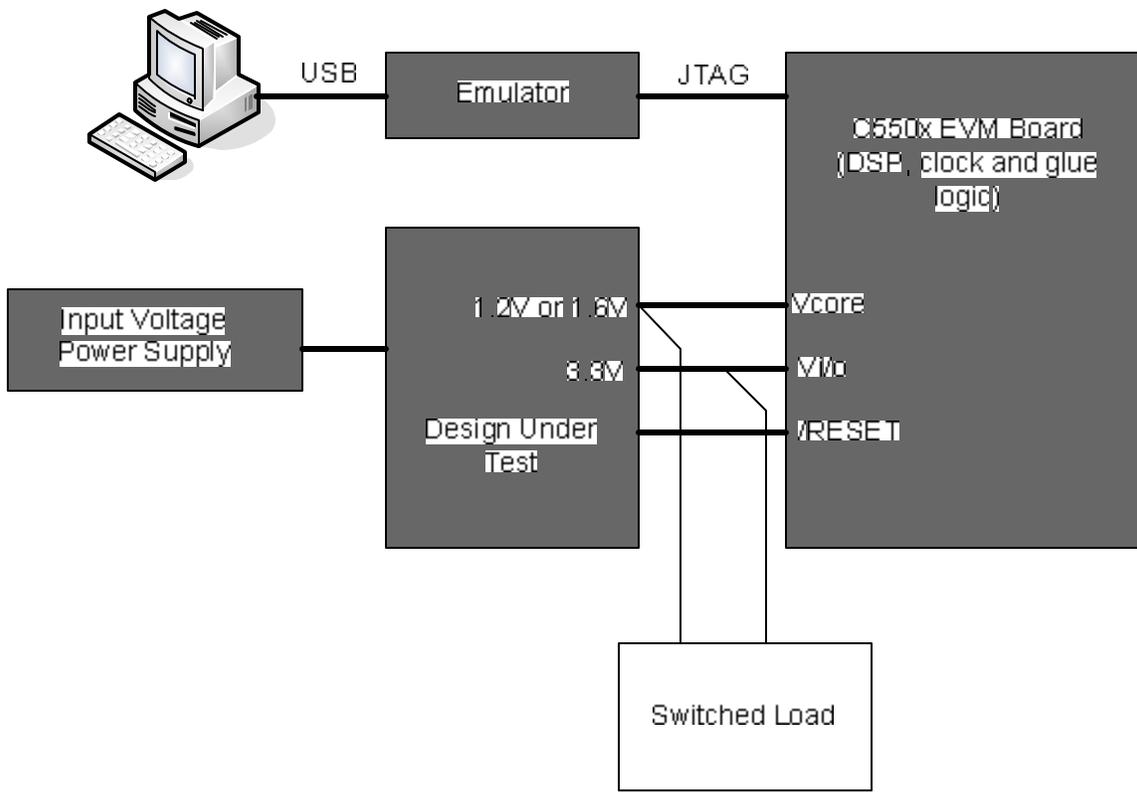
Figure 4 - Power up from Enable when  $V_{IN} = 2.0$  V,  $V_{core} = 1.6$  V @ 250 mA,  $V_{i/o} = 3.3$  V @ 70 mA

### TESTING METHOD:

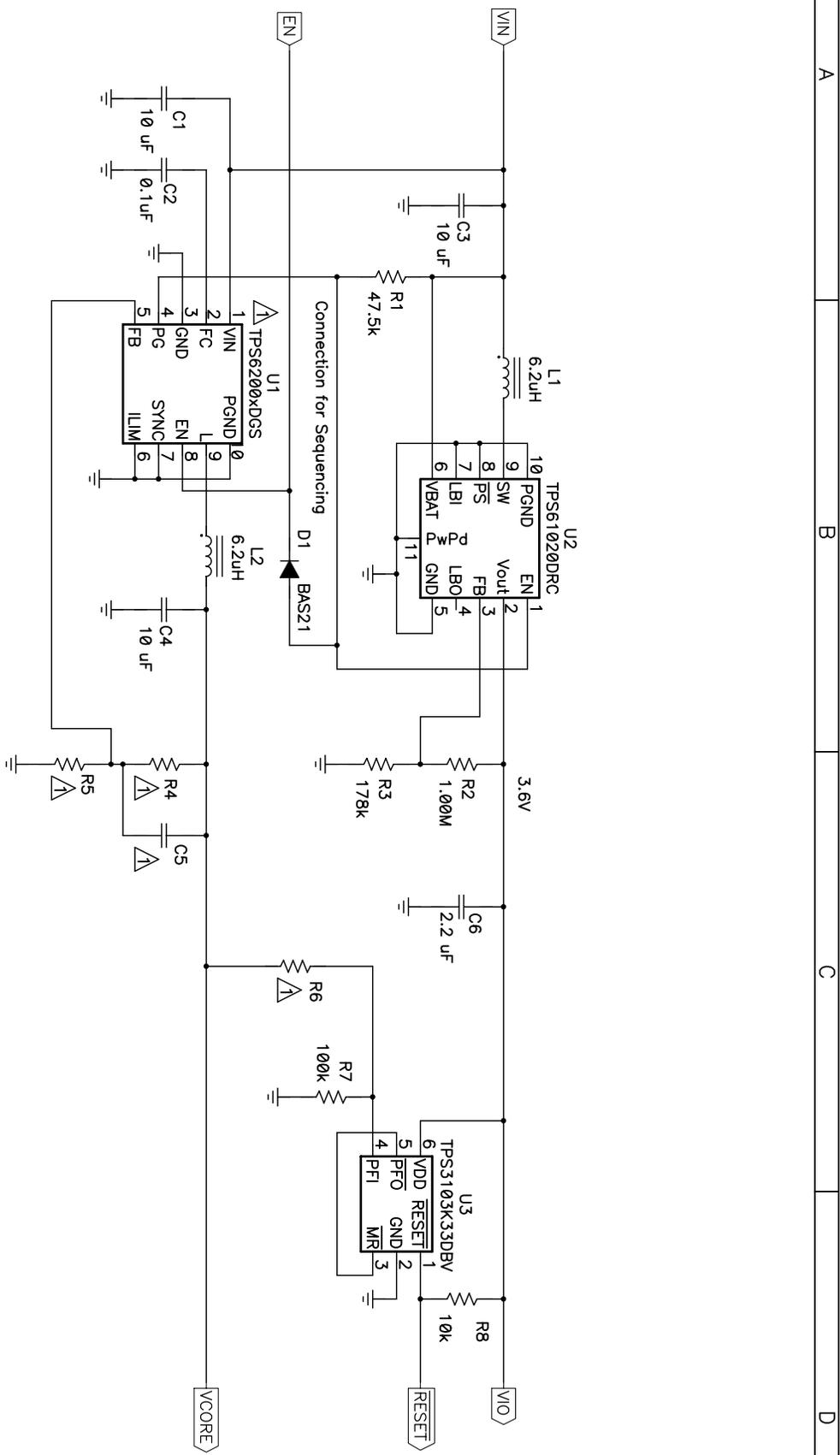
The solution was tested on the bench and in an actual DSP circuit. Bench testing included start up into full DSP load, switched load from no load to full DSP load, and power up sequencing. The full DSP load is defined as the current draw a C550x DSP would present to the power supply under worst operating conditions. This full DSP load current is heavily dependent on board layout, firmware configurations, DSP clock speed, and core voltage. For testing purposes, the following values were assumed to be the full DSP load current.

Voltage (V)	Function	Full load current (mA)
1.2	core	110
1.6	core	256
3.3	I/O	70

The solution was also tested in an active DSP board. The following test setup was used for this testing:



Send an email to <mailto:dsppower@list.ti.com>



Voltage	U1	R4	R5	R6	C5
1.2V	TPS622003	0	Open	97.6k	Open
1.6V	TPS622000	549k	215k	162k	10pF

Title		C5000 DSP Attach Design 4	
Size		for 2.4 < Vin < 3.0V	
B	Number	PR421	Rev
Date	01/05/05	Drawn by	
Filename	pr421.sch	Sheet	of

Filename: PR421_bom.xls						
Date: 01/06/2005						
<b>PR421 BOM</b>						
<b>COUNT</b>						
<b>-001</b>	<b>-002</b>	<b>RefDes</b>	<b>DESCRIPTION</b>	<b>SIZE</b>	<b>Part Number</b>	<b>MFR</b>
1	1	C2	Capacitor, Ceramic, 0.1-uF, 25-V, X7R, 10%	0603	GRM188R71E104KA01	muRata
0	0	C5	Capacitor, Ceramic, xxx-uF, vv-V	0603		
0	1		Capacitor, Ceramic, 10-pF, 50-V, C0G, 5%	0603	GRM1885C1H100JZ01	muRata
1	1	C6	Capacitor, Ceramic, 2.2-uF, 6.3-V, X5R, 10%	0805	GRM21BR60J225KC01B	muRata
1	1	D1	Diode, Switching, 200-mA, 200-V, 330-mW	SOT23	BAS21	Zetex
2	2	L1, L2	Inductor, SM Toroid, 6.2uH, 1.8-A, 43-milliohms	74480	CDRH5D28-6R2	Sumida
1	1	R1	Resistor, Chip, 47.5k-Ohms, 1/16-W, 1%	0603	Std	Std
1	1	R2	Resistor, Chip, 1.00M-Ohms, 1/16-W, 1%	0603	Std	Std
1	1	R3	Resistor, Chip, 178k-Ohms, 1/16-W, 1%	0603	Std	Std
1	0	R4	Resistor, Chip, 0-Ohms, 1/16-W, 1%	0603	Std	Std
0	1		Resistor, Chip, 549k-Ohms, 1/16-W, 1%	0603	Std	Std
0	0	R5	Resistor, Chip, xx-Ohms, 1/16-W, 1%	0603		
0	1		Resistor, Chip, 215k-Ohms, 1/16-W, 1%	0603	Std	Std
1		R6	Resistor, Chip, 97.6k-Ohms, 1/16-W, 1%	0603	Std	Std
	1		Resistor, Chip, 162k-Ohms, 1/16-W, 1%	0603	Std	Std
1	1	R7	Resistor, Chip, 100k-Ohms, 1/16-W, 1%	0603	Std	Std
1	1	R8	Resistor, Chip, 10k-Ohms, 1/16-W, 1%	0603	Std	Std
1		U1	IC, High-Efficiency Step-Down Converter, 1.2-V	DGS10	TPS62003DGS	TI
	1		IC, High-Efficiency Step-Down Converter, Adj-V	DGS10	TPS62000DGS	TI
1	1	U2	IC, Synchronous Boost Converter, Adj V	DRC10	TPS61020DRC	TI
1	1	U3	IC, Ultra Low Current/Supply, Voltage Supervisor	SOT23-6	TPS3103K33DBV	TI

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Mailing Address: Texas Instruments  
Post Office Box 655303 Dallas, Texas 75265