

PR425
TMS320VC550x Design 8

FEATURES:

- Provides sequenced core and I/O voltages from an input source between 3.6 and 5.0 V.
- /RESET delay fixed at 65 ms minimum, 130 ms typical.
- All switching regulators for high efficiency operation.
- Small solution size.

IMPORTANT WEB LINKS:

- Link to the TI power management home page at <http://power.ti.com> then select the TI DSP Solutions link for more information and other reference designs.
- Link to datasheets at:
 - o <http://focus.ti.com/lit/ds/symlink/tps62300.pdf>
 - o <http://focus.ti.com/lit/ds/symlink/tps3103k33.pdf>

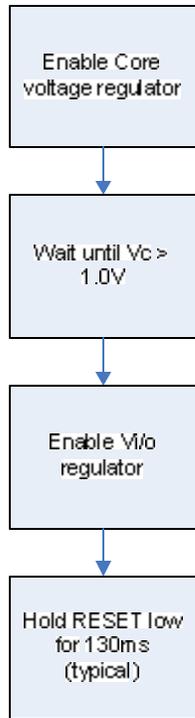
THEORY OF OPERATION:

PR425 consists of two TPS62300 buck regulators to regulate the core and I/O voltages.

CIRCUIT LIMITATIONS AND CAPABILITIES:

Each TPS62300 is capable of supplying 500 mA of current.

POWER UP SEQUENCING:

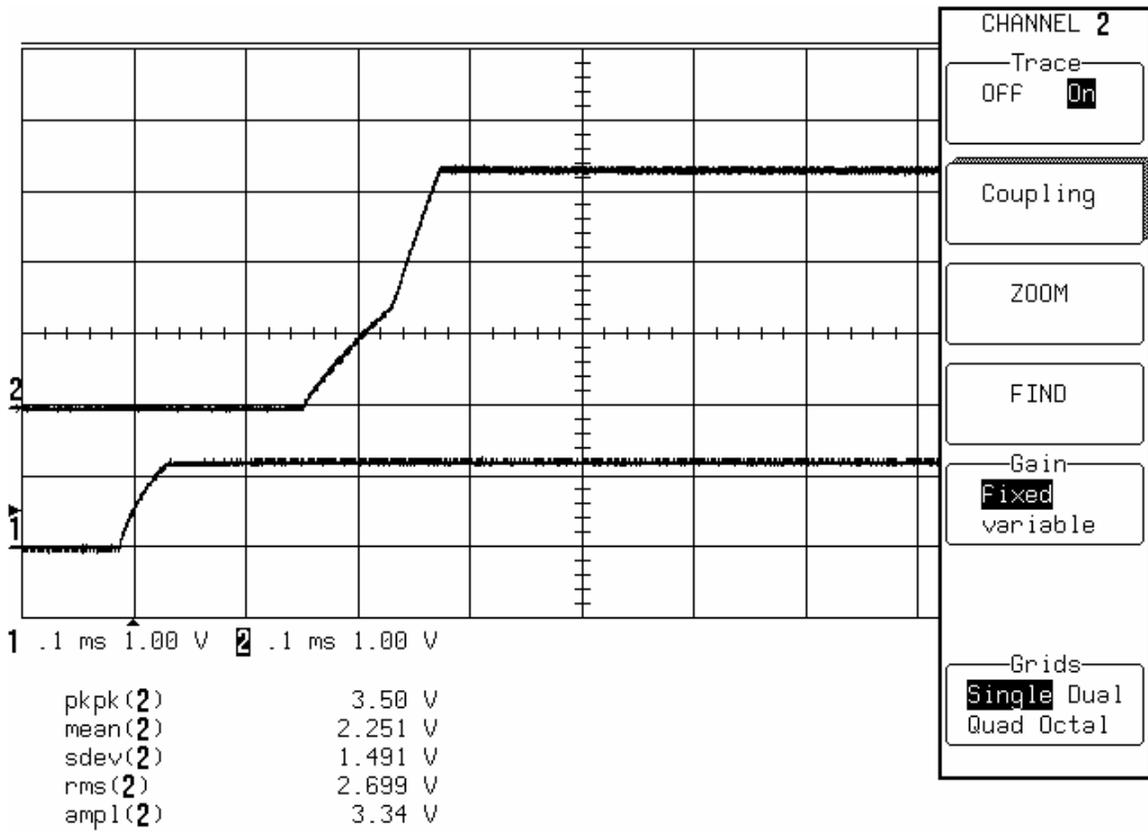


The circuit will start to ramp up the I/O voltage immediately after the core voltage is above about 1.0V. This 1.0V threshold will vary with the characteristics of the transistors being used in the sequencing circuit. Some systems may require a longer time delay between the core and I/O voltage applications. A capacitor can be added between the base of Q2 and ground to slow the turn on of the I/O voltage. The turn on time is delayed by the RC time constant created by R5 and the added capacitor.

The sequencing circuits can be removed if sequencing is not required. Components R3, R4, R5, Q1 and Q2 can all be removed and the two enables tied together. This will not effect the minimum duration of the RESET signal.

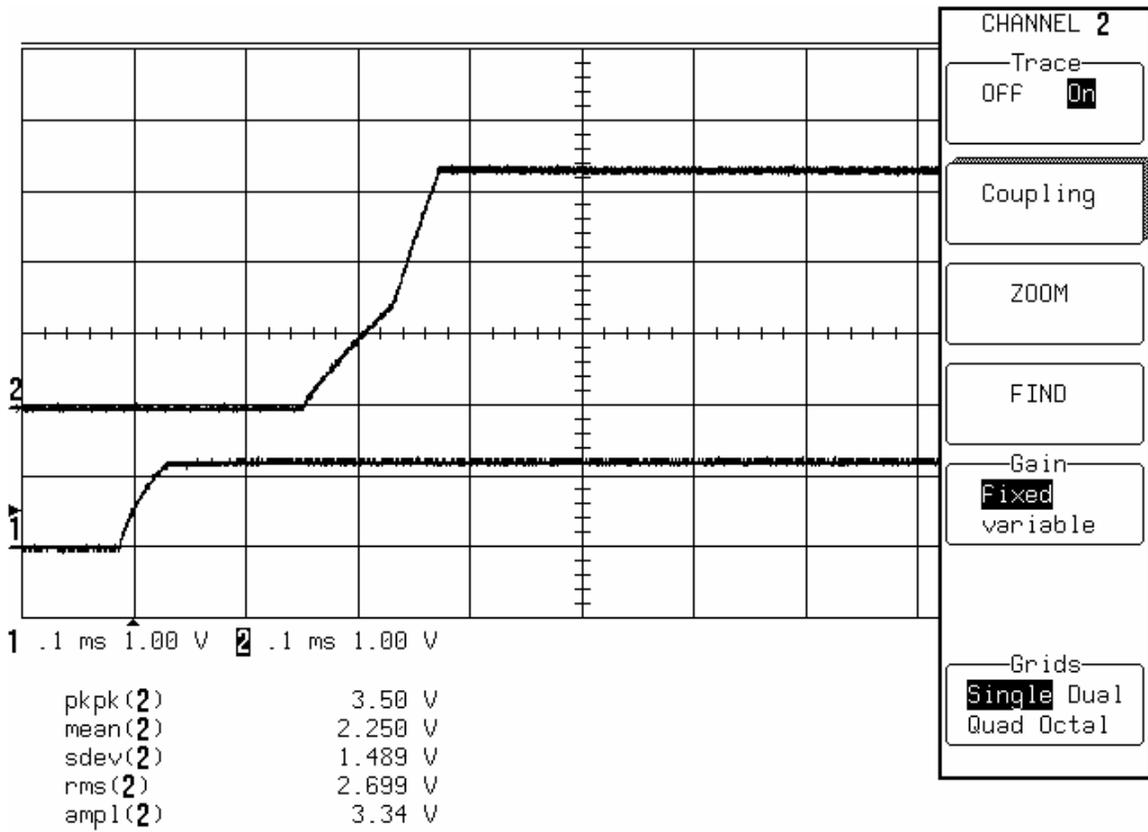
The minimum logic high voltage for U2, the I/O converter, is 1.2 V. For 1.2 V core systems, the nominal output voltage of the core converter is 1.2V. Components R3, R4, R5, Q1 and Q2 provide voltage level translation from 1.2 V to the input voltage level so that U2 is reliably turned on in 1.2 V systems. This circuit is not required for 1.6 V systems so R3, R4, R5, Q1 and Q2 can be removed and the core voltage tied directly to the enable of U2. This will slightly alter the voltage ramp up of the core and I/O rails.

WAVEFORMS:



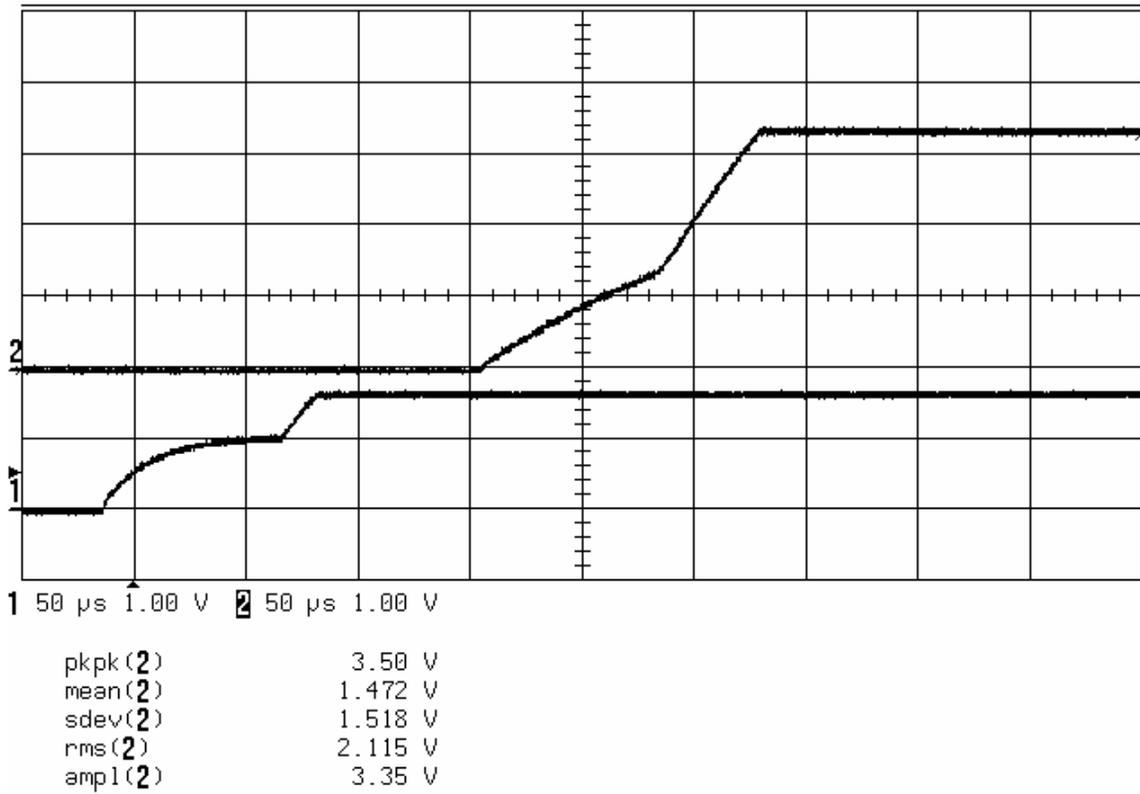
□ NORMAL

Figure 1 - Power up with $V_{IN} = 3.6\text{ V}$, $V_{core} = 1.6\text{ V}$ @ 250 mA, $V_{i/o} = 3.3\text{ V}$ @ 70 mA



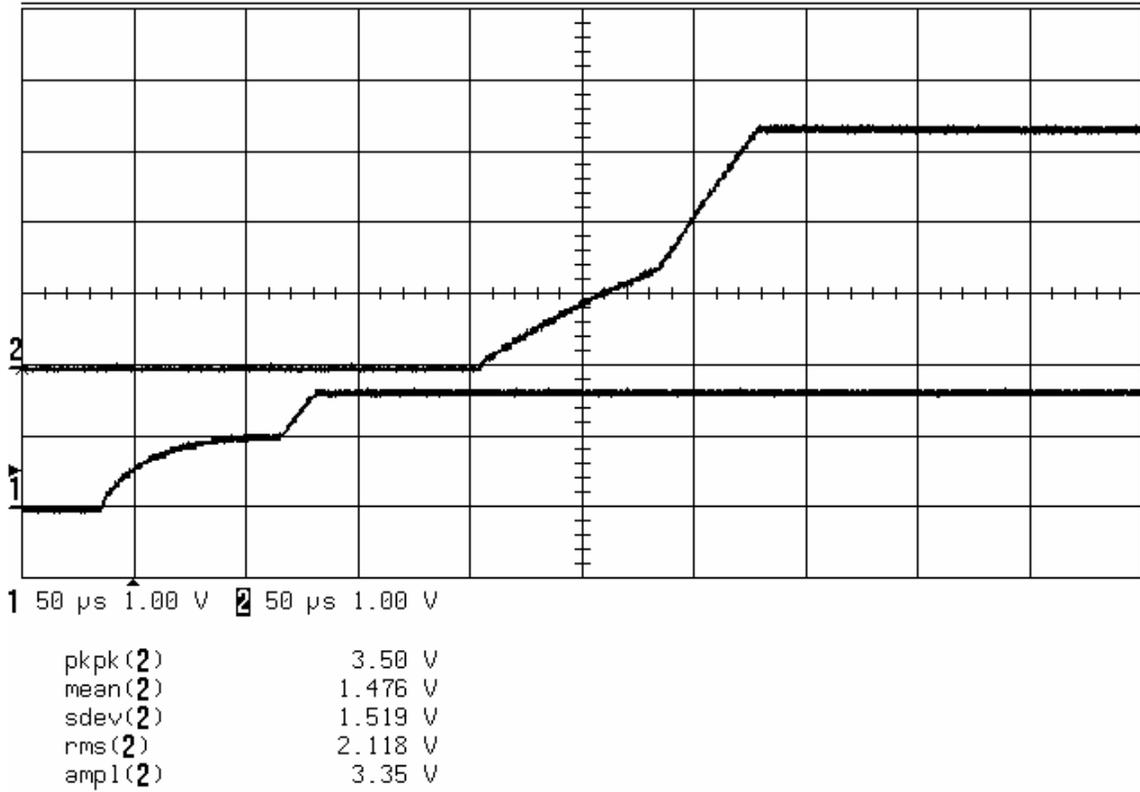
NORMAL

Figure 2 - Power up from Enable when $V_{IN} = 3.6\text{ V}$, $V_{core} = 1.6\text{ V}$ @ 250 mA, $V_{i/o} = 3.3\text{ V}$ @ 70 mA



□ NORMAL

Figure 3 - Power up with $V_{IN} = 3.6$ V, $V_{core} = 1.6$ V @ 250 mA, $V_{i/o} = 3.3$ V @ 70 mA, no sequencing circuit, V_{core} tied to enable of U2



□ NORMAL

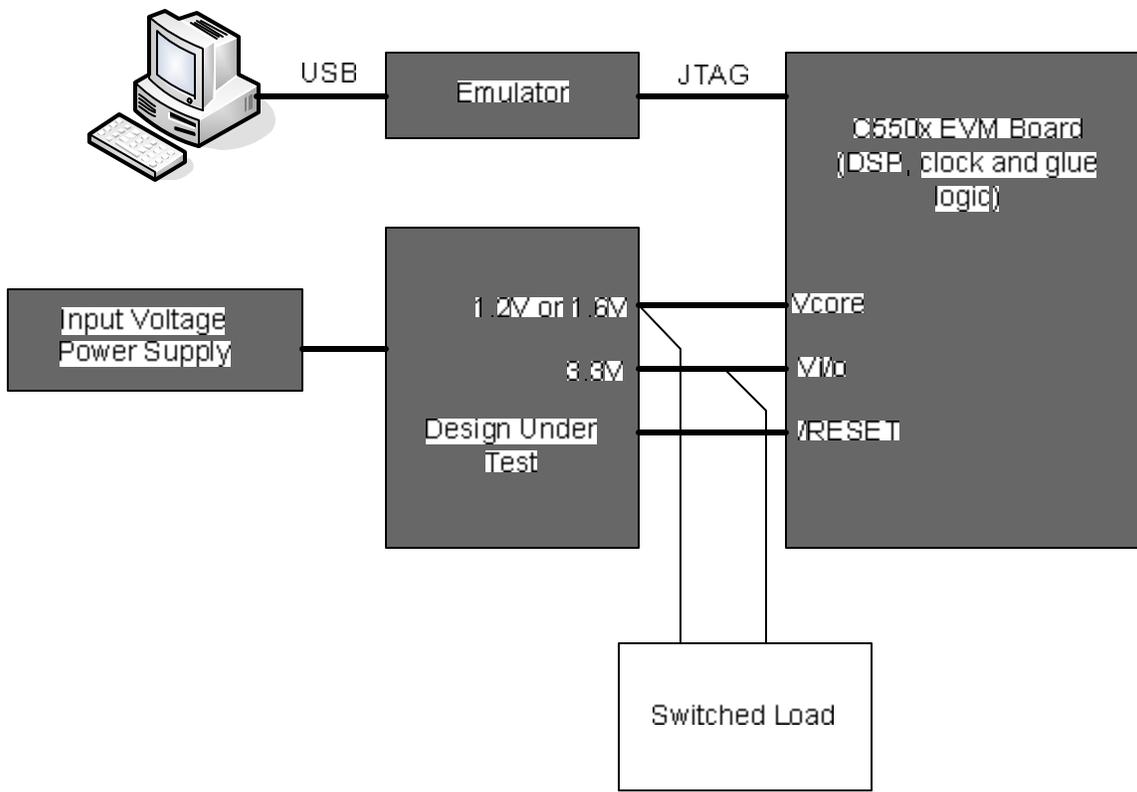
Figure 4 - Power up from Enable when $V_{IN} = 3.6\text{ V}$, $V_{core} = 1.6\text{ V}$ @ 250 mA, $V_{i/o} = 3.3\text{ V}$ @ 70 mA, no sequencing circuit, V_{core} tied to enable of U2

TESTING METHOD:

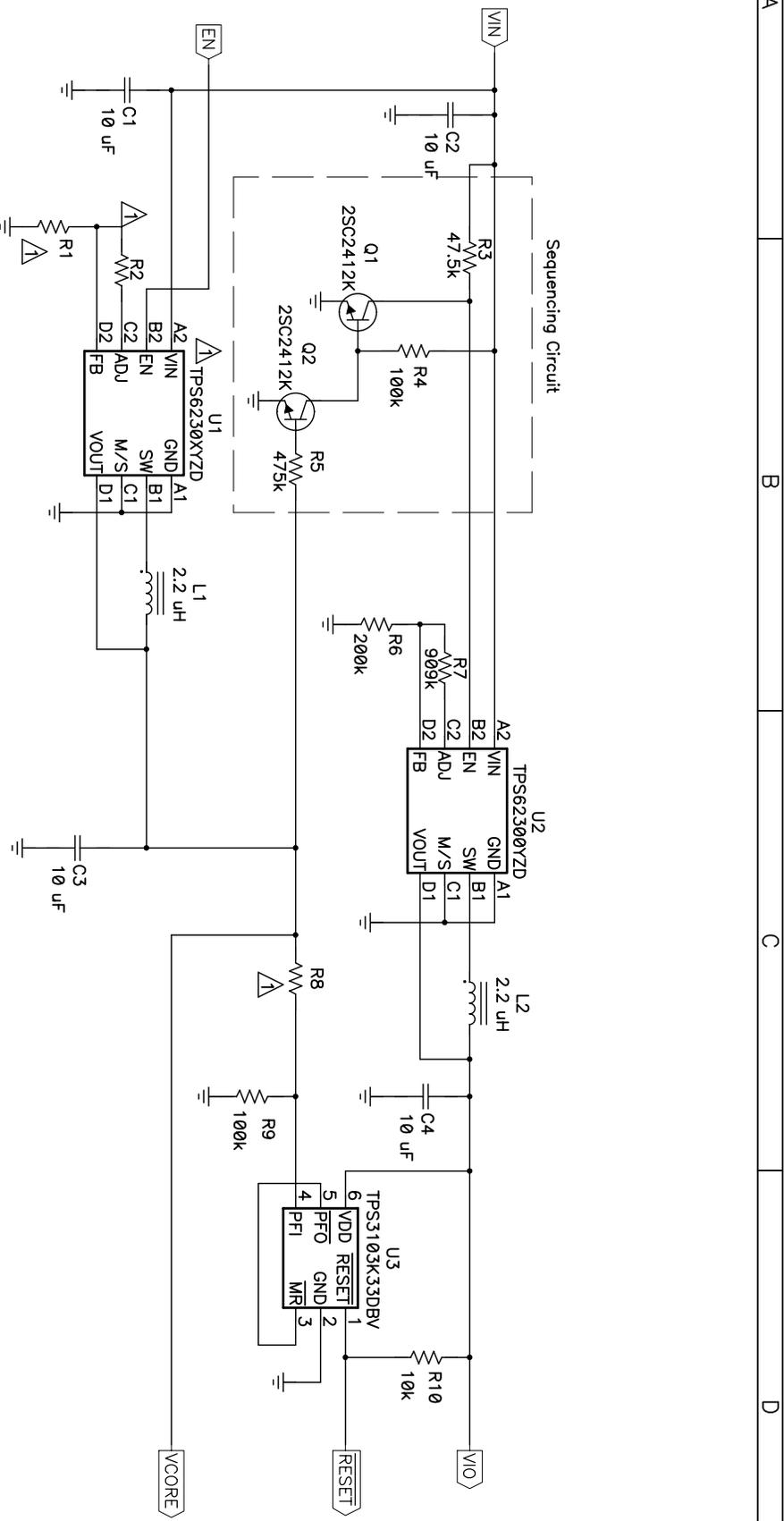
The solution was tested on the bench and in an actual DSP circuit. Bench testing included start up into full DSP load, switched load from no load to full DSP load, and power up sequencing. The full DSP load is defined as the current draw a C550x DSP would present to the power supply under worst operating conditions. This full DSP load current is heavily dependent on board layout, firmware configurations, DSP clock speed, and core voltage. For testing purposes, the following values were assumed to be the full DSP load current.

Voltage (V)	Function	Full load current (mA)
1.2	Core	110
1.6	Core	256
3.3	I/O	70

The solution was also tested in an active DSP board. The following test setup was used for this testing:



Send an email to <mailto:dsppower@list.ti.com>



Part	Value	Part	Value	Part	Value
U1	TPS62300	R1	332k	R2	332k
R1	332k	R2	332k	R8	97.6k
R2	332k	Open	Open	Open	162k
Open	Open	Open	Open	Open	Open

Title		C5000 DSP Attach Design 8	
Size		for 3.6 < Vin < 5.0V	
Number	PR425	Rev	
Date	02/14/05	Drawn by	
Filename	pr425.sch	Sheet	of

Filename: PR425_bom.xls						
Date: 02/14/2005						
PR425 BOM						
COUNT						
-001	-002	RefDes	Description	Size	Part Number	MFR
4	4	C1, C2, C3, C4	Capacitor, Ceramic, 10-uF, 6.3-V, X5R, 10%	0805	GRM21BR60J106KE01	muRata
2	2	L1, L2	Inductor, SMT, 2.2-uH, 770-mA, 230-milliohms	0805	CB2016T2R2M	Taiyo Yuden
2	2	Q1, Q2	Transistor, NPN General Purpose, VCE 50V, VCB 60V, VEB 7V, IC 0.15A	SOT-23	2SC2412K	ROHM
1	0	R1	Resistor, Chip, 332k-Ohms, 1/16-W, 1%	0603	Std	Std
0	0		Resistor, Chip, xx-Ohms, 1/16-W, 1%	0603		
1	0	R2	Resistor, Chip, 332k-Ohms, 1/16-W, 1%	0603	Std	Std
0	0		Resistor, Chip, xx-Ohms, 1/16-W, 1%	0603		
1	1	R3	Resistor, Chip, 47.5k-Ohms, 1/16-W, 1%	0603	Std	Std
2	2	R4	Resistor, Chip, 100k-Ohms, 1/16-W, 1%	0603	Std	Std
1	1	R5	Resistor, Chip, 475k-Ohms, 1/16-W, 1%	0603	Std	Std
1	1	R6	Resistor, Chip, 200k-Ohms, 1/16-W, 1%	0603	Std	Std
1	1	R7	Resistor, Chip, 909k-Ohms, 1/16-W, 1%	0603	Std	Std
1	0	R8	Resistor, Chip, 97.6k-Ohms, 1/16-W, 1%	0603	Std	Std
0	1		Resistor, Chip, 162k-Ohms, 1/16-W, 1%	0603	Std	Std
1	1	R9	Resistor, Chip, 100k-Ohms, 1/16-W, 1%	0603	Std	Std
1	1	R10	Resistor, Chip, 10k-Ohms, 1/16-W, 1%	0603	Std	Std
1	0	U1	IC, 3MHz Synchronous Step-Down Converter, 400mA	CSP-8	TPS62300YDZ	TI
0	1		IC, 3MHz Synchronous Step-Down Converter, 400mA	CSP-8	TPS62302YDZ	TI
1	1	U2	IC, 3MHz Synchronous Step-Down Converter, 400mA	CSP-8	TPS62300YDZ	TI
1	1	U3	IC, Ultra Low Current/Supply, Voltage Supervisor	SOT23-6	TPS3103K33DBV	TI

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