

PR434
Virtex™-4 Design 2
SWIFT™ (TPS54x10 series) DC/DC Converter-based Power Management Solution
Providing up to 6A from $V_{IN}=5V$

FEATURES:

- Used on the ML401 evaluation board available at www.xilinx.com
- High efficiency converters minimize heat
- Interchange SWIFT™ device to support 1.5 A to 14 A load currents
 - o 1.5A and 3A SWIFT devices are pin-pin compatible
 - o 6A, 8A, 9A and 14 A SWIFT devices are pin-pin compatible
- Use of the TPS54x10 adjustable devices allow
 - o use of smallest inductor and/or specific type of output capacitor
 - o flexibility to re-compensate as needed, depending on the bypass/decoupling capacitors used with the FPGA
- TPS51100 used for DDR-I termination voltage
- Additional V_{CCO} rails easily added and sequenced (if desired) using the TPS54xxx PWRGD and ENABLE.

IMPORTANT WEB LINKS:

- Link to the TI home page for Xilinx FPGA power management solutions at <http://www.ti.com/xilinuxfpga> for more information and other reference designs.
- Link to datasheets at <http://focus.ti.com/lit/ds/symlink/TPS54610.pdf> and <http://focus.ti.com/lit/ds/symlink/tps51100.pdf>.
- Link to SWIFT™ design software tool at <http://focus.ti.com/docs/toolsw/folders/print/swift-sw.html> to assist further optimization/customization of design.

IMPLEMENTATION NOTES:

- **Sequencing:** Per Xilinx DS302 v1.3, Virtex-4 power rails can be turned on in any sequence, though V_{CCAUX} must power on before or with V_{CCO} for the minimum power-on current specifications shown in the Xilinx datasheet to apply. For this reason and to reduce the risk that large currents for charging bulk capacitance forces the point of load converter into current limit and/or pulls down the input supply at power up, the following recommended design techniques were used:
 - o Integrated soft-start configured with a capacitor to provide 1.5 ms monotonic rise time for V_{CCINT} , V_{CCAUX} and V_{CCO}
 - o Sequencing V_{CCINT} , V_{CCAUX} then V_{CCO} using PWRGD and ENABLE

- **Additional Capacitance:**

The TPS54x10 devices have been compensated and soft-started to allow for the following amount of additional bulk and decoupling capacitance on each output rail.

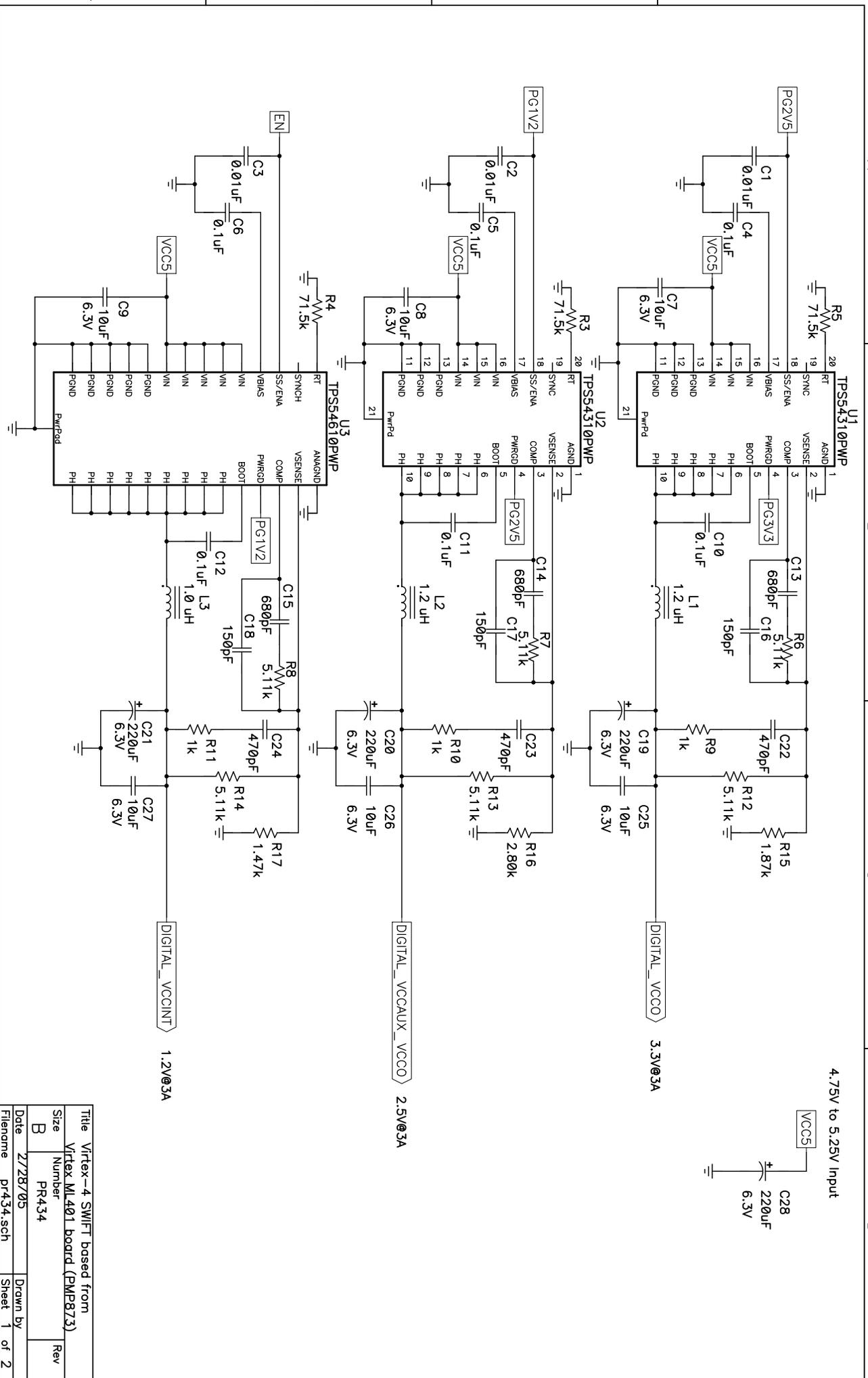
Capacitor (uF)	V _{CCINT} QTY	V _{CCAUX} QTY	V _{CCO} QTY
0.047	18	18	14
0.22	8	9	7
0.68	4	4	3
2.2	3	3	2
330 Low ESR	1	2	1

If the amount of bulk capacitance increases, the TPS54x10 control loop may need to be re-compensated and/or the soft-start timing may need change. The SWIFT design software can help with these design changes.

- **V_{CCAUX} :** V_{CCAUX} powers time-critical resources in the FPGA, including the Digital Clock Managers (DCMs). Therefore, this supply voltage is especially susceptible to power supply noise. V_{CCAUX} can share a power plane with V_{CCO}, but only if V_{CCO} does not have excessive noise. Changes in V_{CCAUX} voltage should take place no faster than 10 mV/ms.
- **Modifications**
 - o For V_{IN} = 3.3 V
 - U1 may be eliminated
 - U2 and U3 may require re-compensation of the control loop using the SWIFT design software.
 - o When interchanging SWIFT™ devices with different maximum load currents, use the SWIFT software for device selection and control loop compensation.

QUESTIONS?

- Send an email to <mailto:fpgasupport@list.ti.com>



4.75V to 5.25V Input

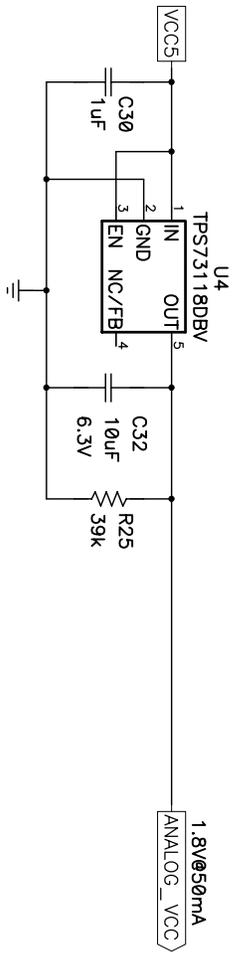
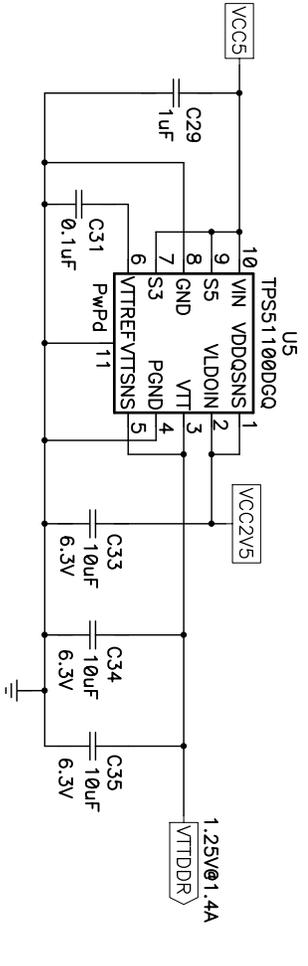
C28
220uF
6.3V

DIGITAL_VCCO 3.3V@3A

DIGITAL_VCCAUX_VCCO 2.5V@3A

DIGITAL_VCCINT 1.2V@3A

Title	Virtex-4 SWIFT based from		
Size	Virtex ML401 board (PMP873)		
Number	PR434	Rev	
Date	2/28/05	Drawn by	
Filename	pr434.sch	Sheet	1 of 2



Additional Caps

VALUE	DIGITAL_VCC0 QTY	DIGITAL_VCCAUX_VCC0 QTY	VCCINT QTY
0.047uF	14	18	18
0.22uF	7	9	8
0.68uF	3	4	4
2.2uF	2	3	3
330uF	1	2	1

Title	Virtex-4 SWIFT based from		
Size	Virtex ML401 board (PMP873)		
Number	PR434	Rev	
Date	2/28/05	Drawn by	
Filename	pr434.sch	Sheet	2 of 2

Filename: PR434_bom.xls					
Date: 02/22/2005					
PR434 BOM					
COUNT	RefDes	Description	Size	Part Number	MFR
3	C1, C2, C3	Capacitor, Ceramic, 0.01uF, 16V, X7R, 10%	0603	Std	Std
3	C13, C14, C15	Capacitor, Ceramic, 680pF, 50V, X7R, 10%	0603	Std	Std
3	C16, C17, C18	Capacitor, Ceramic, 150pF, 50V, X7R, 10%	0603	Std	Std
4	C19, C20, C21, C28	Capacitor, Tantalum, 220-uF, 6.3-V	0.268 x 0.307	ECS-T0JD227R	Panasonic
3	C22, C23, C24	Capacitor, Ceramic, 470pF, 16V, X7R, 10%	0603	Std	Std
2	C29, C30	Capacitor, Ceramic, 1uF, 16V, X7R, 10%	0603	Std	Std
7	C4, C5, C6, C10, C11, C12, C31	Capacitor, Ceramic, 0.1uF, 16V, X7R, 10%	0603	Std	Std
10	C7, C8, C9, C25, C26, C27, C32, C33, C34, C35	Capacitor, Ceramic, 10uF, 6.3V, X5R, 10%	0805	Std	Std
2	L1, L2	Inductor, SMT, 1.2-uH, 4.4-A, 17-milliohm		DO1813P-122HC	Coilcraft
1	L3	Inductor, SMT, 1.0-uH, 9-A, 9-milliohm		DO3316P-102	Coilcraft
1	R15	Resistor, Chip, 1.87k, 1%	0603	Std	Std
1	R16	Resistor, Chip, 2.80k, 1%	0603	Std	Std
1	R17	Resistor, Chip, 1.47k, 1%	0603	Std	Std
1	R25	Resistor, Chip, 39k Ohms, 1%	0603	Std	Std
3	R3, R4, R5	Resistor, Chip, 71.5k, 1%	0603	Std	Std
6	R6, R7, R8, R12, R13, R14	Resistor, Chip, 5.11k, 1%	0603	Std	Std
3	R9, R10, R11	Resistor, Chip, 1k, 1%	0603	Std	Std
2	U1, U2	IC, IFET Power Controller, Adj-V, 3A	PWP20	TPS54310PWP	TI
1	U3	IC, 6A Output Synchronous Buck PWM (SWIFT), Adj-V	PWP28	TPS54610PWP	TI
1	U4	IC, Micro-Power 150 mA LDO Regulator	SOT23-5	TPS73118DBV	TI
1	U5	IC, 3-A Sink/Source DDR Termination Regulator	DGQ10	TPS51100DGQ	TI

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