Texas Instruments

TPS50601 Point of Load Regulator
SEE Summary

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James F. Salzman
Distinguished Member Technical Staff
Director of Technology & Radiation Effects
salzman@ti.com

Overview

- As with most DC-DC synchronous regulators, inductive fly back voltages can approach or exceed the breakdown voltage of the power drivers. In most cases these are MOSFET’s.

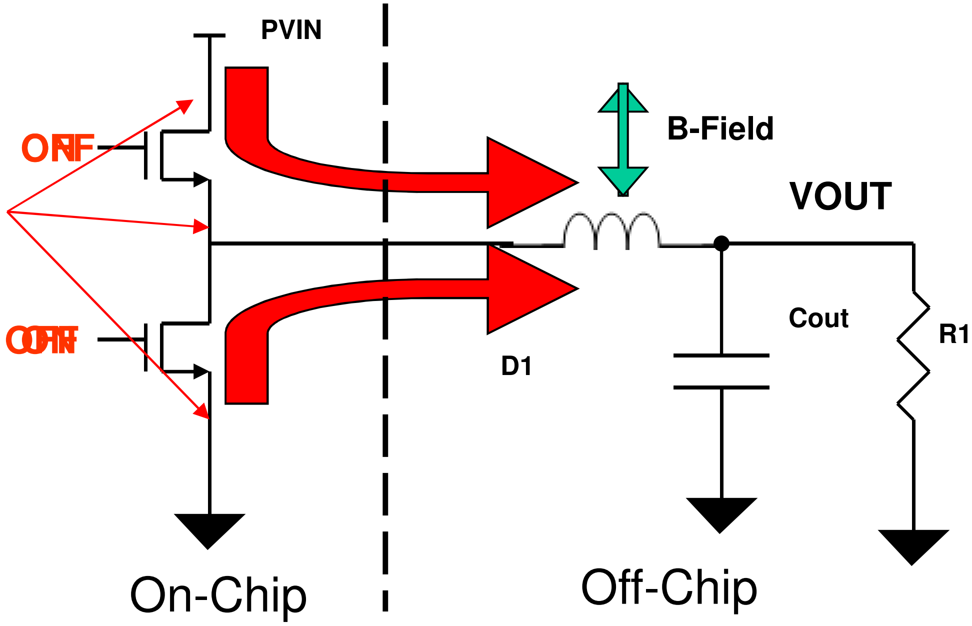
- The TPS50601 uses integrated power MOSFET’s. Further more package inductive parasitics can also contribute to inductive fly back voltage boost, in addition to the external inductor used.

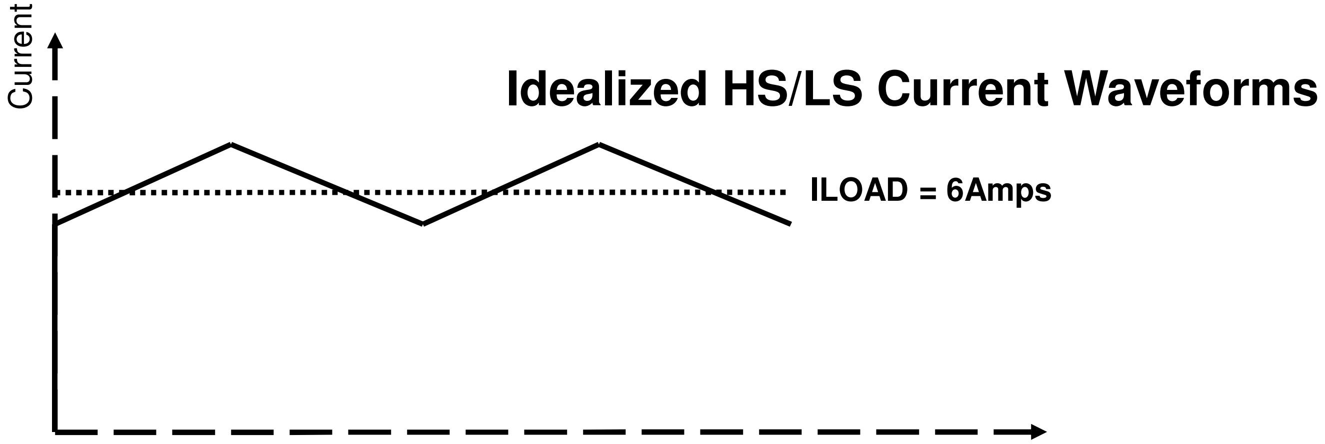
- High Side and Low Side power FET devices can see voltage stress in both high current and no load conditions respectfully. Because of this reason, Single Event Burnout tests of DC-DC converters must be tested to both conditions under heavy ion exposure.

High Side Failure Mechanism
(Heavy Load Conditions)

Current Flow in Synchronous DC/DC

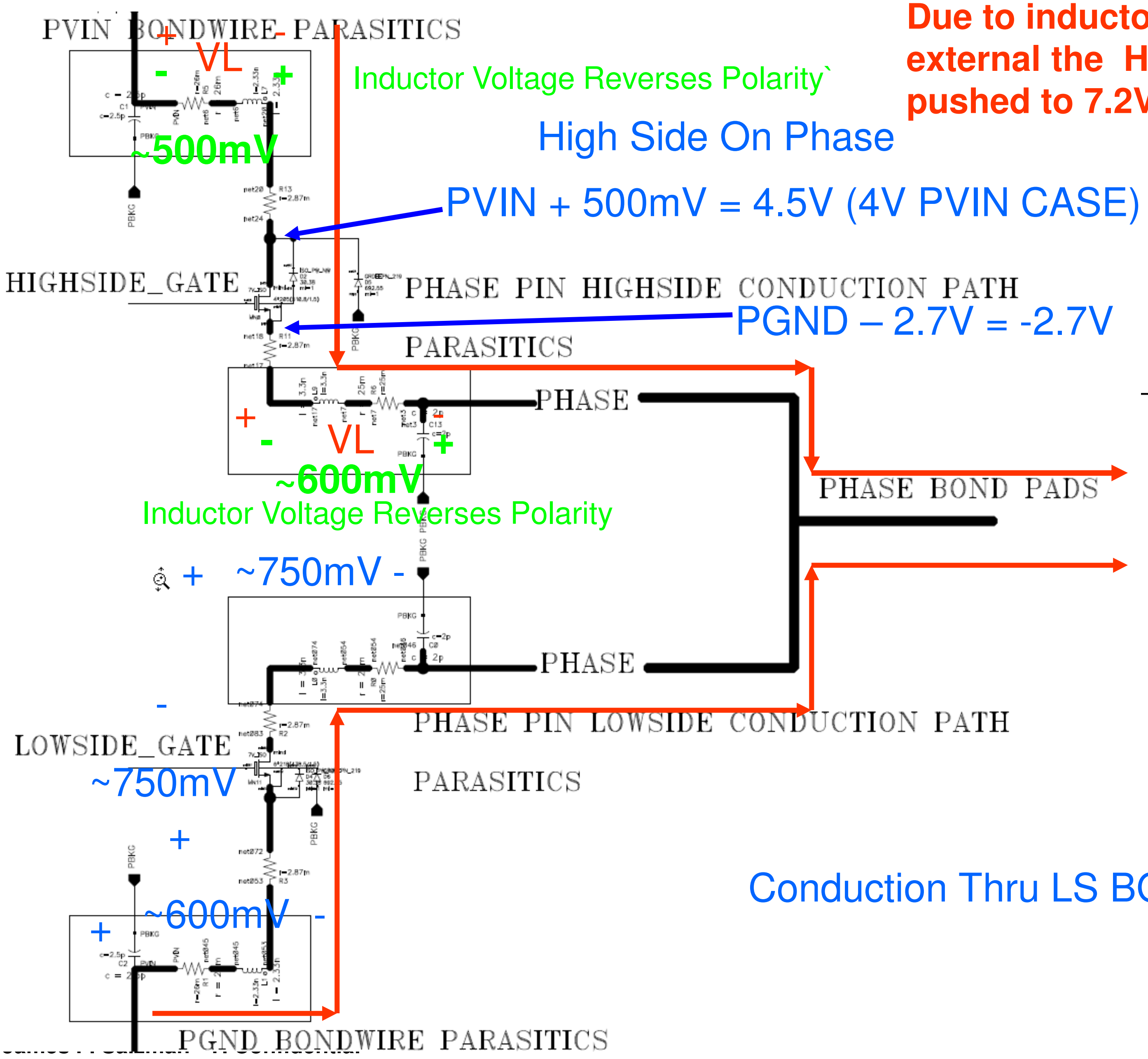
During switching the high side FET experiences stress due to the large changes in current in the bond wire and package parasitics during the inductive switching





Closer Look at Current Flow in Parasitics

Due to inductors, both parasitic and external the High Side FET voltage is pushed to 7.2V for a PVin of just 4V



Inductor Voltage Reverses Polarity`

~500mV

High Side On Phase

PVIN + 500mV = 4.5V (4V PVIN CASE)

PGND – 2.7V = -2.7V

~600mV

Inductor Voltage Reverses Polarity

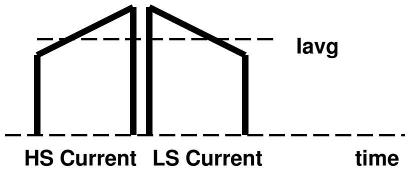
+ ~750mV -

-

~750mV

+

+ ~600mV -



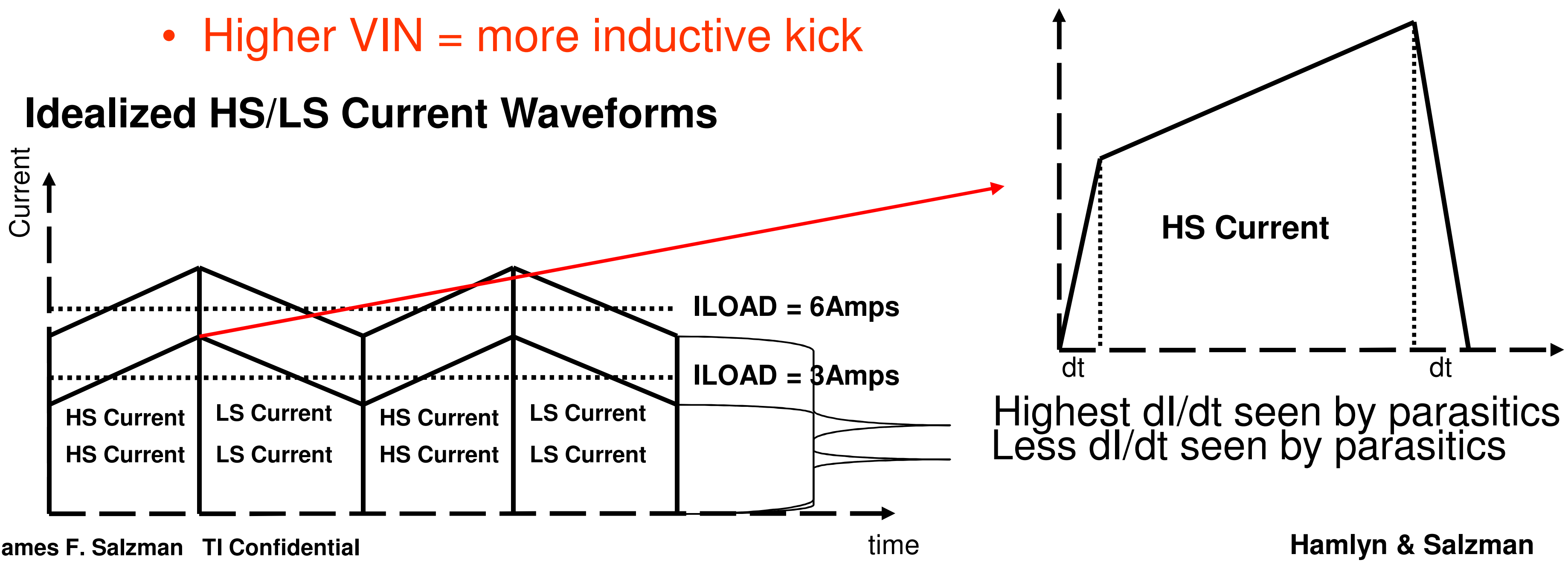
Charge Output Inductor

Low Side BG Diode turns on to maintain conduction Path during Dead-Time

Conduction Thru LS BG Diode Phase

Worse Case Stress

- Conditions selected to keep the part operating within the operational boundaries spelled out in the product datasheet.
  - Sinking Current Limit must be considered (~3Amps)
  - High Side Current Limit must be considered (~10Amps)
  - dt is a function of Vin Supply Level
    - Higher VIN = more inductive kick



Idealized HS/LS Current Waveforms

Realistic Current Waveform

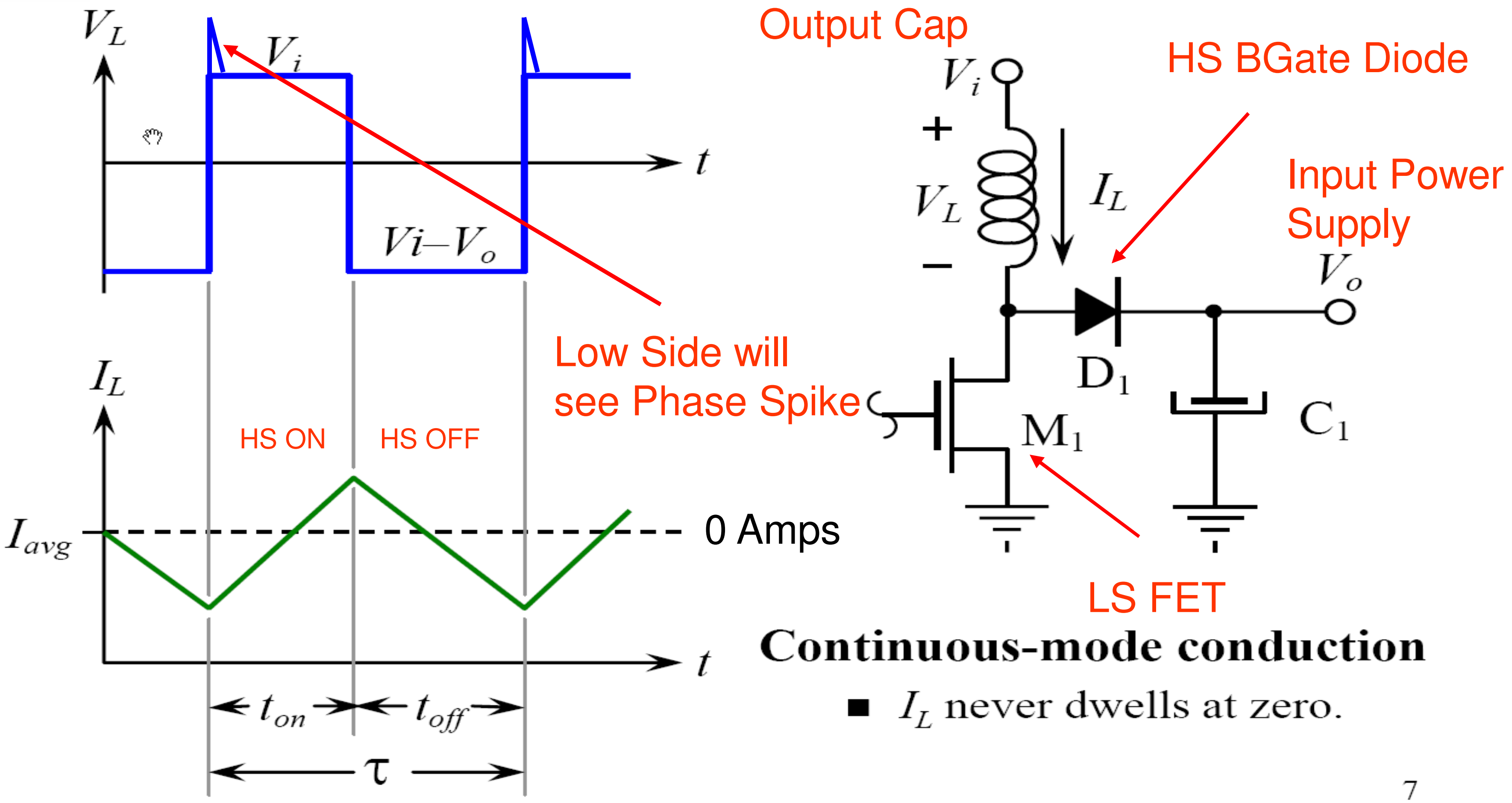
Highest dI/dt seen by parasitics
Less dI/dt seen by parasitics

Worse Case Conditions for High Side Power FET

- Highest Vin will give highest inductive kick in the package parasitics due to higher gate drive on Power FETS (i.e. FETS turn on and off faster…)
  - Vin = 6.3V
- Highest Load will give largest $\Delta I_{current}$
  - Iload = 6 Amperes
- Simulations were conducted to determine how bad the stress on the high side could become under worse case specified operating conditions

Low Side Failure Mechanisms
(light load Conditions)

Voltage Stress under No-Load



Output Cap

HS BGate Diode

Input Power Supply

Low Side will see Phase Spike

HS ON

HS OFF

0 Amps

LS FET

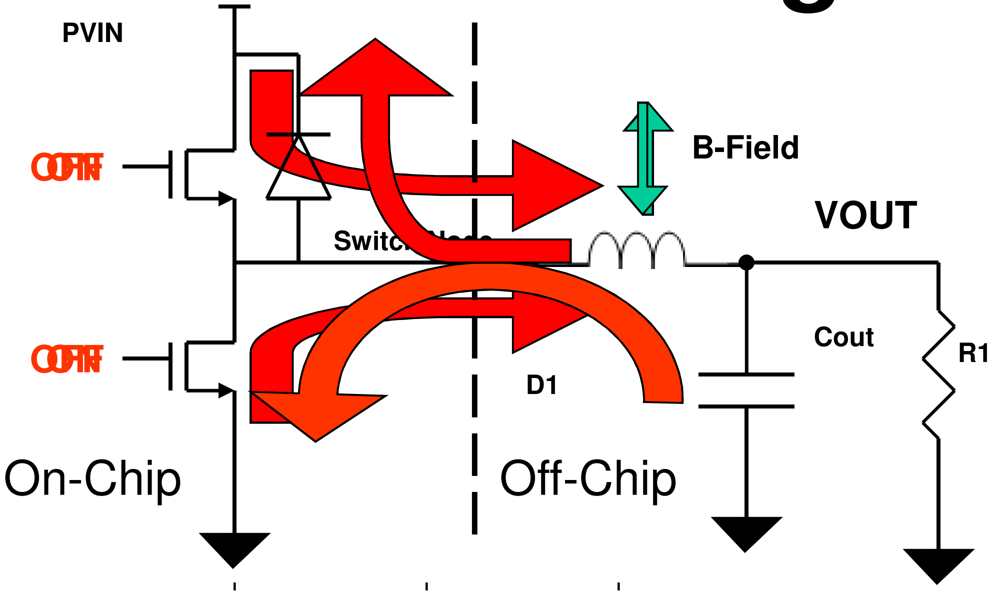
Continuous-mode conduction

- I_L never dwells at zero.

In continuous mode conduction never dwells at 0 Amperes. In a “No Load” condition, during the LS On phase, current is sinking in the reverse direction from the output capacitor, through the output inductor and ultimately through the Low Side FET. At the end of the switching cycle, when the Low Side is told to turn off, The current that was sunk through the inductor will cause the polarity to flip on the inductor and boost phase Higher than the input power supply voltage. This forward biases the High Side back gate diode above the input Power supply and since the input power supply will not be able to sink current, this extra charge is dumped into the PVIN input decoupling cap. This results in a Phase voltage spike and depending on the Level of PVIN, results in electrical overstress of the Low Side Power FET

Phase Boost during No-Load

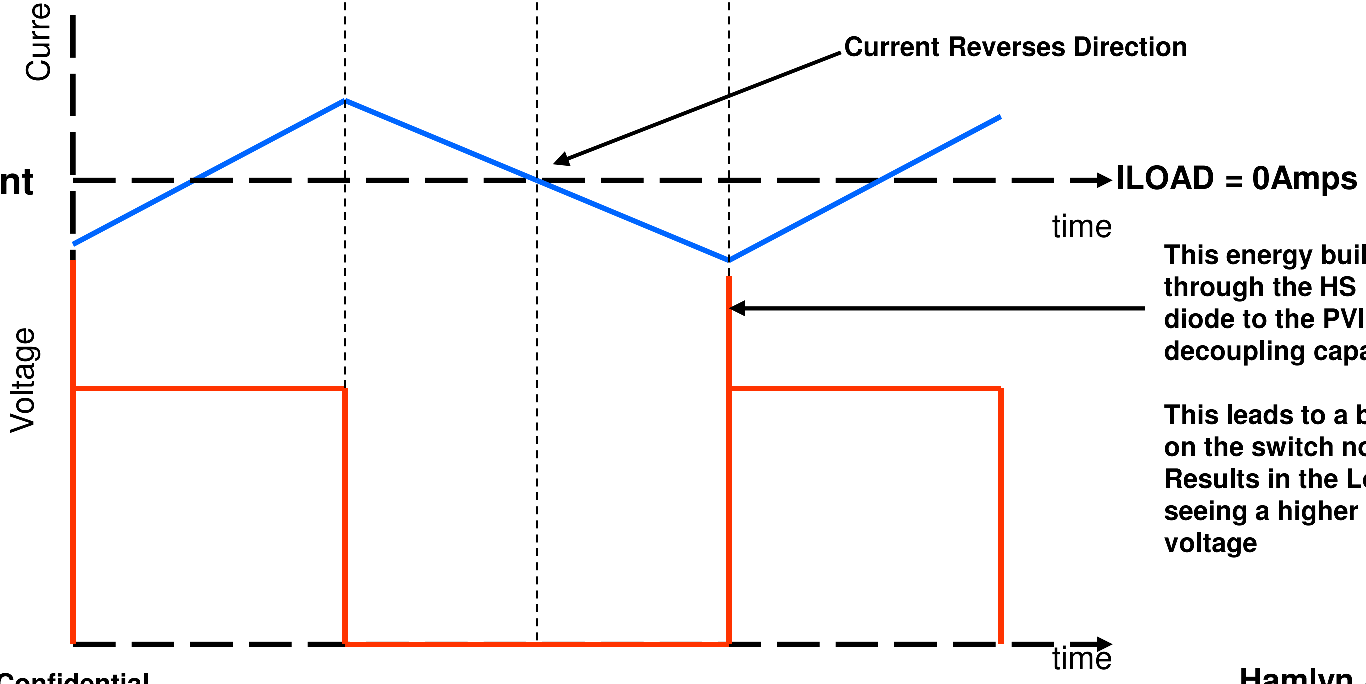
This Charges the B-Field of the inductor, but now in the opposite direction using charge from the output Filter capacitor. This is opposite of how the B-Field charges in a normal switching cycle



If the a heavy ion Strikes occurs during the time of this Switch node spike, The Low Side Power FET CAN BURNOUT If $V_{DSLowside}$ is greater than the voltage required to breakdown the drain during a heavy ion strike

Inductor Current

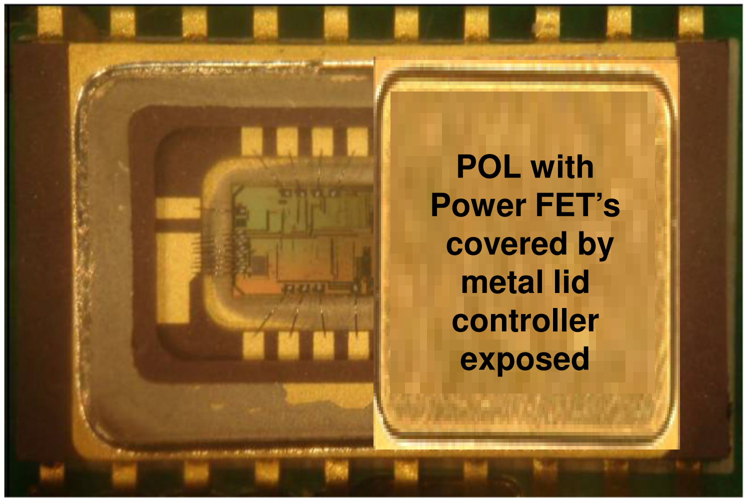
Switch Node



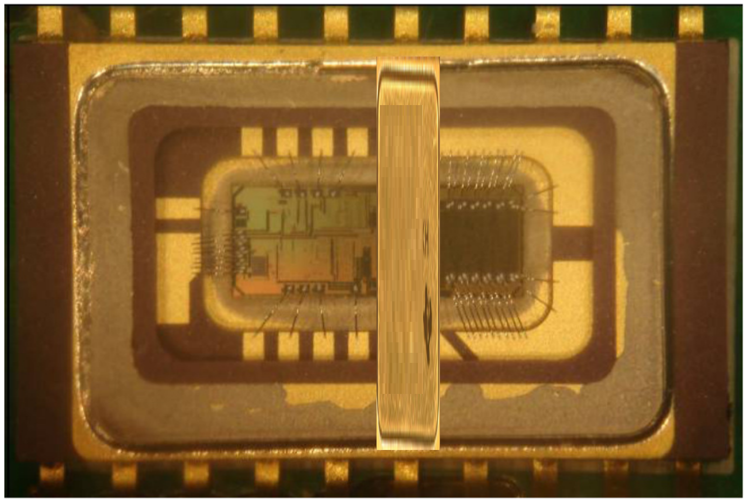
This energy buildup is dumped through the HS Backgate diode to the PVIN input decoupling capacitor

This leads to a boosting action on the switch node that Results in the Low Side FET seeing a higher drain to source voltage

Previous SEB Heavy Ion Masking Test Results
High Side FET Failure remains

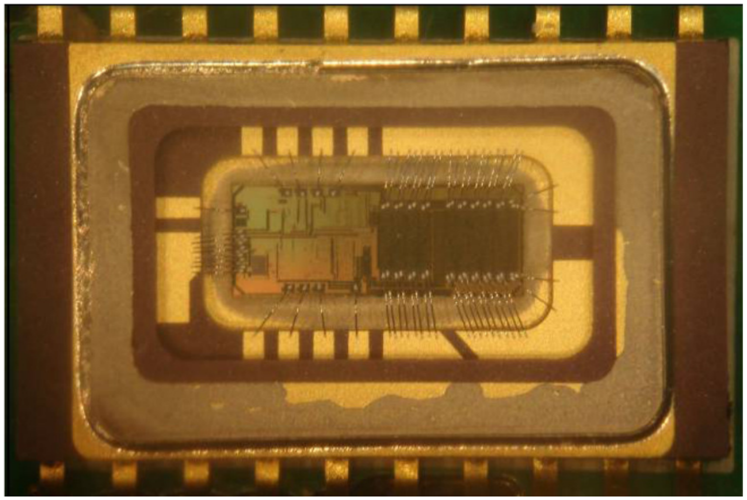


- **Power FET's masked from heavy ion exposure**
- Controller exposed to heavy ions
- Part functioned well to 85MeV-cm^2/mg
- Output perturbations noted – soft starts
- 1E7 ions/cm^2 – no SEL/SEB events
- No FET damage (simultaneous gate drive)
- Controller passed $\leq$ 7.5Volts (V_{in})
- SEB observed at 8 Volts (V_{in})
- Tests covered 25° -125° C



- **7V HS FET masked from heavy ion exposure**
- Controller exposed to heavy ions
- LS Power FET exposed to heavy ions
- Part functioned well to 85MeV-cm^2/mg
- Output perturbations noted – soft starts
- 1E7 ions/cm^2 – no SEL/SEB events
- No FET damage (simultaneous gate drive)
- Controller & LS FET passed $\leq$ 7.5Volts (V_{in})
- SEB seen at 8 Volts (V_{in})
- Tests covered 25° -125° C

SEB Heavy Ion Full Die Test Results with improved High side and Low side FETs



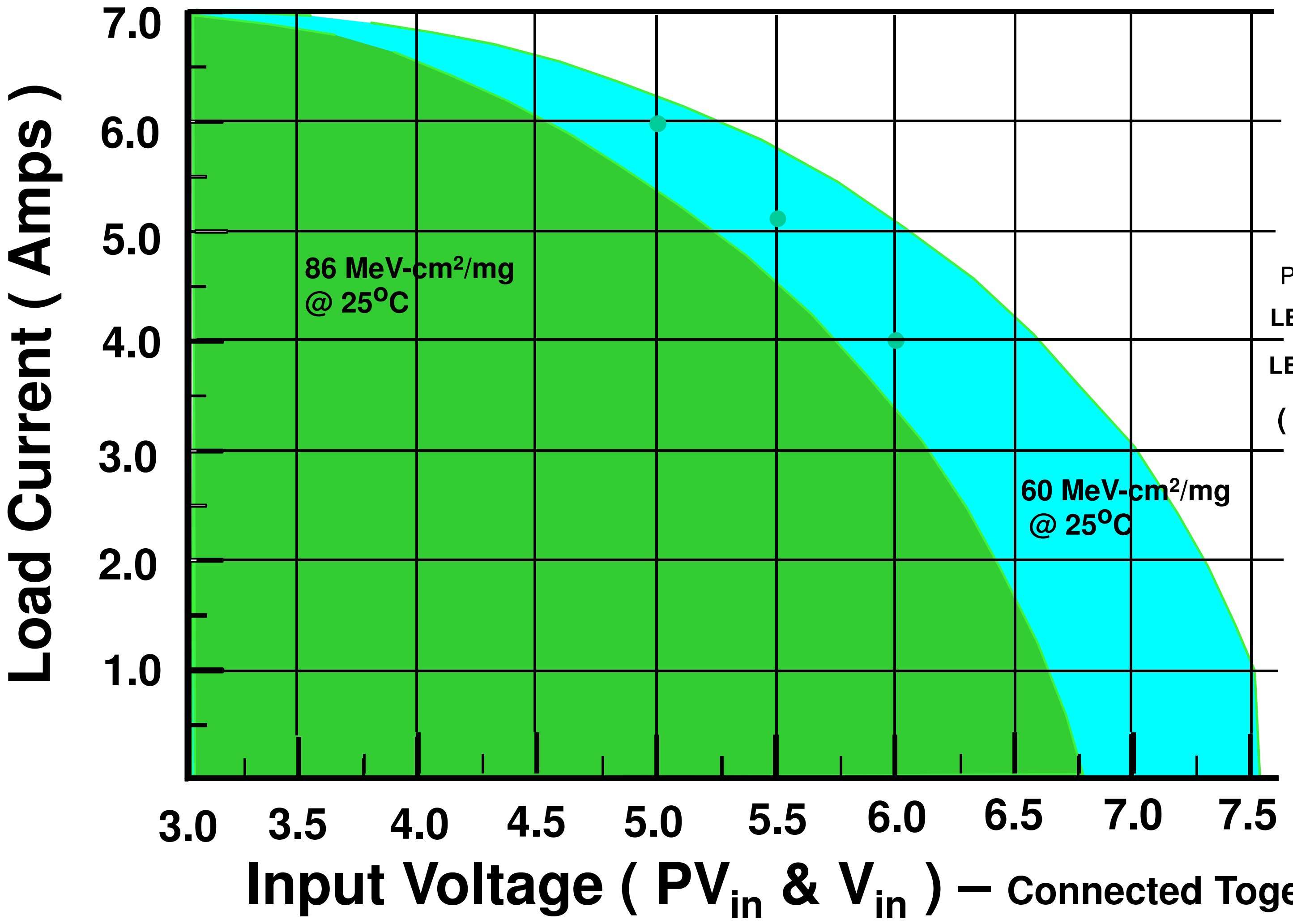
- From Simulation and previous test results
- HS FET Stress = high load conditions
- LS FET Stress = light load conditions
- Matrix of test conditions to cover both cases
- In both conditions high PVin contributes to SEB
- Improved LDMOS Power FET’s

- SEB characterization tests were preformed at TAMU on 7-25-2012
- The die was fully exposed.
- High flux levels were used to minimize required beam time 1E5 ions/cm^2
- A Safe Operating Area was generated from the SEB data. (See next 2 slides)
- A second test at TAMU on 12-2012 validated additional points on the SOA curve

TPS50601 7-25-2012 TAMU Run Log SEB Tests

Run	Device	Selected	Nominal LET	Effective LET	Effective		Average	DUT	Vin	Pvin	Output	DUT Output	TEMP	Pass	Fail
number	Number	15 MeV/u Beam	(MeVcm2/mg)	(MeVcm2/mg)	Fluence(ions/cm2)	Dose(rad)	Flux(ions/(cm2s)	Tilt Angle	Voltge	Voltage	Voltage	Load Amps	C		
1	1A	141 Pr	60.5	60.5	1.00E+07	1.00E+04	1.00E+05	0 deg	5.0V	4.0 V	2.5 V	3	25	🟩	
2	1A	141 Pr	60.5	60.5	1.00E+07	1.00E+04	1.00E+05	0 deg	5.0V	4.5 V	2.5 V	3	25	🟩	
3	1A	141 Pr	60.5	60.5	1.00E+07	1.00E+04	1.00E+05	0 deg	5.0V	5.0V	2.5 V	3	25	🟩	
4	1A	141 Pr	60.5	60.5	1.00E+07	1.00E+04	1.00E+05	0 deg	5.0V	5.5V	2.5 V	3	25	🟩	
5	1A	141 Pr	60.5	60.5	1.00E+07	1.00E+04	1.00E+05	0 deg	5.0V	6.0V	2.5 V	3	25	🟩	
6	1A	141 Pr	60.5	60.5	1.00E+07	1.00E+04	1.00E+05	0 deg	5.0V	6.5V	2.5 V	3	25	🟩	
7	1A	141 Pr	60.5	60.5	1.00E+07	1.00E+04	1.00E+05	0 deg	5.0V	7.0V	2.5 V	3	25	🟩	
8	1A	141 Pr	60.5	60.5	-	-	1.00E+05	0 deg	5.0V	7.5V	2.5 V	3	25		🟥
9	1B	141 Pr	60.5	60.5	1.00E+07	1.00E+04	1.00E+05	0 deg	5.0V	5.0V	2.5 V	0	25	🟩	
10	1B	141 Pr	60.5	60.5	1.00E+07	1.00E+04	1.00E+05	0 deg	5.0V	5.5 V	2.5 V	0	25	🟩	
11	1B	141 Pr	60.5	60.5	1.00E+07	1.00E+04	1.00E+05	0 deg	5.0V	6.0V	2.5 V	0	25	🟩	
12	1B	141 Pr	60.5	60.5	1.00E+07	1.00E+04	1.00E+05	0 deg	5.0V	6.5V	2.5 V	0	25	🟩	
13	1B	141 Pr	60.5	60.5	1.00E+07	1.00E+04	1.00E+05	0 deg	5.0V	7.0V	2.5 V	0	25	🟩	
14	1B	141 Pr	60.5	60.5	1.00E+07	1.00E+04	1.00E+05	0 deg	5.0V	7.5V	2.5 V	0	25	🟩	
15	1B	141 Pr	60.5	60.5	1.00E+07	1.00E+04	1.00E+05	0 deg	5.0V	8.0V	2.5 V	0	25	🟩	
16	1B	141 Pr	60.5	60.5	-	-	1.00E+05	0 deg	5.0V	8.5V	2.5 V	0	25		🟥
17	2A	141 Pr	60.5	60.5	1.00E+07	1.00E+04	1.00E+05	0 deg	5.0V	5.0V	2.5 V	5	25	🟩	
18	2A	141 Pr	60.5	60.5	1.00E+07	1.00E+04	1.00E+05	0 deg	5.0V	5.5 V	2.5 V	5	25	🟩	
19	2A	141 Pr	60.5	60.5	1.00E+07	1.35E+05	1.00E+05	0 deg	5.0V	6.0V	2.5 V	5	25	🟩	
20	2A	141 Pr	60.5	60.5	-	-	1.00E+05	0 deg	5.0V	6.5V	2.5 V	5	25		🟥
21	2B	141 Pr	60.5	60.5	1.00E+07	1.35E+05	1.00E+05	0 deg	5.0V	5.0V	2.5 V	6	25	🟩	
22	2B	141 Pr	60.5	60.5	1.00E+07	1.35E+05	1.00E+05	0 deg	5.0V	5.5 V	2.5 V	6	25	🟩	
23	2B	141 Pr	60.5	60.5	-	-	1.00E+05	0 deg	5.0V	6.0V	2.5 V	6	25		🟥
24	3A	141 Pr	60.5	60.5	1.00E+07	1.35E+05	1.00E+05	0 deg	5.0V	5.5 V	2.5 V	4	25	🟩	
25	3A	141 Pr	60.5	60.5	1.00E+07	1.35E+05	1.00E+05	0 deg	5.0V	6.0V	2.5 V	4	25	🟩	
26	3A	141 Pr	60.5	60.5	1.00E+07	1.35E+05	1.00E+05	0 deg	6.3V	6.3V	2.5 V	4	25	🟩	
27	3A	141 Pr	60.5	85.6	1.00E+07	1.35E+05	1.00E+05	46 deg	5.5V	5.5V	2.5 V	4	25	🟩	
28	3A	141 Pr	60.5	85.6	-	-	1.00E+05	46 deg	6.0V	6.0V	2.5 V	4	25		🟥
29	3B	141 Pr	60.5	85.6	1.00E+07	1.35E+05	1.00E+05	46 deg	5.5V	5.5 V	2.5 V	4	125	🟩	
30	3B	141 Pr	60.5	85.6	1.00E+07	1.35E+05	1.00E+05	46 deg	6.0V	6.0V	2.5 V	4	125	🟩	
31	3B	141 Pr	60.5	85.6	-	-	1.00E+05	46 deg	6.3V	6.3V	2.5 V	4	125		🟥
32	4A	141 Pr	60.5	85.6	1.00E+07	1.35E+05	1.00E+05	46 deg	5.0V	5.0V	2.5 V	5.3	125	🟩	
33	4A	141 Pr	60.5	85.6	1.00E+07	1.35E+05	1.00E+05	46 deg	5.5V	5.5V	2.5 V	5.3	125	🟩	
34	4A	141 Pr	60.5	85.6	1.00E+07	1.35E+05	1.00E+05	46 deg	5.0V	5.0V	2.5 V	6	125	🟩	
35	4A	141 Pr	60.5	85.6	-	-	1.00E+05	46 deg	5.5V	5.5 V	2.5 V	6	125		🟥

TPS50601 PG3.0 SEE Safe Operating Area (SEESOA)*



59

Pr

Praseodymium

140.90765

PRAY-zee-oh-DIM-ee-um

LET@ 0° ~ 60MeV-cm^2/mg

LET@ 46° ~ 86MeV-cm^2/mg

(59.2/COS46.5 = 86)

● **86MeV-cm^2/mg @ 125^{o}C passing Data Points (note: SEB is better at elevated Temperature)**

*** All Data points taken at fluence = 1E7 ions/cm^2**
No SEB or SEL inside curve

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Conclusions

- Simulations demonstrated that the High Side FET experiences voltage stresses that are much higher than the applied PVIN. The higher the output current the higher the fly back voltage stress.

- The Low Side FET on the other hand experiences the highest stress under the No-Load Condition do to high voltage stress from phase boosting action.

- Both heavy load and no load conditions must be SEE tested. The HS power FET is stressed and will exhibit SEB under heavy current loads, while the LS FET is most stressed and is subject to SEB under light load conditions. Both cases are a function of PVin and to Vin to some degree.

SEB Test Conclusions

- Single Event Burnout test results verify simulations. The High Side FET experiences higher voltage stresses under high current loads. The inductive fly back adds to the PVin voltage, resulting in a higher Drain to Source voltage.
- The Low Side FET on the other hand experiences the highest stress under No-Load Condition do to high voltage stress from phase boosting action. This is a function of high output capacitance and inductive boost under no or light load conditions. This action results in a higher Drain to Source voltage.
- During SEFI events, the part shuts down and automatically re-enters soft start. There are several shutdown protection blocks in the POL. Multiple ion strikes could be causing the SEFI’s. SEE tests considered worst case.
- There were no positive going Vout upsets seen, all were droops.

Single Event Transient Test Results

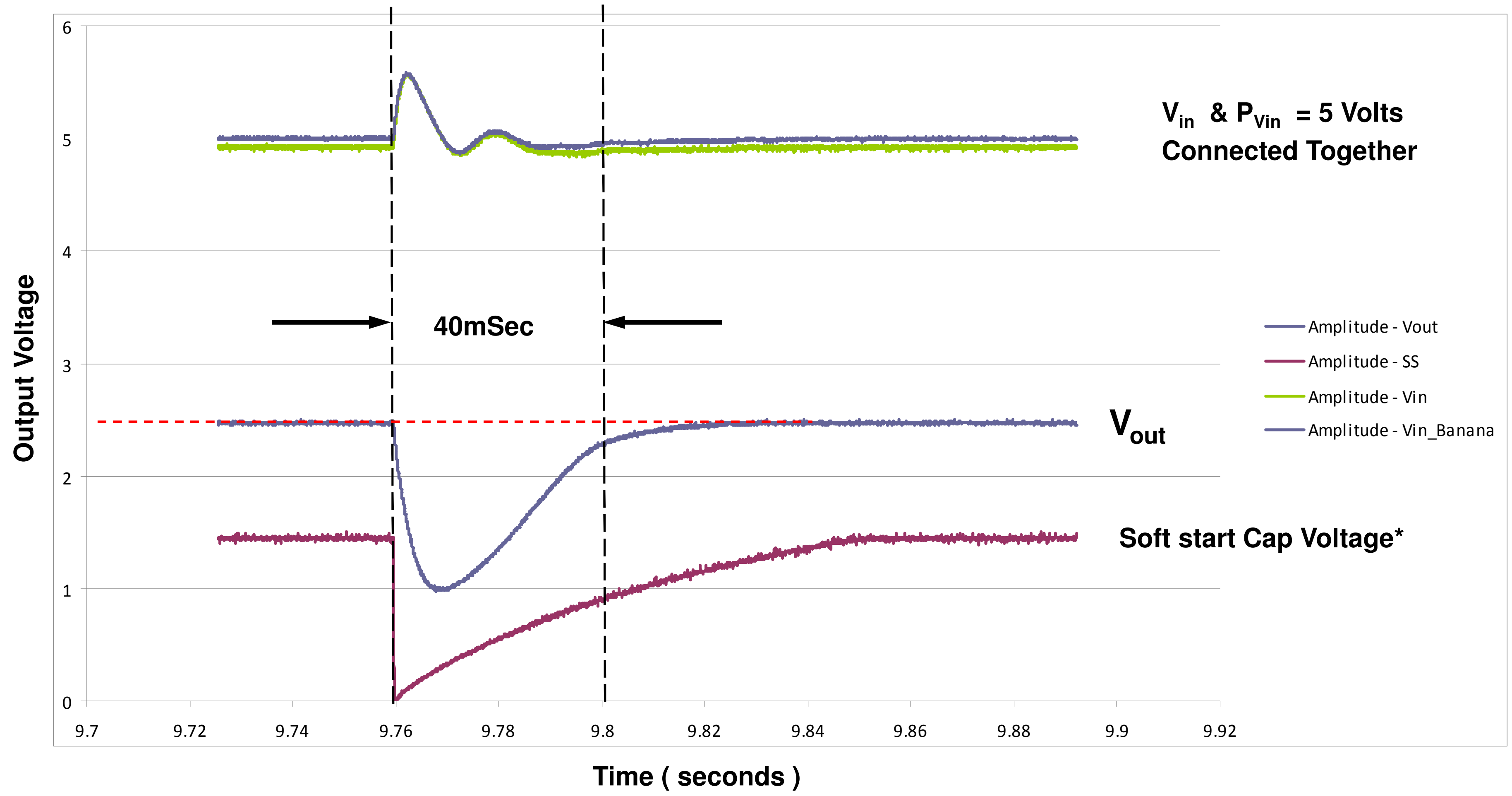
TPS50601 8-28-2012 TAMU Run Log X-Section

Run number	Selected 15 MeV/u Beam	Nominal LET (MeVcm2/mg)	Effective LET (MeVcm2/mg)	Effective Fluence(ions/cm2)	Dose(rad)	Average Flux(ions/(cm2s)	DUT Tilt Angle	Supply Voltge	Output Voltage	DUT Output Load Amps	SET A	SET X-section
3	Ag	44.3	62.7	2.72E+05	2.74E+02	1.04E+04	45 deg	5.5 V	2.5 V	0	9	3.30E-05
4	Ag	44.3	62.7	1.11E+06	1.11E+03	9.15E+03	45 deg	3.5 V	2.5 V	0	1	9.03E-07
8	Ag	44.3	62.7	1.00E+06	1.00E+03	8.19E+02	45 deg	3.5 V	2.5 V	0	0	0.00E+00
9	Ag	44.3	62.7	4.21E+05	4.23E+02	6.89E+02	45 deg	3.5 V	2.5 V	5	1	2.38E-06
12	Ag	44.3	45.9	1.36E+06	1.00E+03	1.81E+04	15 deg	3.5 V	2.5 V	0	4	2.93E-06
13	Ag	44.3	45.9	1.37E+06	1.01E+03	1.89E+04	15 deg	3.5 V	2.5 V	0	4	2.92E-06
14	Ag	44.3	44.3	1.29E+06	9.17E+02	1.58E+04	0 deg	3.5 V	2.5 V	0	5	3.87E-06
15	Ag	44.3	44.3	4.41E+05	3.13E+02	1.60E+04	0 deg	3.5 V	2.5 V	5	4	9.06E-06
16	Ag	44.3	44.3	5.14E+05	3.65E+02	1.55E+04	0 deg	5.5 V	2.5 V	5	9	1.75E-05
17	Ag	44.3	44.3	1.19E+06	8.41E+02	1.37E+04	0 deg	5.5 V	2.5 V	0	8	6.75E-06
18	Ag	44.3	44.3	1.21E+05	8.57E+01	1.28E+04	0 deg	3.4 V	1.2 V	0	8	6.63E-05
19	Ag	44.3	44.3	9.34E+05	6.63E+02	1.27E+04	0 deg	3.4 V	1.2 V	0	6	6.42E-06
20	Ag	44.3	44.3	5.71E+05	4.05E+02	1.33E+04	0 deg	3.4 V	1.2 V	6	7	1.23E-05
21	Ag	44.3	62.7	2.82E+05	2.83E+02	1.18E+04	45 deg	3.4 V	1.2 V	6	8	2.84E-05
22	Ag	44.3	62.7	4.02E+05	4.04E+02	1.18E+04	45 deg	3.4 V	1.2 V	0	9	2.24E-05
23	Ag	44.3	62.7	3.12E+05	3.14E+02	1.74E+04	45 deg	5.5 V	1.2 V	0	8	2.56E-05
24	Ag	44.3	62.7	2.54E+05	2.55E+02	1.80E+04	45 deg	5.5 V	1.2 V	6	7	2.76E-05
29	Ag	44.3	44.3	1.74E+05	1.23E+02	1.50E+04	0 deg	5.5 V	2.5 V	5	3	1.73E-05
34	Cu	20.7	20.7	9.96E+05	3.30E+02	1.05E+04	0 deg	5.5 V	2.5 V	5	0	0.00E+00
35	Cu	20.7	20.7	7.21E+05	2.39E+02	9.80E+03	0 deg	5.5 V	2.5 V	5	0	0.00E+00
36	Cu	20.7	20.7	1.00E+06	3.32E+02	1.06E+03	0 deg	5.5 V	2.5 V	5	0	0.00E+00
37	Cu	20.7	20.7	2.92E+05	9.66E+01	1.03E+03	0 deg	5.5 V	2.5 V	5	0	0.00E+00
38	Cu	20.7	20.7	1.00E+06	3.32E+02	9.69E+02	0 deg	5.5 V	2.5 V	5	0	0.00E+00
39	Cu	20.7	29.3	5.44E+05	2.55E+02	8.97E+02	45 deg	5.5 V	2.5 V	5	0	0.00E+00
40	Pr	60.5	60.5	4.79E+04	4.64E+01	1.11E+03	0 deg	5.5 V	2.5 V	5	3	6.26E-05
41	Pr	60.5	60.5	2.32E+05	2.25E+02	1.01E+03	0 deg	5.5 V	2.5 V	5	6	2.59E-05
42	Pr	60.5	62.6	1.42E+05	1.43E+02	1.00E+03	15 deg	5.5 V	2.5 V	5	2	1.41E-05
43	Pr	60.5	62.6	1.38E+05	1.38E+02	9.96E+02	15 deg	3.5 V	2.5 V	5	0	0.00E+00
44	Pr	60.5	85.6	3.24E+04	4.44E+01	1.07E+03	45 deg	3.5 V	2.5 V	5	1	3.09E-05
45	Pr	60.5	85.6	9.03E+04	1.24E+02	1.15E+03	45 deg	3.5 V	2.5 V	5	1	1.11E-05
46	Pr	60.5	85.6	1.70E+05	2.33E+02	1.16E+03	45 deg	3.5 V	2.5 V	5	3	1.77E-05
47	Pr	60.5	85.6	1.78E+05	2.44E+02	1.19E+03	45 deg	5.5 V	2.5 V	5	5	2.81E-05

SET = Soft Start Event

TPS50601 Heavy Ion SEFI Event

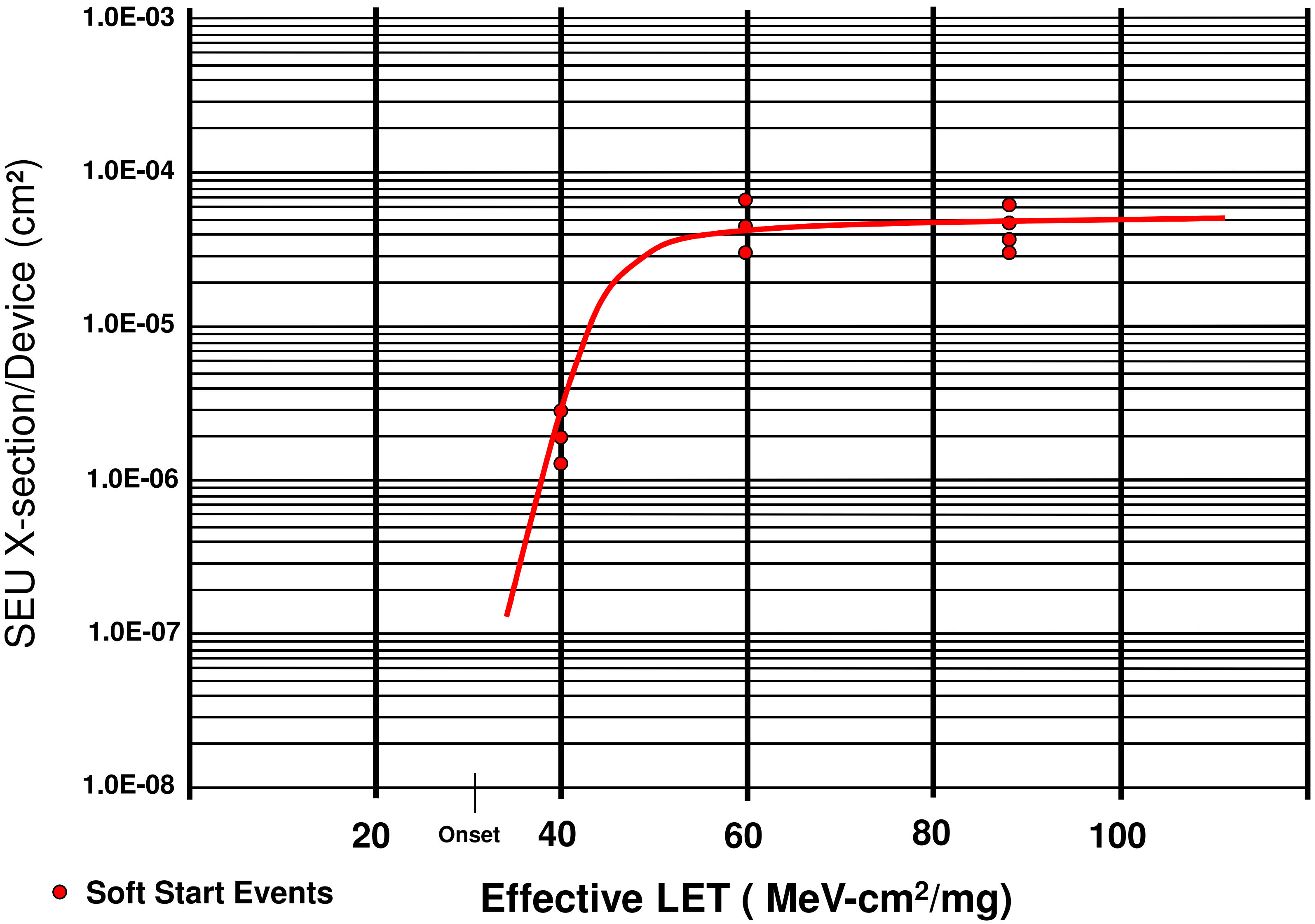
(shut down, and restart)



Device	Run	Time	Distance	Temp	Ion/LET	Angle	Device	Vin	Vout	Flux	Fluence	Load	Focus	Events
POL	47	12:44	40mm	25	Ho / 86MeV	35	2-Feb	5	2.5	1.00E+04	1.00E+06	5A	Vout	33

Test Conditions

TPS50601 SEFI Cross-Section



THANK YOU

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
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