Design Guide: TIDA-010978

Up to 1500V Stackable Battery Management Unit Reference Design with Integrated EIS

Description

This reference design is a full cell temperature sensing and high cell-voltage accuracy Lithium-ion (Li-ion), lithium iron phosphate (LiFePO4) battery pack (52s and 104s). The design monitors each cell voltage, cell temperature, impedance, while supporting integrated electrochemical impedance spectroscopy (EIS) and robust daisy-chain communication. This design supports up to 1500V stackable energy storage systems. These features make this reference design applicable for high-capacity battery pack applications.

Resources

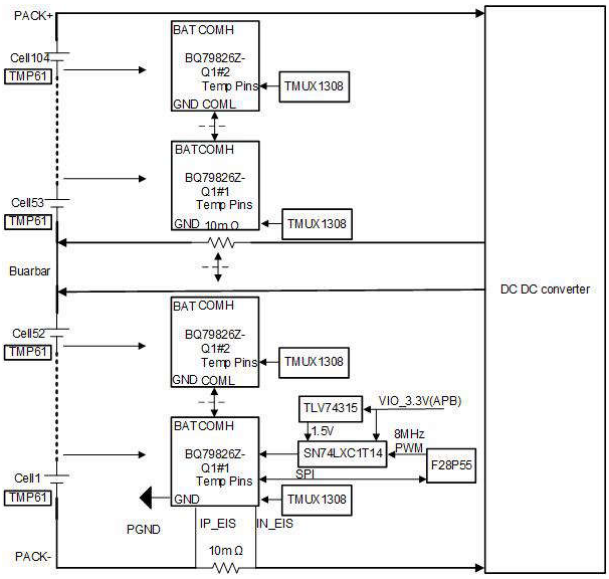
TIDA-010978	Design Folder
BQ79826Z-Q1	Product Folder
TMUX1308	Product Folder
SN74LXC1T14	Product Folder
TMP61	Product Folder

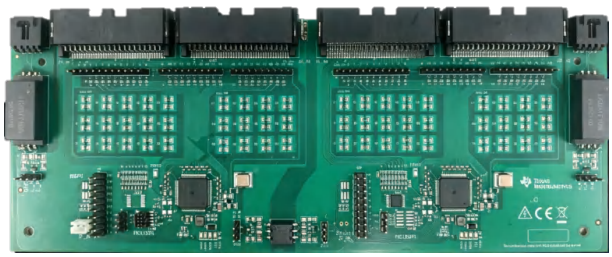
Features

- Integrated EIS for real-time monitoring
- Impedance Accuracy: 1% (with 5A excitation and 100uΩ impedance, Measurement frequency: 0.04Hz to 2kHz)
- ±1.7mV cell voltage accuracy at -40°C to 85°C
- Robust daisy-chain communication with data reclocking and ring architecture for 1500V stackable systems
- Full cell-temperature sensing with multiplexer (MUX) for up to 52 or 104 cells per pack
- Programmable cell/pack protection (OVP, UVP, OTP) with low-power shutdown mode (<10µA)
- Scalable modular architecture supporting multi-pack expansion via daisy-chain and CAN interfaces

Applications

- ESS – Battery management system (BMS)





1 System Description

Battery energy storage systems (BESS) continue rapid growth in residential, commercial, industrial, and grid-scale deployment. The industry is clearly trending toward 1500V high-voltage platforms, large-capacity 500Ah+ cells, and 104s high-series battery pack architectures. Large-format Li-ion and LiFePO4 cells improve system energy density, reduce overall BOM and installation cost, and support long-duration energy storage scenarios, while also bringing new safety and monitoring challenges to conventional BMS designs.

Traditional battery management systems rely only on cell voltage and surface temperature sampling for protection and state estimation. However, large-capacity cells feature high thermal inertia and obvious time delay between internal electrochemical reaction and external temperature rise. Conventional temperature sensors only trigger alarms in the late stage of thermal runaway, resulting in extremely short response windows for system mitigation. In addition, traditional SOC and SOH algorithms lack internal electrochemical characteristic data, leading to low estimation accuracy under dynamic charge-discharge conditions.

To address these industry pain points, the TIDA-010978 reference design is developed as a next-generation stackable BMU integrated with native EIS capability. This design adopts BQ79826ZQ1 as the core 26S battery monitor, supporting 52S per board and cascading to 104S for 1500V ESS applications.

Different from conventional BMU designs, TIDA-010978 integrates pack-level EIS measurement without adding extra excitation hardware, by reusing the active pack balancing power stage (TIDA-010990). TIDA-010978 realizes high accuracy of impedance measurement. Meanwhile, the design retains complete standard BMU functions including high-accuracy cell monitoring, full temperature coverage via multiplexer expansion, passive cell balancing, isolated daisy-chain stacking, and CAN FD communication.

This reference design fully complies with UL1973, IEC 62477, and GB 38031 safety regulations, providing complete hardware schematic, PCB layout, firmware framework, GUI upper computer, and test validation reports for high-voltage large-capacity energy storage developers.

1.1 Key System Specifications

General System Features

- Supports up to 1500V stackable ESS, 52S per BMU board, expandable to 104S battery pack
- Cell voltage accuracy: ±1.7mV across –40°C to 125°C without factory calibration
- Full cell-to-temperature coverage via TMUX1308 analog multiplexer expansion
- Ultra-low power modes: 5μA shutdown, 20μA sleep, 3mA typical operating current
- Robust isolated daisy-chain with ring network support for multi-board stacking
- Full protection: OVP, UVP, OTP, UTP, open-wire, communication fault diagnosis

EIS Exclusive Features

- EIS frequency range: 0.01Hz to 3.5kHz for full battery characteristic analysis
- Reuse active balancing circuit as EIS excitation source, max 5A excitation current
- Impedance precision: magnitude deviation <2%, phase deviation <1° full temperature range
- Time-sharing multiplexing of EIS scanning and APB balancing without mutual interference
- Enables thermal runaway early detection, high-precision SoC/SoH, lithium plating monitoring

2 System Overview

The TIDA-010978 system is divided into several core functional blocks with clear interface and signal interaction:

High-Voltage Cell Monitoring Block

Dual BQ79826Z-Q1 devices are deployed in daisy-chain stacking to sample 52S cell voltages synchronously. Each BQ79826Z-Q1 performs local over/undervoltage judgment and transmits raw data to the main MCU for system-level processing. The daisy-chain topology simplifies high-voltage stacking wiring and improves synchronization accuracy.

Temperature Sensing and Multiplexer Block

TMUX1308 expands limited GPIO ports to achieve full temperature sampling matching cell quantity. TMP61 linear thermistors are placed on cell surfaces and busbar key positions. Each multiplexer reserves fixed resistance channels for online fault diagnosis of switch stuck or open circuit.

EIS Excitation and Control Block

Based on TMS320F28P55 and external FETs, the system generates high-resolution PWM signals to control the power stage. The active balancing circuit is reused as EIS excitation source to inject adjustable AC current into the battery pack. Voltage and current responses are sampled synchronously for impedance spectrum calculation. Multiple pack-level excitation modes are supported for different stacking configurations.

Communication Interface Block

On-board BQ79826Z-Q1s adopt capacitor-isolated daisy-chain; inter-board stacking uses transformer isolation to form ring communication network. Isolated CAN FD provides high-speed data interaction between BMU and upper BCU controller for cell data, EIS spectrum and fault upload.

Protection and Diagnosis Block

Integrates hardware threshold protection and software logic judgment, covering cell voltage abnormality, over-temperature, excitation overcurrent, wiring open circuit and communication failure. Fault code and timestamp are recorded and uploaded via CAN for remote maintenance.

2.1 Block Diagram

Figure 2-1 shows the EIS BMU block diagram.

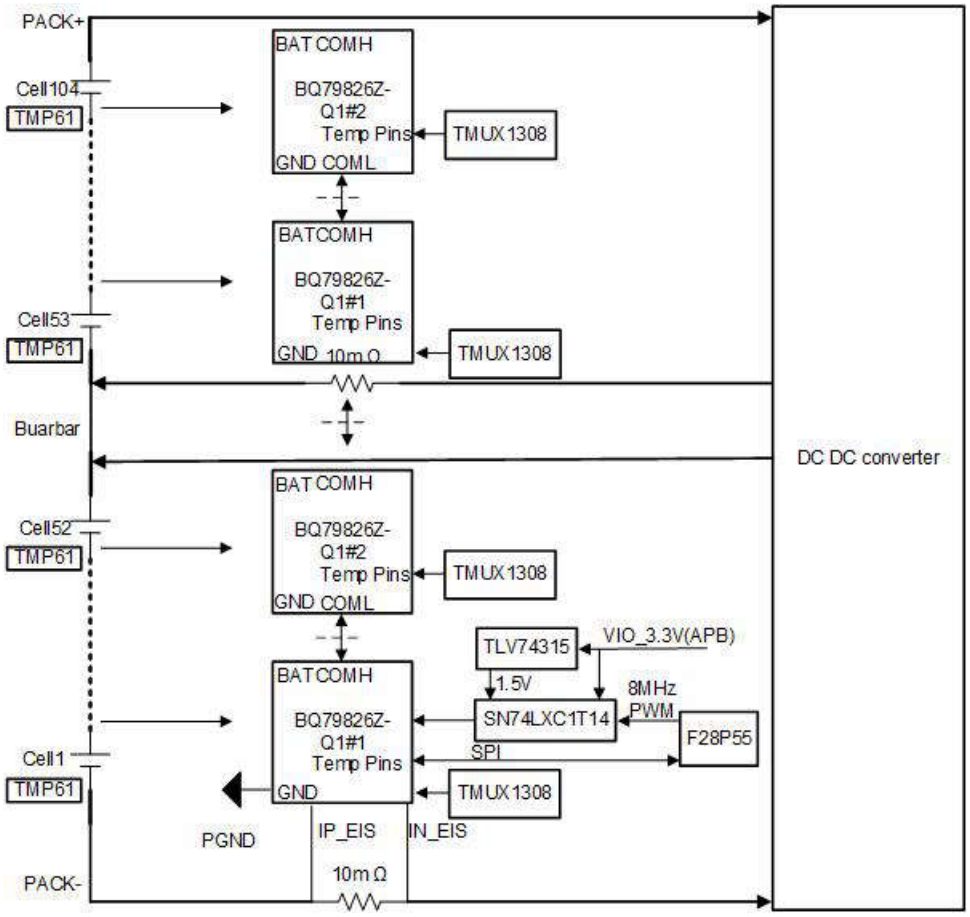


Figure 2-1. 1.TIDA-010978 EIS BMU Block Diagram

2.2 Design Considerations

2.2.1 High-Voltage Stackable Architecture

TIDA-010978 adopts modular stacking design. Single board integrates two BQ79826Z-Q1 to support 52S cell monitoring. Multiple BMUs can be cascaded via daisy-chain to expand to 104S and higher 1500V battery systems.

Each BQ79826Z-Q1 independently completes local cell voltage sampling and basic over/undervoltage protection. Data is transmitted to the main MCU through daisy-chain for system-level comprehensive analysis and scheduling. The daisy-chain communication adopts reclocking and signal shaping mechanism, maintaining stable transmission in high-voltage stacked cabinet environment. The modular design simplifies capacity expansion, on-site assembly and after-sales maintenance.

2.2.2 Electrochemical Impedance Spectroscopy (EIS) Subsystem

Traditional temperature and pressure sensors only respond in the middle and late period of thermal runaway. Battery internal failure undergoes SEI decomposition (80\120°C), electrolyte decomposition (120\150°C), pressure rise (150~200°C) and cathode collapse (>200°C). Only EIS can capture subtle impedance changes in the earliest SEI stage, realizing ultra-early warning.

EIS working principle: Apply controllable AC excitation to the battery pack → synchronously collect voltage and current response → calculate impedance amplitude and phase → scan multiple frequencies to form impedance spectrum → correlate with SOC, SOH, temperature and aging state.

This design selects active balancing circuit multiplexing excitation scheme, no additional excitation power stage required. The design supports 0.04Hz~2kHz accurate scanning, with single cell magnitude deviation <2% and phase deviation <1°, having excellent repeatability and SOC/temperature distinguish-ability. The design can be used for thermal early warning, high-precision state estimation and battery batch screening.

2.2.3 EIS Synchronization Requirement

Excitation output and voltage/current sampling must maintain precise time synchronization. Unified clock domain and hardware trigger are adopted to keep inter-device synchronization error within allowable range, avoiding phase deviation affecting EIS calculation.

2.2.4 PWM Input as Crystal of the First BQ79826Z-Q1

3.3V auxiliary input is stepped down by TLV74315, then converted to 1.5V analog/digital rails via LDO. MCU generates 8MHz PWM to first BQ79826Z as crystal. Analog and digital power/ground are strictly separated to suppress interference to high-precision sampling and EIS weak signals. All power rails have overvoltage, undervoltage and overcurrent protection.

2.2.5 Temperature Sensing and Multiplexer Network

Limited by AFE GPIO quantity, TMUX1308 8-to-1 multiplexers are used to expand temperature channels, realizing one-to-one cell temperature coverage. TMP61 linear thermistor features wide temperature linearity, low self-heating and fast response.

Each MUX reserves fixed resistance diagnosis channel. The system judges MUX channel stuck, open circuit and abnormal resistance by identifying standard resistance value. All stacked AFEs synchronously switch MUX channels, completing full temperature sampling within industry standard 1s period.

2.2.6 Cell Balancing Circuit and Operation

The design adopts passive balancing coordinated with BQ79826ZQ1 internal switch and external power resistors. Odd-even staggered balancing strategy disperses heat generation and avoids local overheating. Balancing action is linked with nearby temperature points; when over temperature is detected, balancing current is automatically reduced or shut down to maintain long-term safe operation.

2.2.7 MCU and System Control Architecture

TMS320F28P55 acts as the system master, undertaking EIS PWM generation, synchronous sampling control, data algorithm processing, balancing logic, fault diagnosis and CAN communication. The software layered design realizes decoupling of hardware and business logic, facilitating function iteration and porting. Multi-cycle task scheduling balances real-time performance and MCU resource consumption.

2.2.8 Protection and On-Board Diagnostics

Multi-level protection covers cell OVP/UVP, OTP/UTP, wiring open circuit, EIS excitation overcurrent, communication exception. The system automatically records fault time and code, uploads to upper computer via CAN, supporting remote troubleshooting and operation maintenance. Daily self-diagnosis pre-judges potential hidden dangers to improve system reliability.

2.3 Highlighted Products

2.3.1 BQ79826Z-Q1

The BQ79826Z-Q1 is a new high-cell count 26S stackable battery monitor that includes integrated electrochemical impedance spectroscopy (EIS) engine. The EIS engine provides a new way to detect impedance changes in the cell that allows for monitoring of aging, temperature, SoC, thermal runaway and many other cell parameters. In addition, the device incorporates an intelligent sensor controller to enable easier and more reliable sensor measurements.

2.3.2 TMUX1308

The TMUX1308-Q1 and TMUX1309-Q1 devices are general purpose complementary metal-oxide semiconductor (CMOS) multiplexers (MUX). The TMUX1308-Q1 is an 8:1, 1-channel (single-ended) MUX, while the TMUX1309-Q1 is a 4:1, 2-channel (differential) MUX. The devices support bidirectional analog and digital signals on the source (Sx) and drain (Dx) pins ranging from GND to VDD. The TMUX13xx-Q1 devices have an internal injection current control feature which eliminates the need for external diode and resistor networks typically used to protect the switch and keep the input signals within the supply voltage. The internal injection current control circuitry allows signals on disabled signal paths to exceed the supply voltage without affecting the signal of the enabled signal path. Additionally, the TMUX13xx-Q1 devices do not have an internal diode path to the supply pin, which eliminates the risk of damaging components connected to the supply pin or providing unintended power to the supply rail. All logic inputs have 1.8V logic compatible thresholds, providing both transistor-transistor logic (TTL) and CMOS logic compatibility when operating with a valid supply voltage. Fail-safe logic circuitry allows voltages on the control pins to be applied before the supply pin, protecting the device from potential damage.

2.3.3 TMP61

The Thermistor Design Tool offers the complete resistance versus temperature table (R-T table) computation and other helpful methods to derive temperature and example C-code. The TMP61 linear thermistor offers linearity and consistent sensitivity across temperature to enable simple and accurate methods for temperature conversion. The low power consumption and a small thermal mass of the device minimize self-heating. With built-in fail-safe behaviors at high temperatures and powerful immunity to environmental variation, these devices are designed for a long lifetime of high performance. The small size of the TMP6 series also allows for close placement to heat sources and quick response times. Take advantage of benefits over NTC thermistors such as no extra linearization circuitry, minimized calibration, less resistance tolerance variation, larger sensitivity at high temperatures, and simplified conversion methods to save time and memory. The TMP61 is currently available in a 0402 X1SON package, a 0603 SOT-5X3 package, and a 2-pin throughhole TO-92S package.

2.3.4 SN74LXC1T14

The SN74LXC1T14 is a single bit, dual-supply inverting voltage level translation device with Schmitt-trigger input. The input pin A is referenced to V_{CCI} logic levels, and output pin Y is referenced to V_{CCO} logic levels. The input pin A is able to accept voltages ranging from 1.1V to 5.5V and can be connected directly to V_{CCI} or GND. See *Device Functional Modes* for a summary of the operation of the logic.

This device maintains low power consumption and is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs when the device is powered down. This inhibits current backflow into the device which prevents damage to the device.

3 Hardware, Software, Testing Requirements, and Test Results

The key performances of the TIDA-010978 were tested in a TI lab. This section describes the end equipment used and the test processes and results.

3.1 Hardware Requirements

Board connectors are divided into cell sampling, temperature, daisy-chain. Each pin is defined with cell differential sampling, thermistor access, differential communication and fault signal functions, following uniform specification for convenient assembly and debugging.

Table 3-1. Battery Connector J4

CONNECTOR AND PIN ASSIGNMENTS	FUNCTION OR SCHEMATIC NET	NOTES
J4-1	TS1	Temperature Sense 1
J4-2	TS3	Temperature Sense 3
J4-3	TS5	Temperature Sense 5
J4-4	TS7	Temperature Sense 7
J4-5	GND	System Ground
J4-6	NC	No Connection
J4-7	NC	No Connection
J4-8	NC	No Connection
J4-9	NC	No Connection
J4-10	CELL0	Cell 0 Voltage Sense
J4-11	CELL2	Cell 2 Voltage Sense
J4-12	CELL4	Cell 4 Voltage Sense
J4-13	CELL6	Cell 6 Voltage Sense
J4-14	CELL8	Cell 8 Voltage Sense
J4-15	CELL10	Cell 10 Voltage Sense
J4-16	CELL12	Cell 12 Voltage Sense
J4-17	NC	No Connection
J4-18	NC	No Connection
J4-19	NC	No Connection
J4-20	NC	No Connection
J4-21	GND	System Ground
J4-22	TS2	Temperature Sense 2
J4-23	TS4	Temperature Sense 4
J4-24	TS6	Temperature Sense 6
J4-25	TS8	Temperature Sense 8
J4-26	NC	No Connection
J4-27	NC	No Connection
J4-28	NC	No Connection
J4-29	NC	No Connection
J4-30	GND	System Ground
J4-31	CELL1	Cell 1 Voltage Sense
J4-32	CELL3	Cell 3 Voltage Sense
J4-33	CELL5	Cell 5 Voltage Sense
J4-34	CELL7	Cell 7 Voltage Sense
J4-35	CELL9	Cell 9 Voltage Sense
J4-36	CELL11	Cell 11 Voltage Sense
J4-37	CELL13	Cell 13 Voltage Sense

Table 3-1. Battery Connector J4 (continued)

CONNECTOR AND PIN ASSIGNMENTS	FUNCTION OR SCHEMATIC NET	NOTES
J4-38	NC	No Connection
J4-39	NC	No Connection
J4-40	NC	No Connection
J4-MNT1	Mounting Pin 1	Mechanical/Shielding Ground
J4-MNT2	Mounting Pin 2	Mechanical/Shielding Ground

Table 3-2. Battery Connector J5

CONNECTOR AND PIN ASSIGNMENTS	FUNCTION OR SCHEMATIC NET	NOTES
J5-1	TS8	Temperature Sense 8
J5-2	TS10	Temperature Sense 10
J5-3	TS12	Temperature Sense 12
J5-4	TS14	Temperature Sense 14
J5-5	GND	System Ground
J5-6	NC	No Connection
J5-7	NC	No Connection
J5-8	NC	No Connection
J5-9	NC	No Connection
J5-10	CELL14	Cell 14 Voltage Sense
J5-11	CELL16	Cell 16 Voltage Sense
J5-12	CELL18	Cell 18 Voltage Sense
J5-13	CELL20	Cell 20 Voltage Sense
J5-14	CELL22	Cell 22 Voltage Sense
J5-15	CELL24	Cell 24 Voltage Sense
J5-16	CELL26	Cell 26 Voltage Sense
J5-17	PWR	Power Rail
J5-18	NC	No Connection
J5-19	NC	No Connection
J5-20	NC	No Connection
J5-21	GND	System Ground
J5-22	TS9	Temperature Sense 9
J5-23	TS11	Temperature Sense 11
J5-24	TS13	Temperature Sense 13
J5-25	TS15	Temperature Sense 15
J5-26	NC	No Connection
J5-27	NC	No Connection
J5-28	NC	No Connection
J5-29	NC	No Connection
J5-30	NC	No Connection
J5-31	CELL15	Cell 15 Voltage Sense
J5-32	CELL17	Cell 17 Voltage Sense
J5-33	CELL19	Cell 19 Voltage Sense
J5-34	CELL21	Cell 21 Voltage Sense
J5-35	CELL23	Cell 23 Voltage Sense
J5-36	CELL25	Cell 25 Voltage Sense
J5-37	NC	No Connection

Table 3-2. Battery Connector J5 (continued)

CONNECTOR AND PIN ASSIGNMENTS	FUNCTION OR SCHEMATIC NET	NOTES
J5-38	NC	No Connection
J5-39	NC	No Connection
J5-40	NC	No Connection
J5-MNT1	Mounting Pin 1	Mechanical/Shielding Ground
J5-MNT2	Mounting Pin 2	Mechanical/Shielding Ground

Table 3-3. Communication Connector J1

CONNECTOR AND PIN ASSIGNMENTS	FUNCTION OR SCHEMATIC NET	NOTES
J1-1	BMU_COMML_P	Daisy-Chain Positive Input
J1-2	BMU_COMML_N	Daisy-Chain Negative Input
J1-3	(GND / Reference)	Transformer Return Path
J1-4	(NC)	No Connection

Table 3-4. Communication Connector J2

CONNECTOR AND PIN ASSIGNMENTS	FUNCTION OR SCHEMATIC NET	NOTES
J2-1	BMU_COMMH_N	Daisy-Chain Negative Output
J2-2	BMU_COMMH_P	Daisy-Chain Positive Output
J2-3	(GND / Reference)	Transformer Return Path
J2-4	(NC)	No Connection

Table 3-5. Logic Level Connector J6

CONNECTOR AND PIN ASSIGNMENTS	FUNCTION OR SCHEMATIC NET	NOTES
J6-1	AVDD	Analog 3.3V Power Rail
J6-2	VIO	Digital 3.3V Power Rail
J6-3	GND	System Ground

Table 3-6. MCU Connector J7

CONNECTOR AND PIN ASSIGNMENTS	FUNCTION OR SCHEMATIC NET	NOTES
J7-1	MCU2AFE_PWM	PWM Control Signal to AFE
J7-2	MCU_SCLK	SPI Clock
J7-3	MCU_MOSI	SPI Master Out / Slave In
J7-4	MCU_MISO	SPI Master In / Slave Out
J7-5	MCU_NCS	SPI Chip Select
J7-6	VIO	3.3V Power Rail
J7-7	GPIO3 / NFAULT	Fault Indication Signal
J7-8	GND	System Ground
J7-9	AFE2MCU_PWM	Feedback PWM from AFE
J7-10	GND	System Ground

Table 3-7. GPIO Debug Connector J8

CONNECTOR AND PIN ASSIGNMENTS	FUNCTION OR SCHEMATIC NET	NOTES
J8-1	GPIO19	General-Purpose I/O 19
J8-2	GPIO20	General-Purpose I/O 20

Table 3-7. GPIO Debug Connector J8 (continued)

CONNECTOR AND PIN ASSIGNMENTS	FUNCTION OR SCHEMATIC NET	NOTES
J8-3	GPIO17	General-Purpose I/O 17
J8-4	GPIO18	General-Purpose I/O 18
J8-5	GPIO15	General-Purpose I/O 15
J8-6	GPIO16	General-Purpose I/O 16
J8-7	GPIO13	General-Purpose I/O 13
J8-8	GPIO14	General-Purpose I/O 14
J8-9	GPIO11	General-Purpose I/O 11
J8-10	GPIO12	General-Purpose I/O 12
J8-11	GPIO9	General-Purpose I/O 9
J8-12	GPIO10	General-Purpose I/O 10
J8-13	GPIO7	General-Purpose I/O 7
J8-14	GPIO8	General-Purpose I/O 8
J8-15	GPIO5	General-Purpose I/O 5
J8-16	GPIO6	General-Purpose I/O 6
J8-17	GPIO3	General-Purpose I/O 3
J8-18	GPIO4	General-Purpose I/O 4
J8-19	GPIO1	General-Purpose I/O 1
J8-20	GPIO2	General-Purpose I/O 2

Table 3-8. Daisy Chain Connector J9

CONNECTOR AND PIN ASSIGNMENTS	FUNCTION OR SCHEMATIC NET	NOTES
J9-1	GND	System Ground
J9-2	COMMH_N	Daisy-Chain Negative
J9-3	COMMH_P	Daisy-Chain Positive

Table 3-9. Daisy Chain Connector J10

CONNECTOR AND PIN ASSIGNMENTS	FUNCTION OR SCHEMATIC NET	NOTES
J10-1	GND	System Ground
J10-2	COMML_N	Daisy-Chain Negative
J10-3	COMML_P	Daisy-Chain Positive

Table 3-10. External SPI Connector J12

CONNECTOR AND PIN ASSIGNMENTS	FUNCTION OR SCHEMATIC NET	NOTES
J12-1	VIO	3.3V Power Rail
J12-2	MSPI_SCLK	SPI Clock (AFE)
J12-3	MSPI_MOSI	SPI Master Out / Slave In (AFE)
J12-4	MSPI_MISO	SPI Master In / Slave Out (AFE)
J12-5	MSPI_NCS	SPI Chip Select (AFE)
J12-6	GND	System Ground

3.2 Software

Software framework is one of the most critical design considerations for TIDA-010978, adopting complete layered modular architecture with clear division of labor and strong scalability. The whole software is divided into hardware driver layer, middleware layer, application layer, and upper computer GUI layer.

Hardware diver layer: includes SPI, CAN, ePWM, eCAP, ADC, GPIO, multiplexer and other peripheral drivers, providing standard calling interfaces for upper layers.

Middleware layer: integrates temperature conversion, voltage filtering, communication protocol parsing, EIS raw data preprocessing and balancing logic algorithm.

Application layer: Adopts multi-cycle real-time task scheduling:

- 20μs high-priority task: EIS closed-loop control, PWM timing and ADC synchronous sampling
- 100ms task: Cell voltage and temperature data refresh, normal status upload
- 5s task: AFE status detection and fault diagnosis update
- 300s task: Full-band EIS scanning and spectrum data storage

Upper Computer GUI Interaction Layer: Implements data parsing, protocol interaction, real-time curve display, parameter configuration and automated test interface.

Task priority is strictly divided to maintain that protection and EIS synchronous control are not blocked by low-priority tasks. Fault handling, low-power switching and EIS flow logic are embedded in each layer to maintain system stability and functional integrity.

3.3 Test Setup

The BMU is placed in temperature chamber; cell interface connects battery, temperature ports connect thermistors, power and communication connect test instruments. Calibrate equipment parameters, configure BMU protection threshold and working mode, then test in sequence of voltage accuracy, EIS and power consumption.

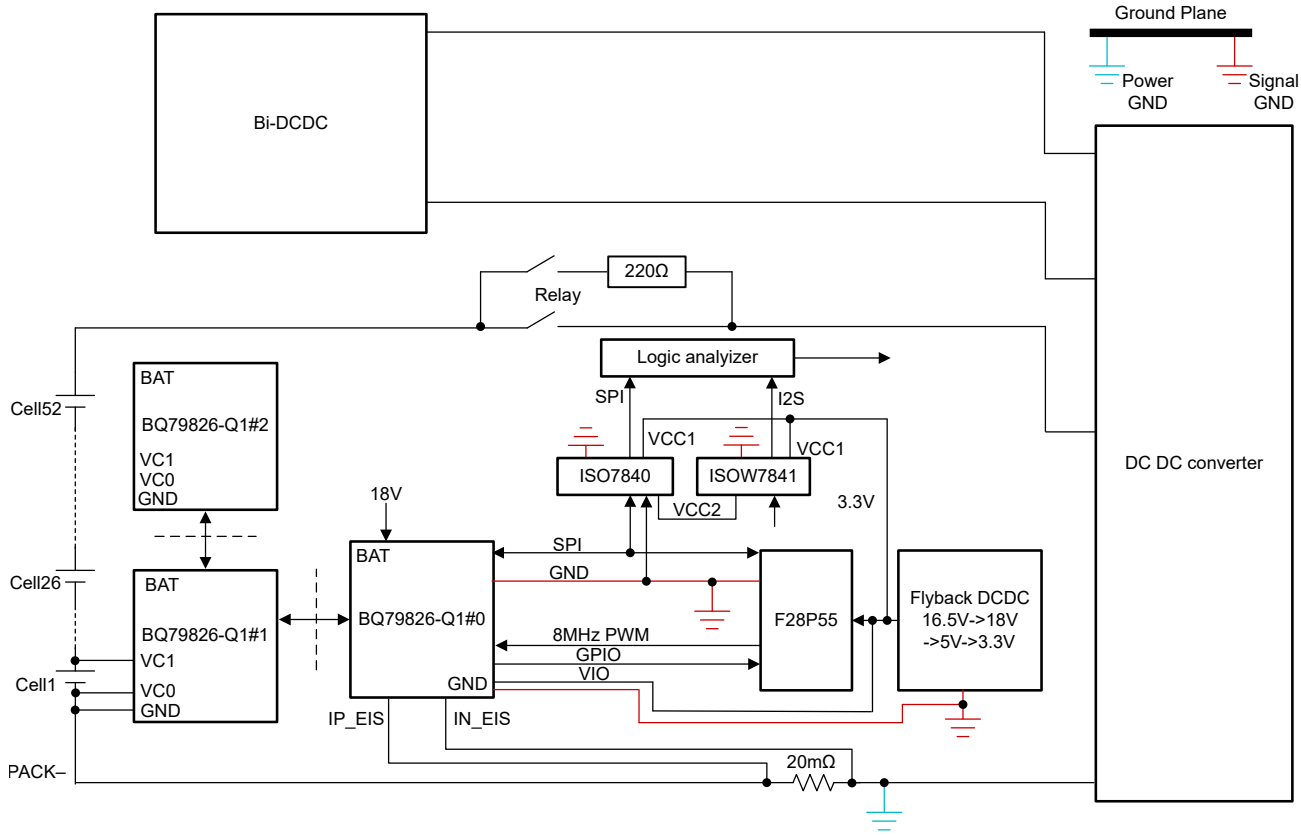


Figure 3-1. EIS BMU Test Setup

Figure 3-1 is a high-integrity test bench built around BQ79826 AFE devices, designed to validate a 52-series stackable battery management system (BMS) with integrated electrochemical impedance spectroscopy (EIS).

The system uses multiple cascaded BQ79826 ICs to simultaneously monitor cell voltage, temperature, and impedance across the full battery pack. The system features an isolated power architecture, including a flyback DC/DC converter, that generates 18V and 3.3V rails from a 16.5V input to power the AFE chain and the F28P55 C2000™ MCU.

Communication between the high-voltage BQ79826 domain and the low-voltage MCU is isolated using ISO7840/ ISO7841 digital isolators, supporting SPI and I2S signals safely across the barrier. A logic analyzer interface is included to capture and verify the integrity of these digital communication links during debug.

The test bench also incorporates a dedicated EIS signal path, with the MCU generating a 8MHz PWM stimulus that is injected into the battery via the BQ79826's EIS interface. A precision 20mΩ shunt resistor measures the resulting response current for impedance calculation.

An external 220Ω resistor is used as a pre-charge resistor, controlled by a relay to limit inrush current during system power-up and protect the downstream load circuits. The board employs a split ground plane design, with separate Power GND and Signal GND planes, to minimize noise and improve measurement accuracy in the high-voltage environment.

This comprehensive setup supports all validation steps, from cell voltage reliability tests in a temperature chamber to full EIS sweeps, making this setup a complete platform for verifying BMS functionality and performance under real-world conditions.

3.4 Pack Test Results

3.4.1 Cell Voltage Reliability Test

Test step

1. Put battery pack in the temp chamber and set temperature to room temperature. Wait for thermal equilibrium.
2. Collect Vcell data from all the cells.
3. Repeat step 2 nine times (10 measurements total).
4. Compute the mean and rms voltage value from each cell.

Test Result

Vrms < 0.3mV for every cell

Vmax < 1mV for every cell

3.4.2 EIS Measurement Repeatability

Test step

1. Put battery pack in the temp chamber and set temperature to room temperature. Wait for thermal equilibrium.
2. Collect Vcell data from all the cells.
3. Set excitation current to Imax and measure Z data (0.04Hz to 563Hz) 5 times.
4. Collect Vcell data from all the cells.

Test result

Magnitude deviation <2%, phase deviation <1°.

Table 3-11 shows the phase and magnitude deviation test result. Repeated scanning curves have high consistency; impedance characteristics under different SOC and temperature are clearly distinguishable.

Table 3-11. Phase and Magnitude Deviation Test Results

Cell No.	cell0	cell 1	cell 2	cell 3	cell 4	cell 5	cell 6	cell 7	cell 8	cell 9	cell 10	cell 11	cell 12	cell 13	cell 14	cell 15	cell 16	cell 17	cell 18	cell 19	cell 20	cell 21	cell 22	cell 23	cell 24	cell 25
Phase Deviation (degrees)	0.82	0.41	0.64	0.43	0.43	0.42	0.44	0.44	0.39	0.42	0.42	0.43	0.43	0.43	0.47	0.42	0.42	0.42	0.47	0.43	0.45	0.43	0.45	0.47	0.41	0.50
Magnitude Deviation (%)	1.69 %	0.77 %	0.97 %	0.87 %	0.72 %	0.71 %	0.69 %	0.75 %	0.67 %	0.68 %	0.69 %	0.73 %	0.71 %	0.70 %	0.72 %	0.66 %	0.68 %	0.64 %	0.71 %	0.76 %	0.83 %	0.83 %	0.83 %	0.81 %	0.79 %	0.77 %
Cell No.	cell26	cell 27	cell 28	cell 29	cell 30	cell 31	cell 32	cell 33	cell 34	cell 35	cell 36	cell 37	cell 38	cell 39	cell 40	cell 41	cell 42	cell 43	cell 44	cell 45	cell 46	cell 47	cell 48	cell 49	cell 50	cell 51
Phase Deviation (degrees)	0.67	0.83	0.69	0.91	0.33	0.54	0.27	0.49	0.32	0.48	0.29	0.42	0.35	0.37	0.38	0.40	0.38	0.36	0.46	0.45	0.40	0.38	0.43	0.39	0.41	0.41
Magnitude Deviation (%)	1.32 %	0.74 %	0.80 %	1.78 %	0.45 %	0.47 %	0.46 %	0.53 %	0.46 %	0.56 %	0.53 %	0.48 %	0.47 %	0.53 %	0.43 %	0.49 %	0.51 %	0.42 %	0.58 %	0.54 %	0.53 %	0.51 %	0.56 %	0.51 %	0.52 %	0.54 %

3.4.3 Pack EIS Measurement Nyquist Plot

Figure 3-2 is a Nyquist plot showing the measured impedance spectra of multiple cells within a series-connected pack. Each curve represents the impedance of one individual cell, plotted as imaginary impedance versus real impedance across a range of frequencies.

All curves follow the same general trend, starting near the real axis at high frequencies, forming a distinct arc in the mid-frequency range, and extending downward into the negative imaginary plane at low frequencies. The high-frequency region, close to the origin, corresponds to the ohmic resistance of each cell, which is consistent across all units. The mid-frequency arc reflects the combined effects of charge transfer and capacitive behavior at the electrode interfaces. The low-frequency tail shows the typical response associated with mass transport processes inside the cell.

While all curves share the same fundamental shape, there is a small but noticeable spread between them. This indicates minor differences in impedance magnitude and phase across the cells, which is expected due to normal manufacturing variations and minor differences in operating history. No curve deviates significantly from the common trend, confirming that all cells are operating within a similar range of electrical behavior.

This measurement demonstrates the ability to consistently capture the impedance response of every cell in the pack. The plot provides a clear visual representation of the overall impedance distribution and confirms that all cells exhibit the expected behavior for this type of energy storage device.

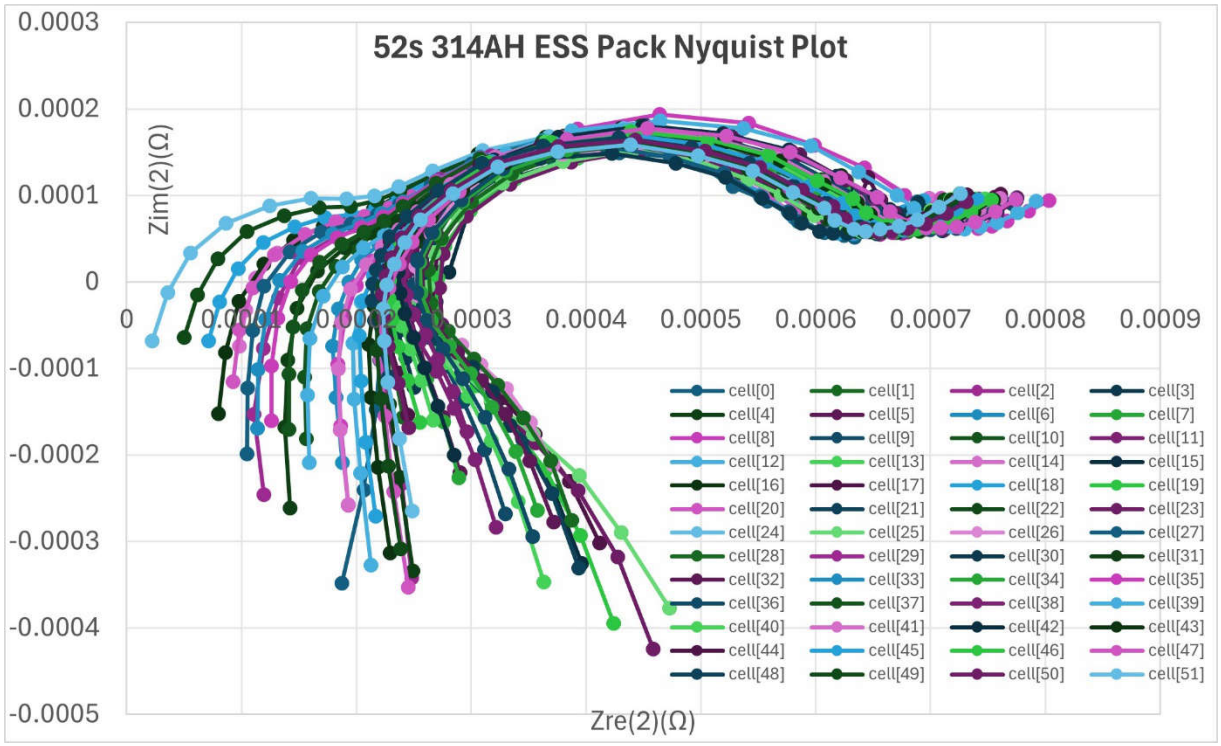


Figure 3-2. 2.Pack EIS Measurement Nyquist Plot

3.4.4 Current Consumption per BQ79826Z-Q1

Table 3-12. Current Consumption

	Shutdown current	Active operation current
1st BQ79826Z-Q1	<5uA	<3mA
2nd BQ79826Z-Q1	<5uA	<3mA
3rd BQ79826Z-Q1	<5uA	<3mA
4th BQ79826Z-Q1	<5uA	<3mA

Table 3-12 shows the current consumption per BQ79826Z-Q1. Low power consumption adapts long-term standby ESS application.

4 Design and Documentation Support

4.1 Design Files

4.1.1 Schematics

To download the schematics, see the design files at TIDA-010978.

4.1.2 BOM

To download the BOM, see the design files at TIDA-010978.

4.1.3 PCB Layout Recommendations

- Strict high/low voltage partition, follow 1500V creepage/clearance
- Analog EIS and temperature traces away from high-current switching loops
- Isolation zone complete partitioning, no cross routing
- Heating devices reserved sufficient heat dissipation copper and spacing
- Analog/digital ground separate, single-point star grounding
- Multiplexer sampling lines equal-length routing to ensure consistency

4.2 Tools and Software

CCSTUDIO Code Composer Studio™ integrated development environment (IDE)

4.2.1 Tools

USB2ANY interface adapter

4.3 Documentation Support

1. Texas Instruments, *LiFePO4 Design Considerations* application note
2. Texas Instruments, *BQ78706 Functional Safety-Compliant 14S Battery Monitor* data sheet
3. Texas Instruments, *Expanding Functionality of Cell Supervision Unit in Battery Management Systems* application brief

4.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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5 About the Author

JUNHUA YAN, is a TI system engineer from the SEM Energy Infrastructure team. Junhua focuses on battery pack and energy storage system applications and has created several designs to address industrial battery pack design challenges.

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