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# TLV987 3-V 10-BIt 27-MSPS Area CCD Analog Front End EVM

## User's Guide

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1998

Mixed-Signal Imaging Products

TEXAS INSTRUMENTS

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SLVU008

# TLV987 3-V 10-Bit 27-MSPS Area CCD Analog Front End EVM User's Guide

DRAFT ONLY

*Literature #SLVU008*

*September 1998*

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## Preface

# Read This First

### About This Manual

This User's Guide describes the features, operation, and use of the TI TLV987 evaluation module (EVM).

### How to Use This Manual

This document contains the following chapters:

- ❑ Chapter 1: Overview
- ❑ Chapter 2: Analog Input
- ❑ Chapter 3: Analog Outputs
- ❑ Chapter 4: Digital Inputs/Outputs
- ❑ Chapter 5: Clock Circuit
- ❑ Appendix A: TLV987 Data Sheet

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# Chapter 1

# Overview

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This user's guide describes features of the Texas Instruments evaluation module (EVM) for the TLV987 10-Bit, 27-MSPS, Area CCD Analog Front End (AFE). The EVM provides a platform for the lab prototype evaluation of the TI TLV987. Careful attention has been given to component selection, grounding, power supply bypassing, and signal path layout. The EVM uses standard SMA miniature RF connectors for the high-speed analog inputs and the outputs.

**Topic** **Page**

## 1.1 Schematic Diagram

Figure 1−1 is the schematic diagram for the EVM.

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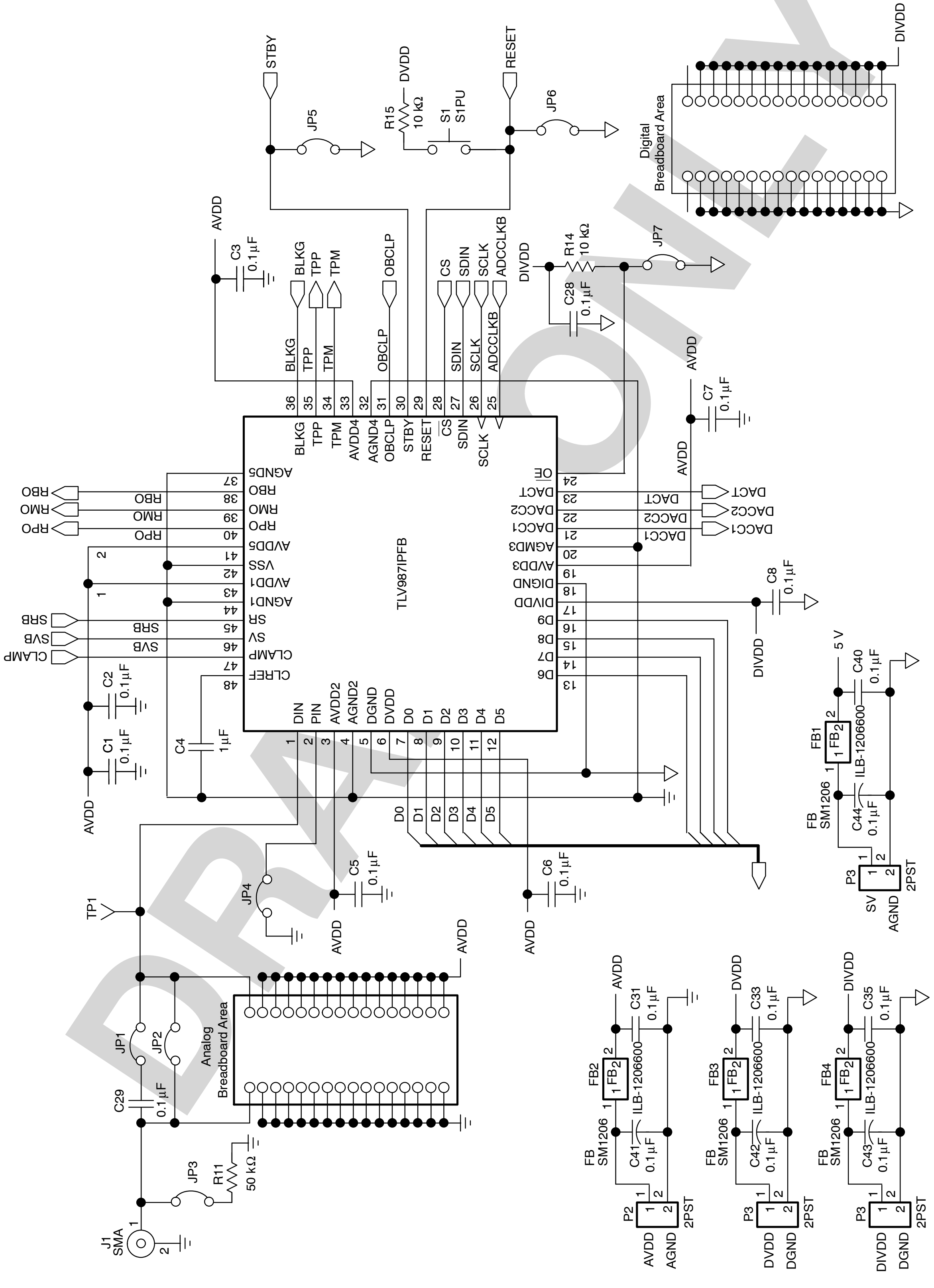
*Figure 1−1. EVM Schematic Diagram*



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## 1.2 Power Supply Requirements

The EVM can be powered by regulated lab power supplies. Three supplies are needed to power the EVM and the digital interface circuitry, and one is needed to supply analog power for the on-board op amps. Table 1−1 lists the supplies, the connectors used, and their uses.

*Table 1−1. EVM Power Supply Requirements*

| SUPPLY | CONNECTOR | USE |
|---|---|---|
| AVDD (3V) | P2 | Analog power |
| DVDD (3V) | P3 | Digital internal logic supply |
| DIVDD (2 – 4.4V) | P4 | Digital Interface logic supply |
| 5 V | P1 | Analog supply to the opamps |

The additional DIVDD supply allows the user to interface to different logic devices (having logic supplies in the range of 2 V – 4.4 V). The analog (AGND) and the digital (DGND/DIGND) are isolated from each other on the ground plane. Pads allow the grounds to be tied together directly below the TLV987 IC or at the power supply inputs, thereby providing low-inductive ground connections for return current paths.

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## 1.3 EVM Board Layout

Figures 1−2 through 1−7 show the EVM board layouts.

*Figure 1−2. EVM Top Silkscreen*

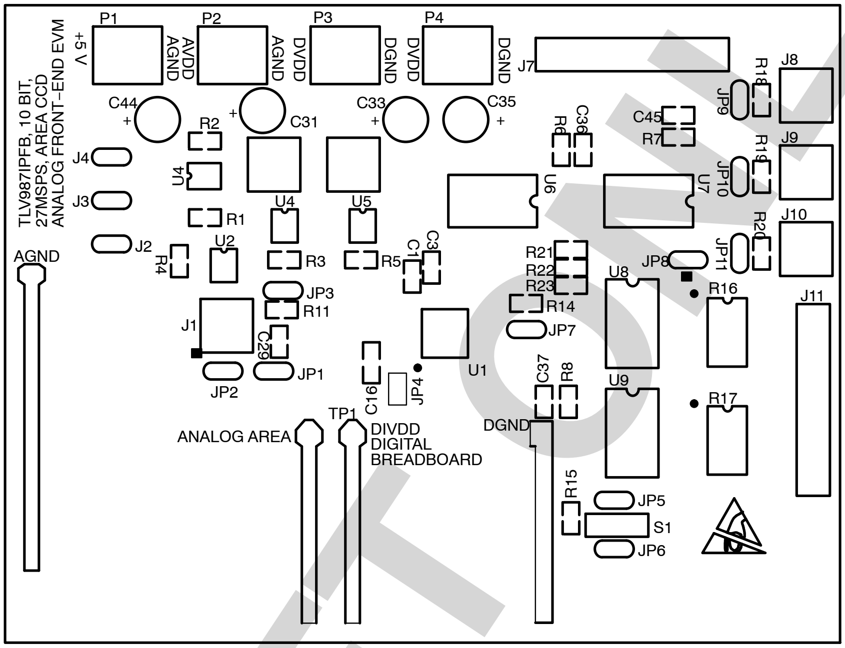

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Figure 1−3. EVM Component Layer

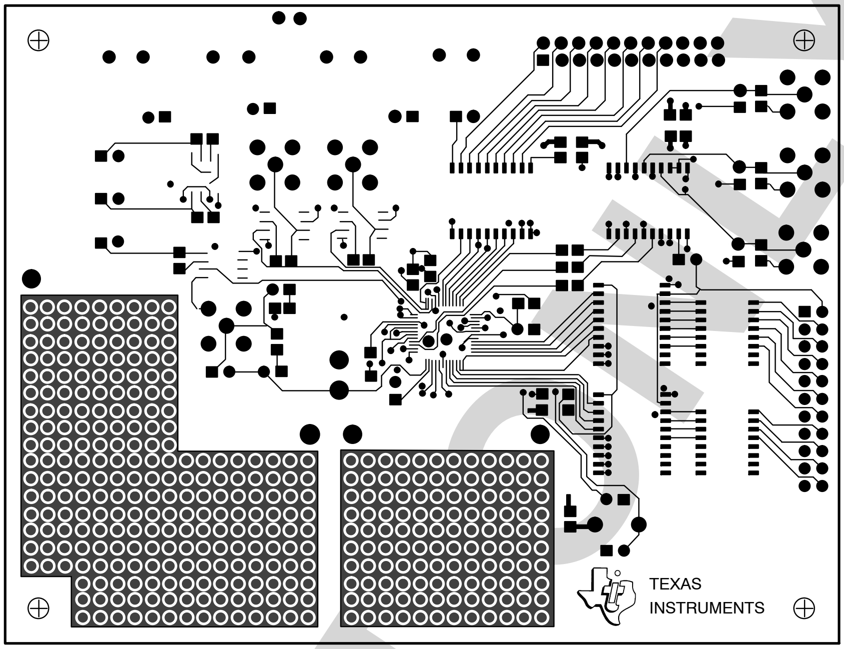

Figure 1−4. EVM Power Plane

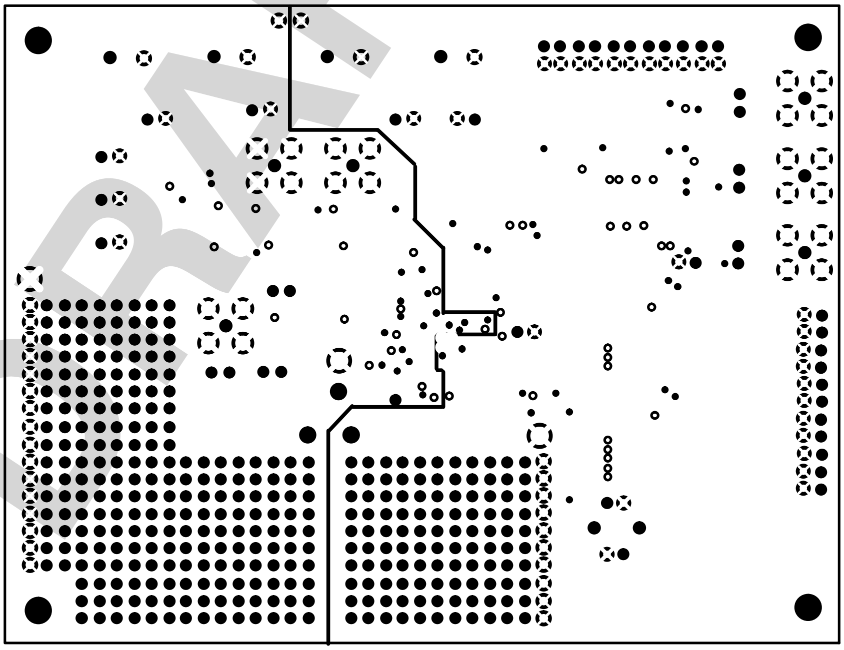

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*Figure 1−5. EVM Power Plane*

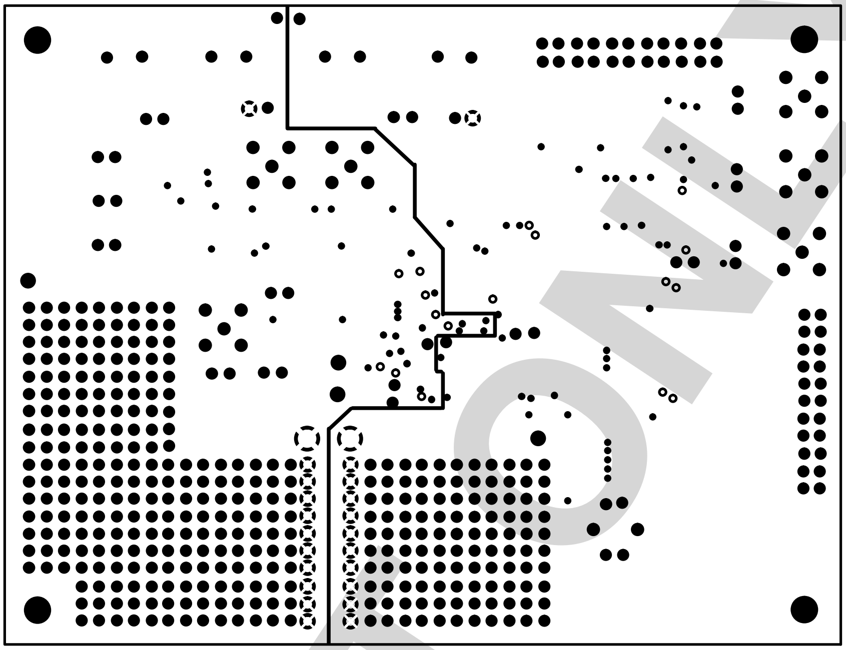

*Figure 1−6. EVM Bottom Silkscreen*

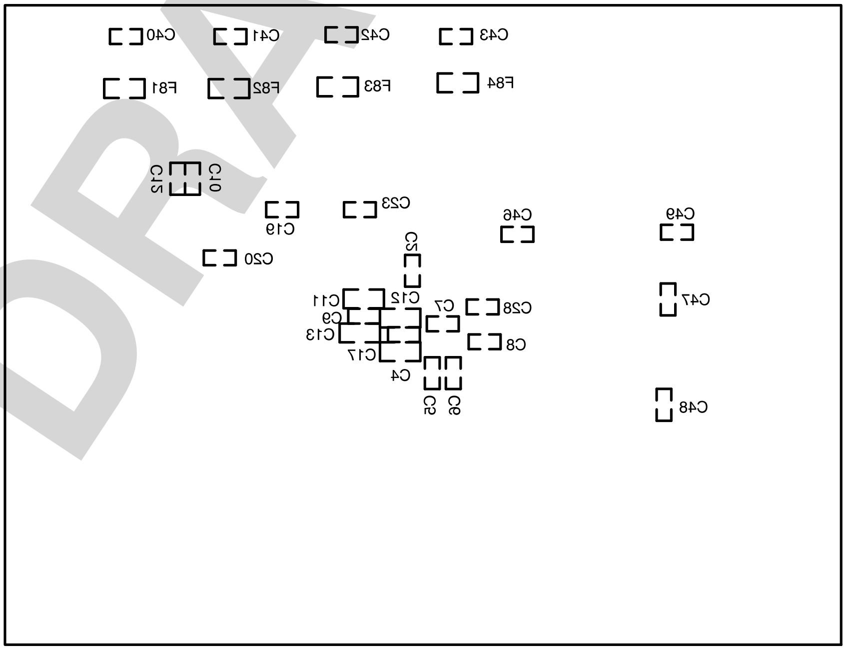

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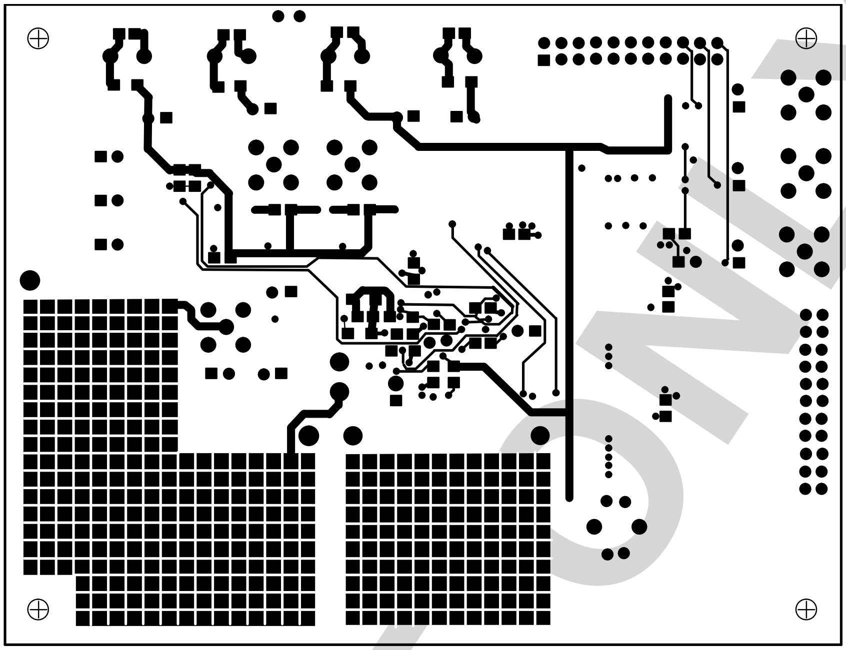
Figure 1−7. EVM Solder Layer



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## Chapter 2

# Analog Input

This chapter describes the EVM analog input.

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## 2.1 Analog Input

Refer to the schematic diagram, Figure 1–1.

The analog input is provided through SMA connector J1. This signal is routed to the DIN pin of the TLV987 by one of three paths:

- ❑ Direct input
- ❑ AC coupled input
- ❑ User supplied input

### 2.1.1 Direct Input

To route the signal from the CCD directly to the DIN pin of the TLV987, install jumper JP1. This provides a 50-Ω load (R11) at the input connector. A termination is required, since unterminated loads such as coaxial cables can provide reactive loads to the inputs.

### 2.1.2 AC Coupled Input

If ac coupling is desired, install jumper JP2 (JP1 open). In addition to the 50-Ω termination, this provides a series 0.1-µF capacitor for coupling ac inputs. This allows the CCD sensor to be connected directly to the J1 input.

### 2.1.3 User Supplied Input Circuit

A breadboarding area allows custom input filters or other signal conditioning circuits to be used. To route the signal from the breadboarding area, open jumpers JP1 and JP2, and connect the requisite circuitry on the breadboard. This connects the DIN SMA to pin 1 of the TLV987.

To prevent excessive signal-path capacitance from degrading the signal quality at high frequencies, only one of the above configurations can be used at one time. Jumper JP3 must be installed to terminate the input with 50 Ω..

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## Chapter 3

# Analog Outputs

This chapter describes the EVM analog outputs.

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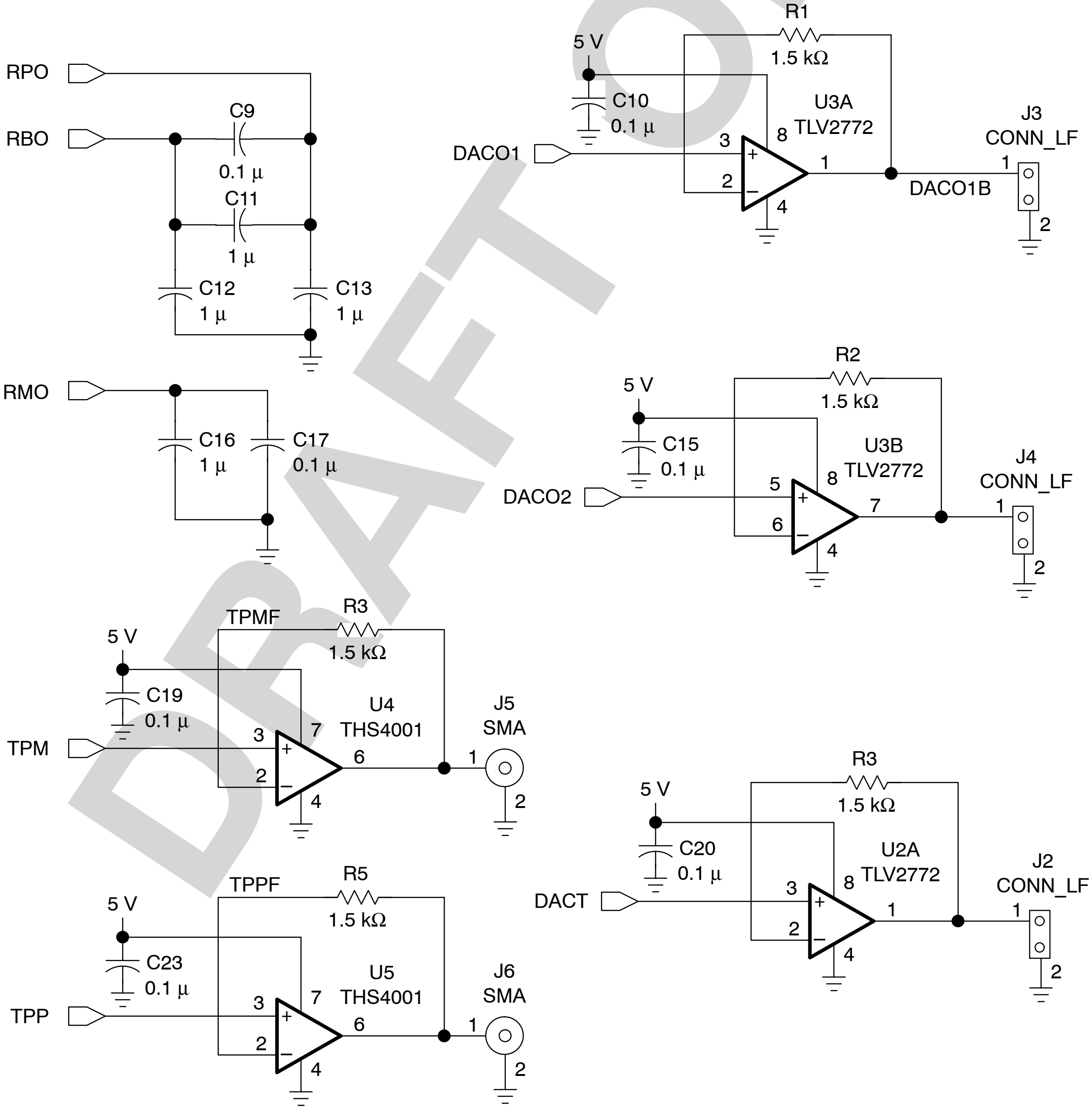
## 3.1 Analog Outputs

Refer to the schematic diagram, Figure 1−1, and the detailed analog output schematics in Figure 3−1.

The outputs of the PGA (TPP and TPM) and the outputs of the DACs (DACO1, DACO2 and DACT) are provided through SMA and vertical pin connectors. High-speed op amps buffer the outputs to provide proper driving capability at the output.

*Figure 3−1. EVM Analog Outputs*



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## Chapter 4

# Digital Inputs/Outputs

This chapter describes the EVM digital inputs and outputs.

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## 4.1 Digital Inputs/Outputs

Figures 4−1 and 4−2 show the EVM digital I/O schematic diagrams. Table 4−1 lists and describes the connectors.

Four buffers (U6−U9) drive input and output digital signals. All high frequency inputs and outputs have series 22-Ω damping resistors. Connector J7 provides the inputs, and connector J11 provides the ADC outputs and the 3-state enable.

Pin 2 of output connector J11 can drive the outputs of U8 and U9 to a high impedance state allowing a bus interface to the external circuitry. A logic 1 applied to pin 2 of J11 will 3-state the outputs of the 74AHC245s.

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*Figure 4−1. EVM Digital I/O Part 1*

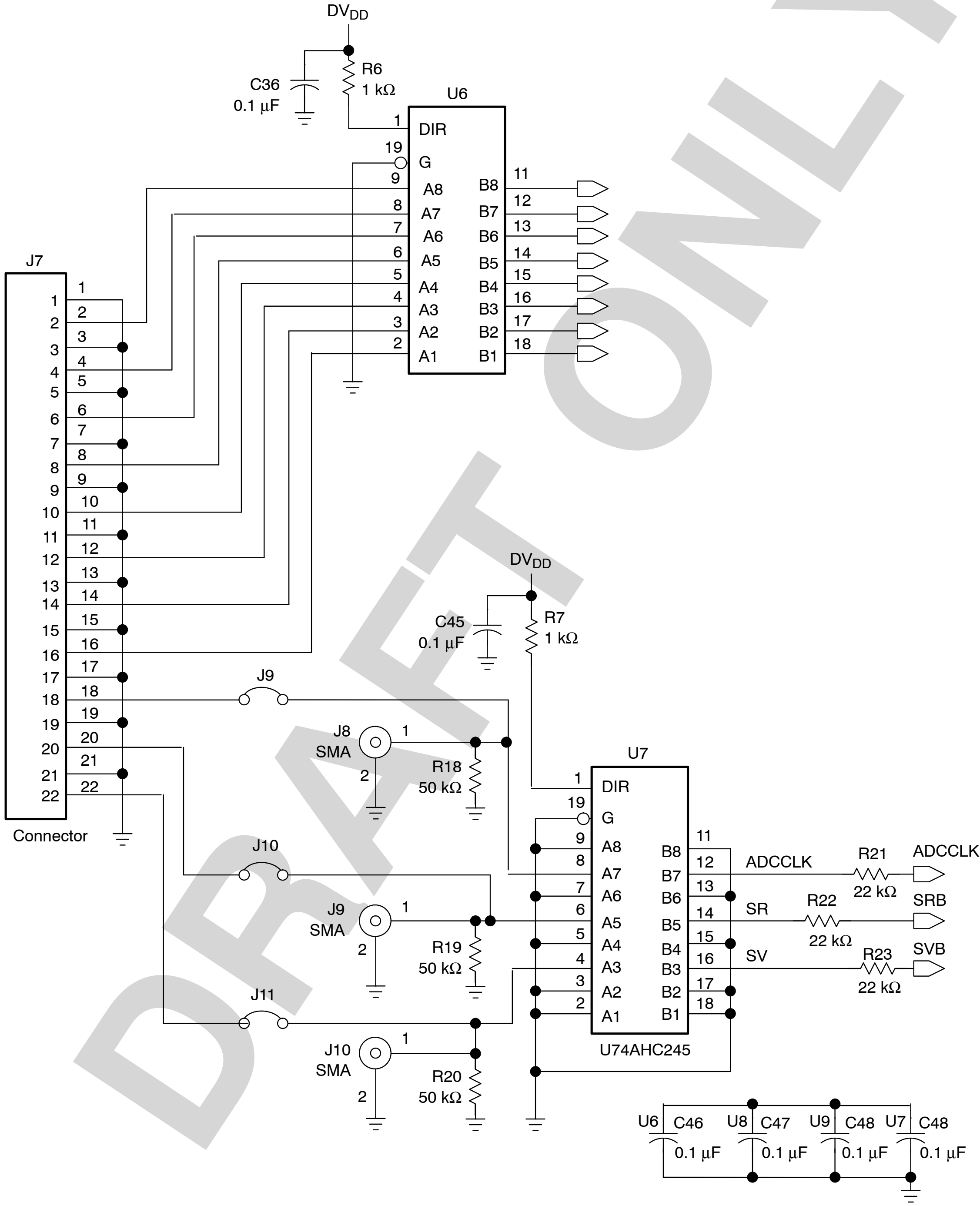

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*Figure 4–2. EVM Digital I/O Part 2*

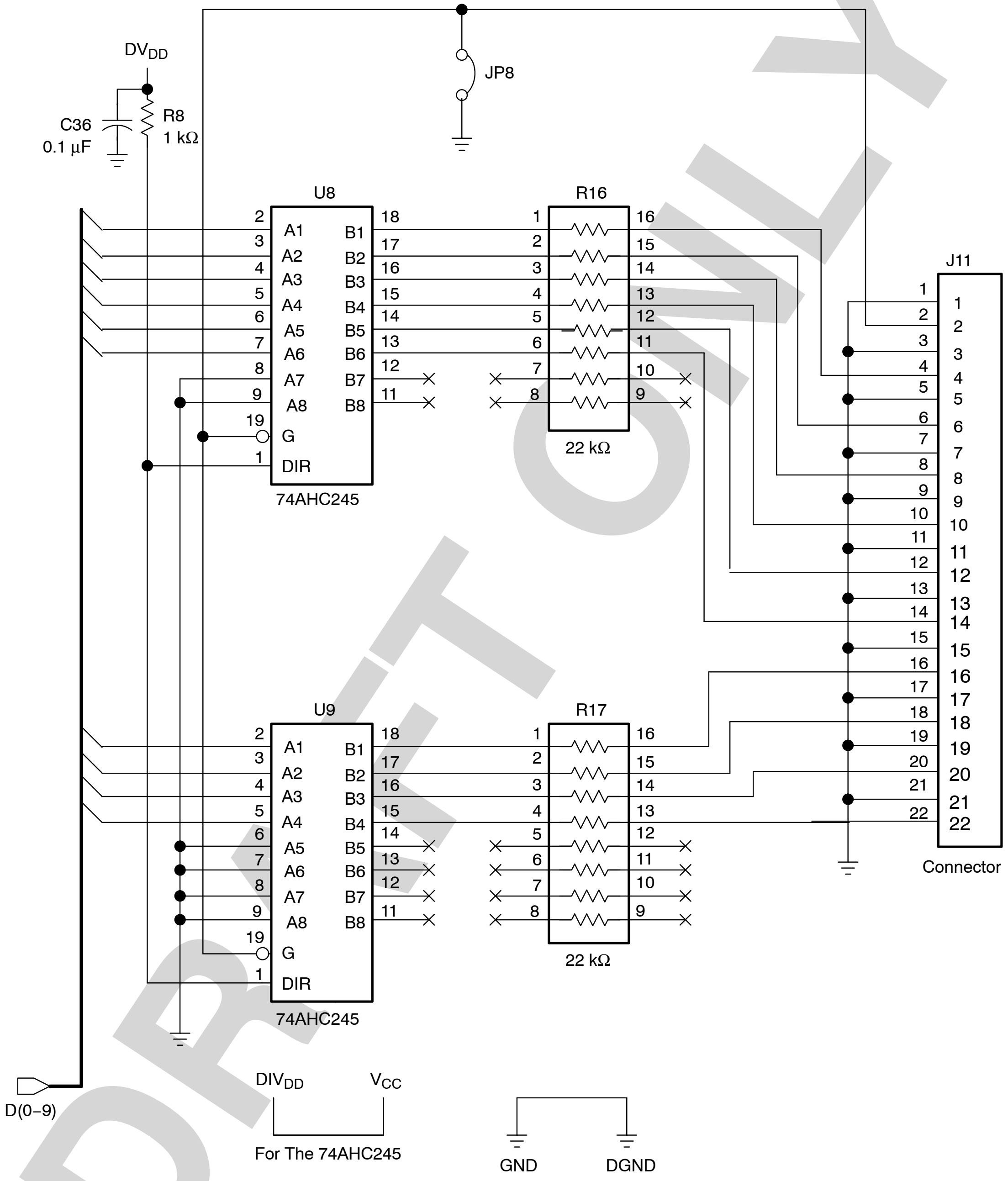

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*Table 4–1. Connector Descriptions*

<table>
<tr><th>Connector</th><th>Description</th></tr>
<tr><td>J1</td><td>Analog signal input from CCD</td></tr>
<tr><td>J2</td><td>Buffered DACT output</td></tr>
<tr><td>J3</td><td>Buffered DACO1 output</td></tr>
<tr><td>J4</td><td>Buffered DACO2 output</td></tr>
<tr><td>J5</td><td>Buffered TPM output (PGA noninverting output or PGA clock)</td></tr>
<tr><td>J6</td><td>Buffered TPP output (PGA inverting output or CDS clock)</td></tr>
<tr><td>J7</td><td>Connector for digital inputs.<br>All odd numbered pins connected to digital ground.
<table>
<tr><th>Pin</th><th>Function</th><th>Pin</th><th>Function</th></tr>
<tr><td>2</td><td>CLAMP</td><td>124</td><td>SDIN</td></tr>
<tr><td>4</td><td>BLKG</td><td>16</td><td>SCLK</td></tr>
<tr><td>6</td><td>$\overline{\text{OBCLP}}$</td><td>18</td><td>ADCCLK (opt)</td></tr>
<tr><td>8</td><td>STBY</td><td>20</td><td>SR (opt)</td></tr>
<tr><td>10</td><td>RESET</td><td>22</td><td>SV (opt)</td></tr>
<tr><td>12</td><td>$\overline{\text{CS}}$</td><td></td><td></td></tr>
</table>
</td></tr>
<tr><td>J8</td><td>ADCCLK input (JP9 needs to be open)</td></tr>
<tr><td>J9</td><td>SRB input (JP10 needs to be open)</td></tr>
<tr><td>J10</td><td>SVB input (JP11 needs to be open)</td></tr>
<tr><td>J11</td><td>Output connector for ADC outputs and 3-state enable input for output buffers.<br>All odd numbered pins are connected to digital ground.
<table>
<tr><th>Pin</th><th>Function</th><th>Pin</th><th>Function</th></tr>
<tr><td>2</td><td>G (3-state enable)</td><td>14</td><td>D4</td></tr>
<tr><td>4</td><td>D9</td><td>16</td><td>D3</td></tr>
<tr><td>6</td><td>D8</td><td>18</td><td>D2</td></tr>
<tr><td>8</td><td>D7</td><td>20</td><td>D1</td></tr>
<tr><td>10</td><td>D6</td><td>22</td><td>D0</td></tr>
<tr><td>12</td><td>D5</td><td></td><td></td></tr>
</table>
</td></tr>
</table>

Jumper JP5 can be removed if external control on the STBY pin is required. The TLV987 can be reset using pushbutton switch S1, which temporarily connects the RESET pin to DVDD. In normal operation, the RESET pin is connected to digital ground.

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## Chapter 5

# Clock Circuit

This chapter describes the EVM clock circuit.

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## 5.1 Clock Circuit

Refer to the schematic diagram, Figure 1–1.

Two external clocks are required for proper operation of the EVM. One clock (ADCCLK) provides the input to the internal ADC. The other (SCLK) is required to synchronize the serial data transfer. These clock sources are provided through the SMA J8 for ADCCLK or through pin 16 of connector J7. The SMA is terminated at 50W **(50W???)**. Noninverting drivers buffer both clocks. ADCCLK also has a series termination to prevent spikes and instability at higher frequencies. The buffers are powered by DIVDD, so the output levels will be dependent on the DIVDD supply.

### 5.1.1 Test Points

Test points TP1 & TP2 provide points to monitor the input signal and the corresponding reference ground. Most of the other signals can be monitored using the corresponding output connectors.

### 5.1.2 Breadboarding Areas

Two breadboarding areas (analog and digital) provide space for user-supplied input/output circuitry. These allow the user to condition the response as desired for a particular application.

### 5.1.3 Summary

The TLV987 EVM provides an easy means for evaluating the programming capabilities and speed of the TI TLV987. Simple ribbon-connector Inputs and outputs make it easy to connect to any logic analyzer.

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## Appendix A

# TLV987 Data Sheet

This appendix contains the data sheet for the TLV987.

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# TLV987
# 3 V, 10-BIT, 27 MSPS, AREA CCD SENSOR PROCESSOR

SLVSXXXX – AUGUST 1998

Package Information

- **10-Bit, 27 MSPS, A/D Converter**
- **Single 3 V Supply Operation**
- **Differential Nonlinearity Error: <±0.5 LSB Typ.**
- **Integral Nonlinearity Error: <±1 LSB Typ.**
- **Programmable Gain Amplifier (PGA) with −3dB to 42dB Gain Range (0.09 dB/step)**
- **Automatic or Programmable Black Level and Offset Calibration**
- **Additional DACs for External Analog Setting**
- **Low Power: 400 mW Typical, 1 mW Power-down Mode**
- **Serial Interface for Register Configuration**
- **Internal Reference Voltages**
- **48-Pin TQFP Package**

## applications

- **Digital Still Camera**
- **Digital Camcorder**
- **Digital Video Camera**

## description

The TLV987 is a highly integrated monolithic analog signal processor/digitizer designed to interface the area charge-coupled device (CCD) sensors in digital camera applications. The TLV987 performs all the analog processing functions necessary to maximize the dynamic range, corrects various errors associated with the CCD sensor, and then digitizes the results with an on-chip high-speed analog-to-digital converter (ADC). The key components of the TLV987 include: input clamp circuitry and a correlated double sampler (CDS), a programmable gain amplifier (PGA) with −3 dB to 42 dB gain range, two internal digital-to-analog converters (DAC) for automatic or programmable optical black level and offset calibration, a 10-bit, 27 MSPS pipeline ADC, a parallel data port for easy microprocessor interface and a serial port for configuring internal control registers, two additional DACs for external system control, and internal reference voltages.

Designed in advanced CMOS process, the TLV987 operates from a single 3 V power supply with a normal power consumption of 400 mW and a 1 mW power-down mode.

Very high throughput rate, single 3 V operation, low power consumption, and fully integrated analog processing circuitry make the TLV987 an ideal CCD sensor interfacing solution for the digital camera applications.

The part is available in a 48-pin TQFP package and is specified over −40°C to 85°C operating temperature range.

**AVAILABLE OPTIONS**

| $T_A$ | PACKAGED DEVICE |
|---|---|
| | TQFP (PFB) |
| −40°C to 85°C | TLV987IPFB |

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## functional block diagram

## Terminal Functions

| Terminal | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| DIN | 1 | I | Input signal from CCD (video channel) |
| PIN | 2 | I | Input signal from CCD (black channel) |
| AVDD2 | 3 | | Analog supply voltage for internal PGA circuits, 3 V |
| AGND2 | 4 | | Analog ground for internal PGA circuits |
| DGND | 5 | | Digital ground |
| DVDD | 6 | | Digital supply voltage, 3 V |
| D0 – D9 | 7–16 | O | 10-bit 3-state ADC output data or offset DACs test data |
| DIVDD | 17 | | Digital interface circuit supply voltage |
| DIGND | 18 | | Digital interface circuit ground |
| AVDD3 | 19 | | Analog supply voltage for internal DAC circuits, 3 V |
| AGND3 | 20 | | Analog ground for internal DAC circuits |
| DACO1 | 21 | O | Digital–to–analog converter output1 |
| DACO2 | 22 | O | Digital–to–analog converter output2 |
| DACT | 23 | O | Mux’ed test output for internal offset DACs |
| OE | 24 | I | Output data enable. Active low. |
| ADCCLK | 25 | I | ADC clock input. |
| SCLK | 26 | I | Serial clock input. This clock synchronizes the serial data transfer. |
| SDIN | 27 | I | Serial data input to configure the internal registers. |
| $\overline{\text{CS}}$ | 28 | I | Chip Select. A logic low on this input enables the TLV987. |
| RESET | 29 | I | Hardware reset input, active high. This signal forces a reset of all internal registers. |
| STBY | 30 | I | Hardware power-down control input, active high |
| OBCLP | 31 | I | Optical black level and offset calibration control input. Active low. |

## Terminal Functions (Continued)

| Terminal NAME | Terminal NO. | I/O | DESCRIPTION |
|---|---|---|---|
| AGND4 | 32 | | Analog ground for internal ADC circuits |
| AVDD4 | 33 | | Analog supply voltage for internal ADC circuits, 3 V |
| TPM | 34 | O | Mux'ed test output: PGA noninverting output or PGA clock |
| TPP | 35 | O | Mux'ed test output: PGA inverting output or CDS clock |
| BLKG | 36 | I | Control input. The SR and SV input signals are disabled when the BLKG is high. |
| AGND5 | 37 | | Analog ground for internal REF circuits |
| RBD | 38 | O | Internal bandgap reference for external decoupling |
| RMD | 39 | O | Ref– output for external decoupling |
| RPD | 40 | O | Ref+ output for external decoupling |
| AVDD5 | 41 | | Analog supply voltage for internal ADC circuits, 3 V |
| VSS | 42 | | Silicon substrate, normally connected to analog ground |
| AVDD1 | 43 | | Analog supply voltage for internal CDS circuits, 3 V |
| AGND1 | 44 | | Analog ground for internal CDS circuits |
| SR | 45 | I | CCD reference level sample clock input |
| SV | 46 | I | CCD signal level sample clock input |
| CLAMP | 47 | I | CCD signal clamp control input |
| CLREF | 48 | O | Clamp reference voltage for external decoupling |

## absolute maximum ratings over operating free-air temperature (unless otherwise noted)[†]

| | |
|---|---|
| Supply voltage, AVDD, DVDD, DIVDD | −0.3 V to 6.5 V |
| Analog input voltage range | −0.3 V to AVDD+0.3 V |
| Digital input voltage range | −0.3 V to DVDD+0.3 V |
| Operating virtual junction temperature range, $T_J$ | −40°C to 150°C |
| Operating free-air temperature range, $T_A$ | 0°C to 70°C |
| Storage temperature range, $T_{stg}$ | −65°C to 150°C |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds | 260°C |

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## recommended operating conditions

### power supplies

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Analog supply voltage | AVDD | 2.7 | 3 | 3.3 | V |
| Digital supply voltage | DVDD | 2.7 | 3 | 3.3 | V |

## recommended operating conditions (continued)

### digital inputs

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| High-level input voltage, $V_{IH}$ | DIVDD = 3 V | 0.8 DIVDD | | | V |
| Low-level input voltage, $V_{IL}$ | DIVDD = 3 V | | | 0.2 DIVDD | V |
| Input ADCCLK frequency | DVDD = 3 V | | 27 | | MHz |
| ADCCLK pulse duration, clock high, $t_{w(MCLKH)}$ | DVDD = 3 V | | 18.5 | | ns |
| ADCCLK pulse duration, clock low, $t_{w(MCLKL)}$ | DVDD = 3 V | | 18.5 | | ns |
| Input SCLK frequency | DVDD = 3 V | | 16 | | MHz |
| SCLK pulse duration, clock high, $t_{w(SCLKH)}$ | DVDD = 3 V | | 31.3 | | ns |
| SCLK pulse duration, clock low, $t_{w(SCLKL)}$ | DVDD = 3 V | | 31.3 | | ns |

## electrical characteristics over recommended operating free-air temperature range, $T_A$ = 25°C, AVDD = DVDD=3 V, ADCCLK=27 MHz (unless otherwise noted)

### total device

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| AVDD operating current | | | 105 | | mA |
| DVDD operation current | | | 28 | | mA |
| Device power consumption | | | 400 | | mW |
| Power consumption in powerdown mode | | | 1 | | mW |

### analog-to-digital converter (ADC)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| | ADC Resolution | | | 10 | | Bits |
| INL | Integral nonlinearity | AVDD=DVDD= 2.7 V – 3.3 V | | ±1 | ±2 | :SB |
| DNL | Differential nonlinearity | AVDD=DVDD= 2.7 V – 3.3 V | | ±0.5 | ±0.75 | LSB |
| | No missing codes | | | | | |
| | Full scale input span | | | 2 | | $V_{p-p}$ |
| | Conversion rate | | | | 27 | MHz |
| | ADC output latency | | | 5 | | CLK cycles |
| SINAD | Signal–to–noise ratio + distortion | 0 dB gain, $f_{IN}$ = 1 MHz | | 57 | | dB |

### correlated double sampler (CDS) and programmable gain amplifier (PGA)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| CDS and PGA sample rate | | | | 27 | MHz |
| CDS full scale input span | Single-ended input | | 1 | 1.4 | V |
| Input capacitance of CDS | | | 4 | | pF |
| Minimum PGA gain | | −4 | −3 | −2 | dB |
| Maximum PGA gain | | 39 | 42 | 44 | dB |
| PGA gain resoultion | | | 0.09 | | dB |
| PGA programming code resolution | 8-bit monotonic gain control | | 9 | | Bits |

## electrical characteristics over recommended operating free-air temperature range, $T_A$ = 25°C, AVDD = DVDD=3 V, ADCCLK=27 MHz (unless otherwise noted) (continued)

### internal digital-to-analog converters (DAC) for offset correction

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| | DAC resolution | | | 8 | | Bits |
| INL | Integral nonlinearity | | | ±1 | | LSB |
| DNL | Differential nonlinearity | | | ±0.5 | | LSB |
| | Output settling time | To 1% accuracy | | 80 | | ns |

### output digital-to-analog converters (DAC)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| | DAC resolution | | | 8 | | Bits |
| INL | Integral nonlinearity | | | ±1 | | LSB |
| DNL | Differential nonlinearity | | | ±0.5 | | LSB |
| | Output voltage range | | 0 | | 2 | V |
| | Output settling time | 5 pF external load, To 1% accuracy | | 3 | | µs |

### reference voltages

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| | Internal bandgap voltge reference | | 1.43 | 1.50 | 1.58 | V |
| | Temperature coefficient | | | 100 | | ppm/°C |
| | Voltage reference noise | | | 0.5 | | LSB |
| | ADC Ref+ | Externally decoupled | | 2 | | V |
| | ADC Ref− | Externally decoupled | | 1 | | V |

### digital specifications

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **Logic Inputs** | | | | | | |
| $I_{IH}$ | High-level input current | DIVDD = 3 V | −10 | | 10 | µA |
| $I_{IL}$ | Low-level input current | DIVDD = 3 V | −10 | | 10 | µA |
| $C_i$ | Input capacitance | | | 5 | | pF |
| **Logic Outputs** | | | | | | |
| $V_{OH}$ | High-level output voltage | $I_{OH}$ = 50 µA, DIVDD = 3 V | | DIVDD = −0.4 | | V |
| $V_{OL}$ | Low-level output voltage | $I_{OL}$ = 50 mA, DIVDD = 3 V | | | | V |
| $I_{OZ}$ | High-impedance-state output current | | −10 | | 10 | µA |
| $C_o$ | Output capacitance | | | 5 | | pF |

## typical operation timing diagram

## serial interface timing diagram

## internal register definition

### serial input data format

| DI15 | DI14 | DI13 | DI12 | DI11 | DI10 | DI9 | DI8 | DI7 | DI6 | DI5 | DI4 | DI3 | DI2 | DI1 | DI0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| X | X | A3 | A2 | A1 | A0 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

| **A3** | **A2** | **A1** | **A0** | | **D9–D0** |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | Control register | 10-bit data to be written into the selected register |
| 0 | 0 | 0 | 1 | PGA gain register | |
| 0 | 0 | 1 | 0 | Output DAC1 register | |
| 0 | 0 | 1 | 1 | Output DAC2 register | |
| 0 | 1 | 0 | 0 | Coarse offset DAC | |
| 0 | 1 | 0 | 1 | Fine offset DAC | |
| 0 | 1 | 1 | 0 | Digital Vb register (set reference code level at the ADC output during the optical black interval) | |
| 0 | 1 | 1 | 1 | Optical black register (set the number of clack pixels per line [N] and number of lines [L] to average) | |
| 1 | 0 | 0 | 0 | Test register | |

## internal register definition (continued)

### control register format

| D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| STBY | X | X | X | X | X | X | X | X | SRT |

### control register description

| BIT | NAME | DESCRIPTION |
|---|---|---|
| D9 | STBY | Device standby control: 1 = standby, 0 = active |
| D8–D1 | | Reserved |
| D0 | SRT | Software reset, 1 – reset system to the default settings |

### PGA register format

| D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| X | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |

### output DAC1 and DAC2 registers format

| D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| X | X | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |

The output DAC register default value = XX00000000

### coarse offset DAC register format

| D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| BCAC | SIGN | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |

### coarse offset DAC register description

| BIT | NAME | DESCRIPTION |
|---|---|---|
| D9 | BCAC | 0 = Auto calibration (default), 1 = Bypass auto calibration |
| D8 | SIGN | Coarse DAC sign bit |
| D7–D0 | | Coarse DAC control data when the D9 is set at 1 |

### fine offset DAC register format

| D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| BFAC | SIGN | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |

### fine offset DAC register description

| BIT | NAME | DESCRIPTION |
|---|---|---|
| D9 | BCAC | 0 = Auto calibration (default), 1 = Bypass auto calibration |
| D8 | SIGN | Fine DAC sign bit |
| D7–D0 | | Fine DAC control data when the D9 is set at 1 |

### digital Vb (optional black level) register format

| D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |

Auto calibration will correct the total circuit offset and optical black offset and set this value at the ADC’s output during optical black interval. The Vb register default value = 40 Hex.

## internal register definition (continued)

### optical black calibration register format

| D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| X | SD1 | SD0 | LN3 | LN2 | LN1 | LN0 | PN2 | PN1 | PN0 |

### optical black calibration register description

| BIT | NAME | DESCRIPTION |
|---|---|---|
| D9 | | Reserved |
| D8, D7 | SD1, SD0 | Digital output control (data presented at pin7−pin16)<br>SD1 SD0<br>0 0 ADC output (default)<br>0 1 ADC output<br>1 0 Auto−calibrated coarse DAC value (for test)<br>1 1 Auto−calibrated fine DAC value (for test) |
| D6−D3 | LN3−LN0 | Number of black lines for moving average = $2^L$<br>The L can be 0, 1, 2, 3, 4, 5, 6, 7, and 8. Or number of lines can be 1 (default), 2, 4, 8, 16, 32, 64, 128, and 256.<br>The maximum number of lines is 256 even if L>8. |
| D2−D0 | PN2−PN0 | Number of black pixels per line to average = $2^N$<br>The N can be 0, 1, 2, 3, 4, 5, and 6. Or number of pixels per line can be 1, 2, 4, 8 (default), 16, 32, and 64.<br>The maximum number of pixels per line is 64 even if N>6. |

### test register format

| D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| X | X | X | X | TB5 | TB4 | TB3 | TB2 | TB1 | TB0 |

### test register description

| BIT | NAME | DESCRIPTION |
|---|---|---|
| D5, D4 | TB5, TB4 | Test outputs (pin 34/35 – TPM/TPP) control:<br>TB5 TB4<br>0 0 or 1 High impedance outputs<br>1 0 TPP = internal CDS clock, TPM = PGA clock<br>1 1 PGA inverting output at pin TPM,<br>PGA non-inverting output at pin TPP |
| D3 | TB3 | 1 – use external reference, power down internal reference<br>0 – use internal reference. |
| D2 | TB2 | 1 – CDS block bypassed, 0 – CDS enabled |
| D1, D0 | TB1, TB0 | Test output (pin 23 – DACT) control for offset DACs:<br>TB1 TB0<br>0 0 or 1 High impedance outputs<br>1 0 DACT = coarse offset DAC output<br>1 1 DACT = fine offset DAC output |

## Hdr:h0 (TEXT STRING IN FRAME—ENTER IN ALL CAPS, CENTER TO FRAME TOP & BOTTOM)