User's Guide

TPS5430 and TPS5431 Step-Down Converter Evaluation Module User's Guide

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1 Introduction

This user's guide contains background information for the TPS5430 and TPS5431 as well as support documentation for the TPS5430EVM-173 evaluation module (HPA173-001) and the TPS5431EVM-173 evaluation module (HPA173-002) . Also included are the performance specifications, the schematic, and the bill of materials for the TPS5430EVM-173 and the TPS5431EVM-173.

1.1 Background

The TPS5430 and TPS5431 dc/dc converters are designed to provide up to a 3-A output from an input voltage source of 5.5 V to 36 V (TPS5430) or 5.5 V to 23 V (TPS5431EVM-173). Rated input voltage and output current range for the evaluation module is given in Table 1-1. This evaluation module is designed to demonstrate the small printed-circuit-board areas that may be achieved when designing with the TPS5430 and TPS5431 regulators. The switching frequency is internally set at a nominal 500 kHz. The high-side MOSFET is incorporated inside the TPS5430/31 package along with the gate drive circuitry. The low drain-to-source on resistance of the MOSFET allows the TPS5430/31 to achieve high efficiencies and helps keep the junction temperature low at high output currents. The compensation components are provided internal to the integrated circuit (IC), whereas an external divider allows for an adjustable output voltage. Additionally, the TPS5430/31 provides an enable input. The absolute maximum input voltage is 38 V for the TPS5430EVM-173 and 25 V for the TPS5431EVM-173 .

Table 1-1. Input Voltage and Output Current Summary

EVM	INPUT VOLTAGE RANGE	OUTPUT CURRENT RANGE
TPS5430EVM-173	VIN = 10 V to 35 V	0 A to 3 A
TPS5431EVM-173	VIN = 9 V to 21 V	0 A to 3 A

1.2 Performance Specification Summary

A summary of the TPS5430EVM-173 performance specifications is provided in Table 1-2. Specifications are given for an input voltage of VIN = 15 V and an output voltage of 5 V, unless otherwise specified. The TPS5430EVM-173 is designed and tested for VIN = 10 V to 35 V. The ambient temperature is 25°C for all measurements, unless otherwise noted.

Table 1-2. TPS5430EVM-173 and TPS5431EVM-173 Performance Specification Summary

SPECIFICATION		TEST CONDITIONS		MIN	TYP	MAX	UNIT
VIN voltage range	TPS5430EVM-173			10	15	35	V
	TPS5431EVM-173			9	15	21	
Output voltage set point					5.0		V
Output current range		V_{IN} = 3.3 V		0		3	A
Line regulation	TPS5430EVM-173	I_O = 0 A – 3 A, VIN = 10 V – 35 V			±0.07%		
	TPS5431EVM-173	I_O = 0 A – 3 A, VIN = 9 V – 21 V			±0.04%		
Load regulation	TPS5430EVM-173	VIN = 15 V, I_O = 0 A to 3 A			±0.03%		
	TPS5431EVM-173				±0.05%		
Load transient response	TPS5430EVM-173	I_O = 0.75 A to 2.25 A	Voltage change		–50		mV
			Recovery time		150		µs
	TPS5431EVM-173		Voltage change		–40		mV
			Recovery time		150		µs
	TPS5430EVM-173	I_O = 2.25 A to 0.75 A	Voltage change		50		mV
			Recovery time		150		µs
	TPS5431EVM-173		Voltage change		40		mV
			Recovery time		150		µs

Table 1-2. TPS5430EVM-173 and TPS5431EVM-173 Performance Specification Summary (continued)

SPECIFICATION		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Loop bandwidth	TPS5430EVM-173	VIN = 25 V, I_O = 1 A		25.0		kHz
	TPS5431EVM-173	VIN = 15 V, I_O = 1 A		23.9		
Phase margin	TPS5430EVM-173	VIN = 25 V , I_O = 1 A		50°		
	TPS5431EVM-173	VIN = 15 V, I_O = 1 A		51°		
Input ripple voltage	TPS5430EVM-173	I_O = 3 A		255	300	mVpp
	TPS5431EVM-173			295	350	
Output ripple voltage	TPS5430EVM-173	I_O = 3 A		20		mVpp
	TPS5431EVM-173			20		
Output rise time				8		ms
Operating frequency				500		kHz
Max efficiency	TPS5430EVM-173	VIN = 10 V, V_O = 5 V, I_O = 0.75 A		93.6%		
	TPS5431EVM-173	VIN = 9 V, V_O = 5 V, I_O = 0.75 A		94.0%		

1.3 Modifications

These evaluation modules are designed to demonstrate the small size that can be attained when designing with the TPS5430 and TPS5431. A few changes can be made to this module.

1.3.1 Output Voltage Set Point

To change the output voltage of the EVMs, it is necessary to change the value of resistor R2. Changing the value of R2 can change the output voltage above 1.25 V. The value of R2 for a specific output voltage can be calculated using Equation 1.

$$R2 = 10\ k\Omega \times \frac{1.221\ V}{V_O - 1.221\ V} \quad (1)$$

Table 1-3 lists the R2 values for some common output voltages. Note that VIN must be in a range so that the minimum on-time is greater than 200 ns, and the maximum duty cycle is less than 87%. The values given in Table 1-3 are standard values, not the exact value calculated using Equation 1.

Table 1-3. Output Voltages Available

Output Voltage (V)	R_2 Value (kΩ)
1.8	21.5
2.5	9.53
3.3	5.90
5	3.24

2 Test Setup and Results

This section describes how to properly connect, set up, and use the TPS5430EVM-173 and TPS5431EVM-173 evaluation modules. The section also includes test results typical for the evaluation modules and covers efficiency, output voltage regulation, load transients, loop response, output ripple, input ripple, and startup.

2.1 Input/Output Connections

The TPS5430EVM-173 and TPS5431EVM-173 are provided with input/output connectors and test points as shown in Table 2-1. A power supply capable of supplying 3 A must be connected to J1 through a pair of 20 AWG wires. The load must be connected to J3 through a pair of 20 AWG wires. The maximum load current capability should be 3 A. Wire lengths must be minimized to reduce losses in the wires. Test-point TP1 provides a place to monitor the VIN input voltages with TP2 providing a convenient ground reference. TP3 is used to monitor the output voltage with TP4 as the ground reference.

Table 2-1. EVM Connectors and Test Points

Reference Designator	Function
J1	VIN (see Table 1-1 for Vin range)
J2	OUT, 5 V at 3 A maximum
JP1	2-pin header for enable. Connect EN to ground to disable, open to enable.
TP1	VIN test point at VIN connector
TP2	GND test point at VIN
TP3	Output voltage test point at OUT connector
TP4	GND test point at OUT connector
TP5	Test point between voltage divider network and R3. Used for loop response measurements.
TP6	PH test point

2.2 Efficiency

The efficiency for both EVMs peak at a load current of about 0.75 A and then decrease as the load current increases towards full load. Figure 2-1 shows the efficiency for the TPS5430EVM-173 at an ambient temperature of 25°C.

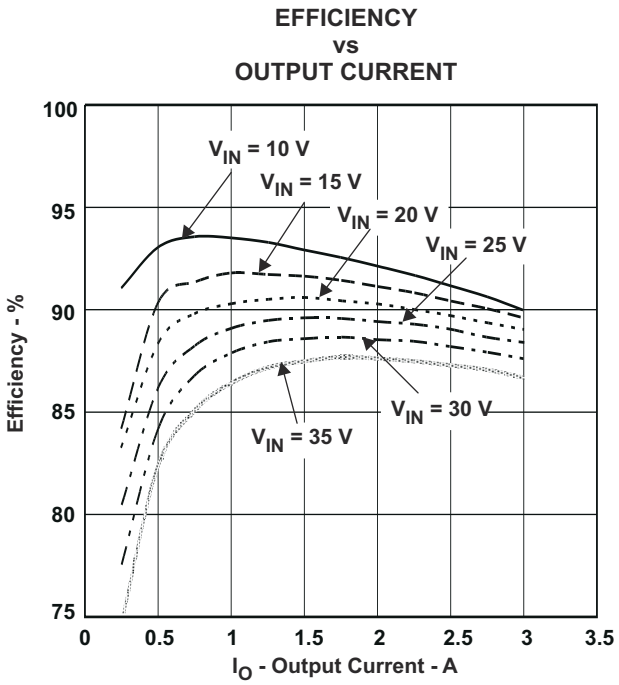

Figure 2-1. TPS5430 Efficiency

Figure 2-2 shows the efficiency for the TPS5431EVM-173 at an ambient temperature of 25°C.

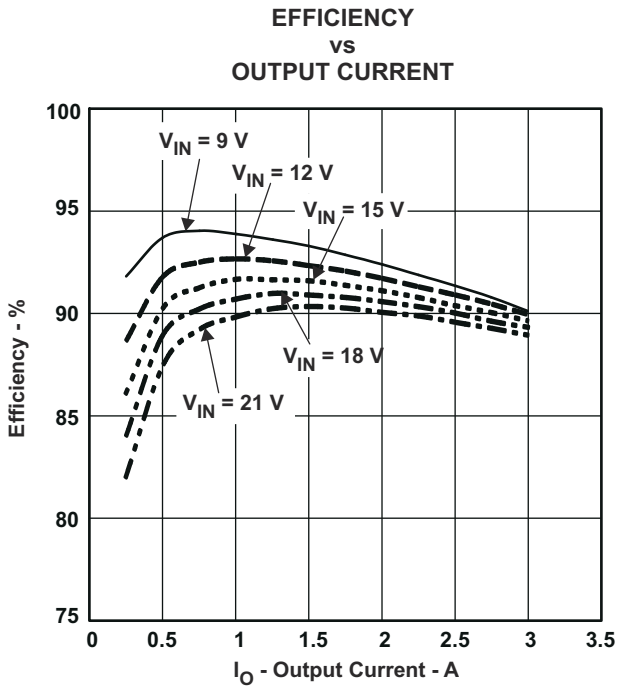

Figure 2-2. TPS5431 Efficiency

The efficiency is lower at higher ambient temperatures, due to temperature variation in the drain-to-source resistance of the MOSFETs.

2.3 Output Voltage Load Regulation

The load regulation for the TPS5430EVM-173 and TPS5431EVM-173 are shown in Figure 2-3 and Figure 2-4.

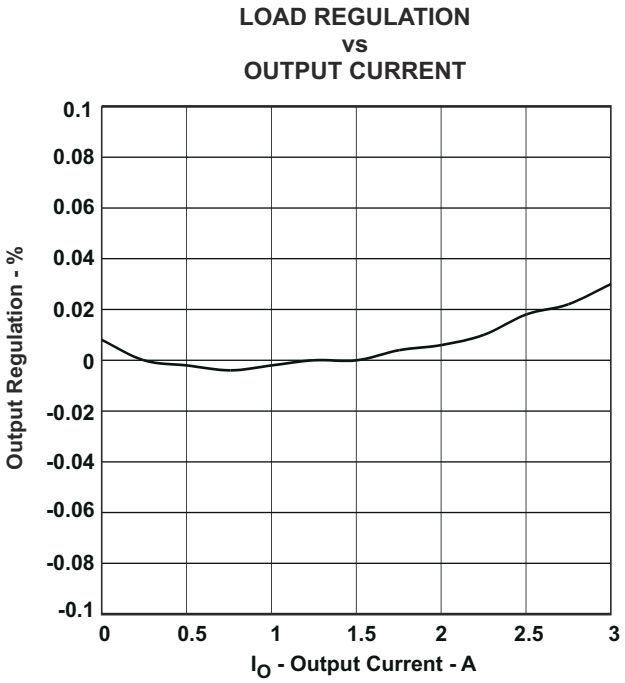

Figure 2-3. TPS5430 Load Regulation

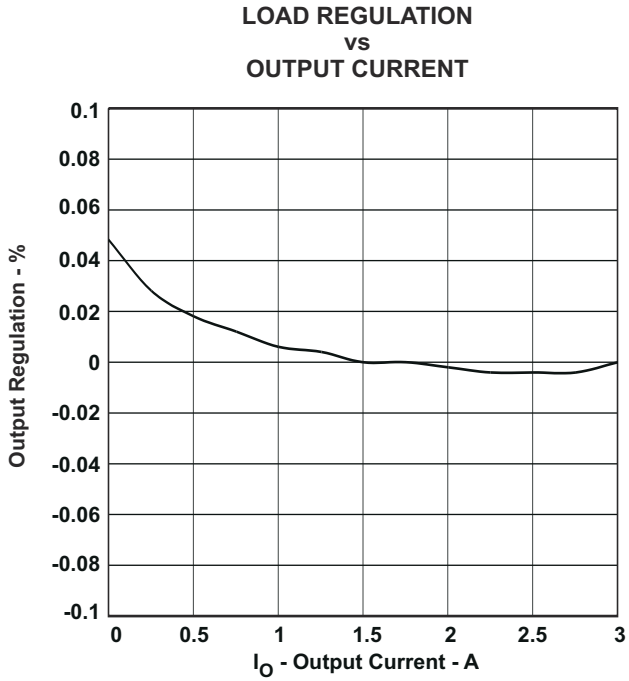

Figure 2-4. TPS5431 Load Regulation

Measurements are given for an ambient temperature of 25°C.

2.4 Output voltage Line Regulation

The load regulation for the TPS5430EVM-173 and TPS54310EVM-173 are shown in Figure 2-5 and Figure 2-6.

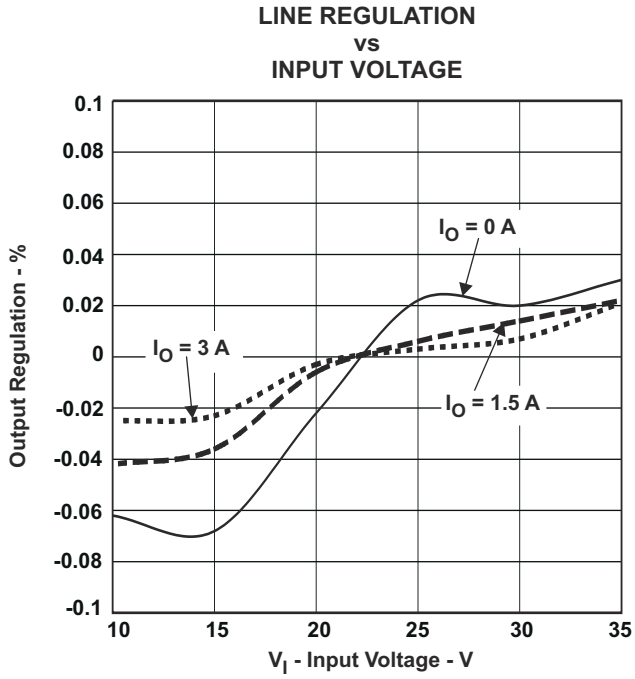

Figure 2-5. TPS5430 Line Regulation

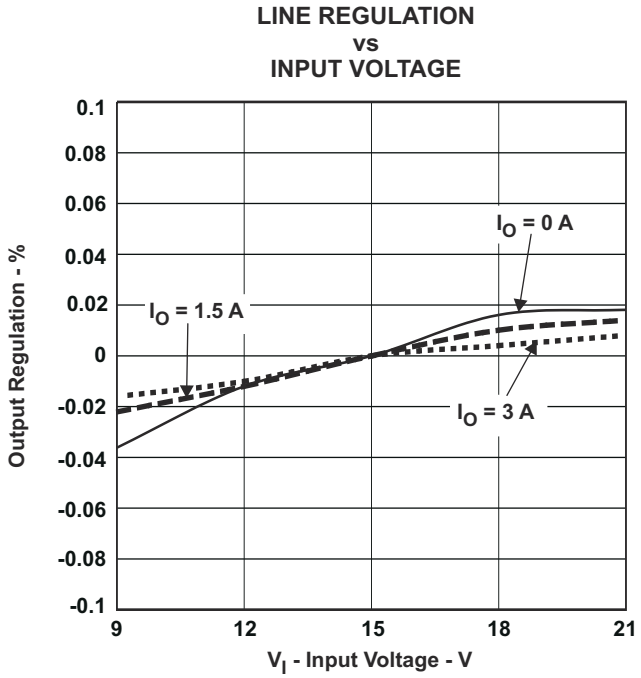

Figure 2-6. TPS5431 Line Regulation

2.5 Load Transients

The TPS5430EVM-173 and TPS5431EVM-173 response to load transients is shown in Figure 2-7 and Figure 2-8. The current step is from 25% to 75% of maximum rated load. Total peak-to-peak voltage variation is as shown, including ripple and noise on the output.

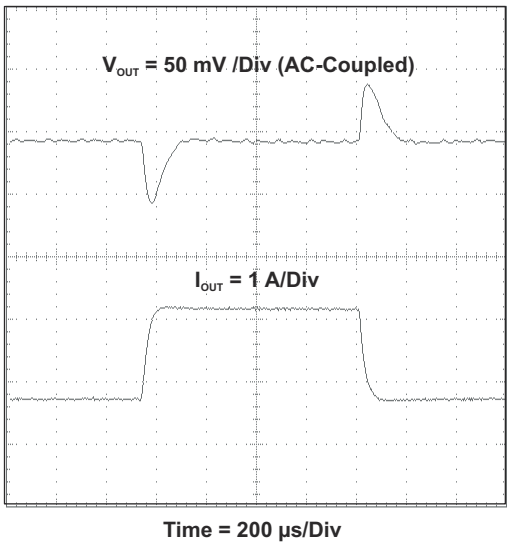

Figure 2-7. PS5430 Transient Response

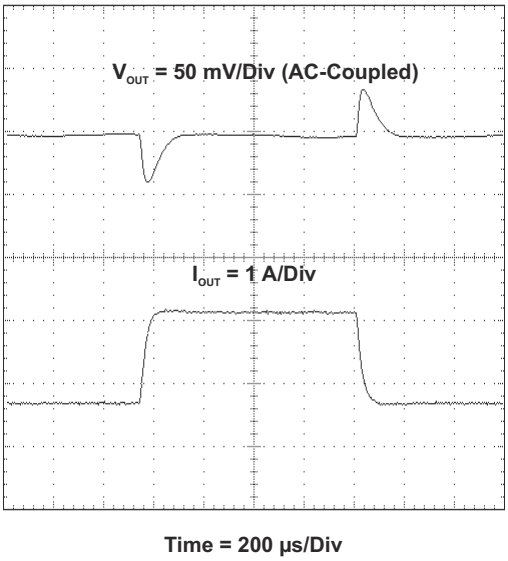

Figure 2-8. TPS5431 Transient Response

2.6 Loop Characteristics

The TPS5430EVM-173 and TPS5431EVM-173 loop-response characteristics are shown in Figure 2-9 and Figure 2-10. Gain and phase plots are shown for VIN voltage of 25 V for the TPS5430EVM-173 and 15 V for the TPS5431EVM-173. Load current for both measurements is 1 A.

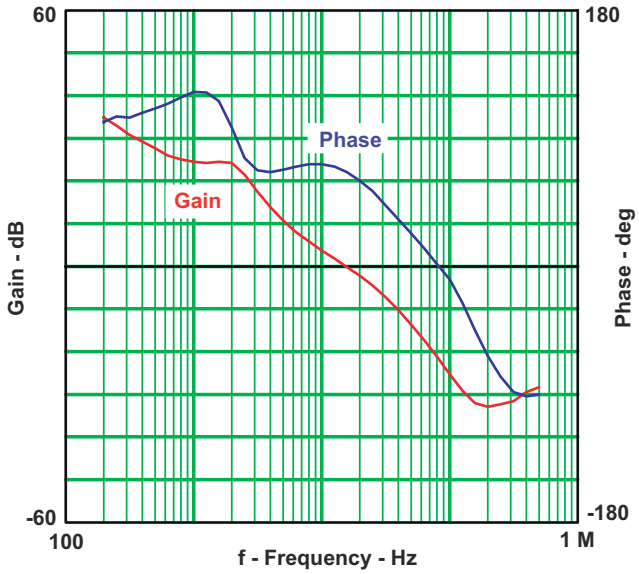

Figure 2-9. TPS5430 Loop Response

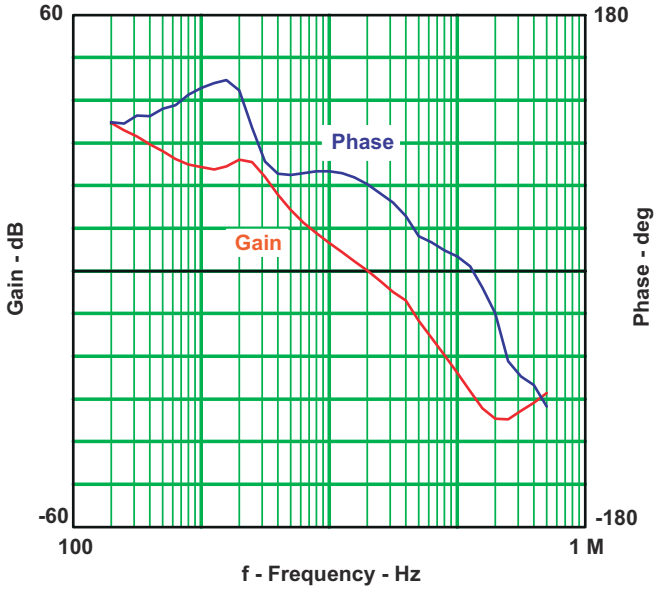

Figure 2-10. PS5431 Loop Response

2.7 Output Voltage Ripple

The TPS5430EVM-173 and TPS5431EVM-173 output voltage ripple is shown in Figure 2-11 and Figure 2-12 . The output current is the rated full load of 3 A. Voltage is measured directly across output capacitors.

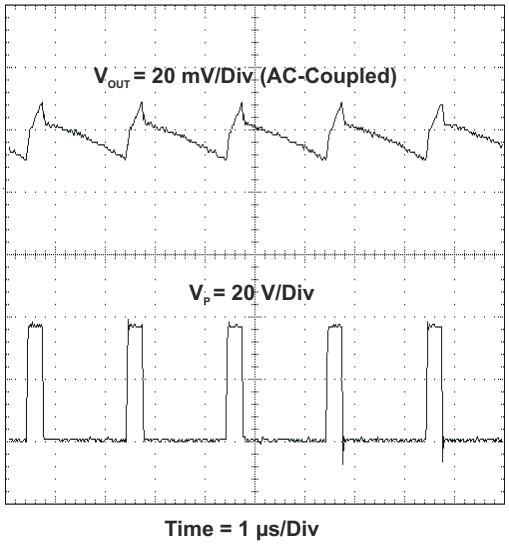

Figure 2-11. TPS5430 Output Ripple

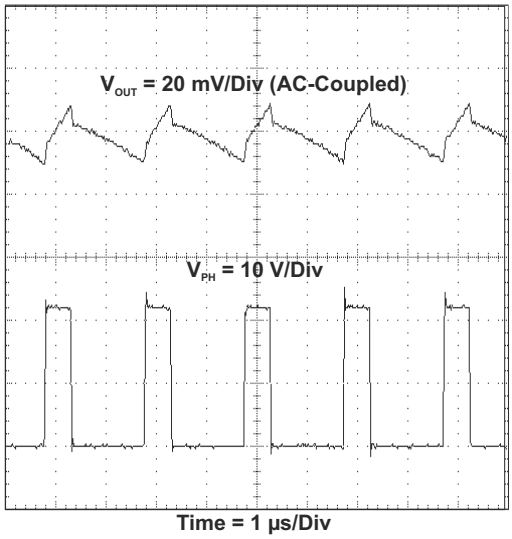

Figure 2-12. PS5431 Output Ripple

2.8 Input Voltage Ripple

The TPS5430EVM-173 and TPS5431EVM-173 input voltage ripple is shown in Figure 2-13 and Figure 2-14. The output current for each device is at full rated load of 3 A.

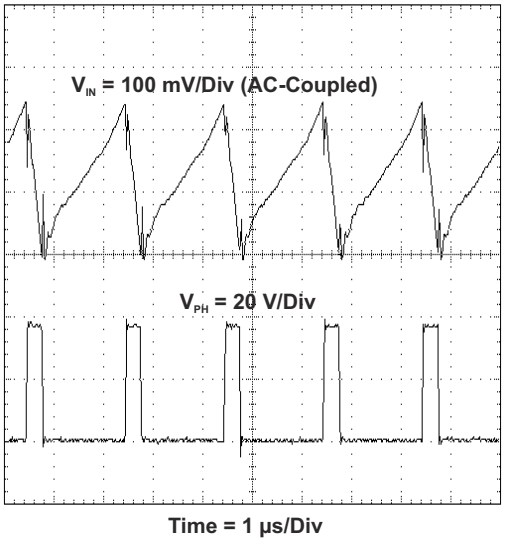

Figure 2-13. TPS5430 Input Ripple

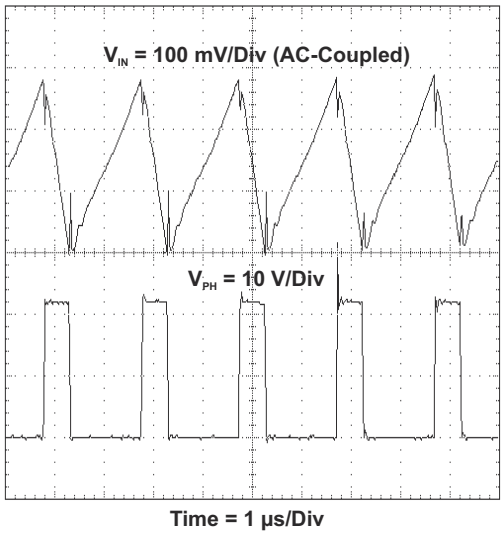

Figure 2-14. TPS5431 Input Ripple

2.9 Powering Up

The start-up waveform is shown in Figure 2-15. The top trace shows ENA, and the bottom trace shows Vout. Initially, the output is inhibited by using a jumper at JP1 to tie EN to GND. When the jumper is removed, ENA is released. When the ENA voltage reaches the enable-threshold voltage of 1.06 V, the start-up sequence begins and the internal reference voltage begins to ramp up at the internally set rate towards 1.221 V and the output voltage ramps up to the externally set value of 5 V. The start-up waveform is the same for both the TPS5430EVM-173 and the TPS5431EVM-173.

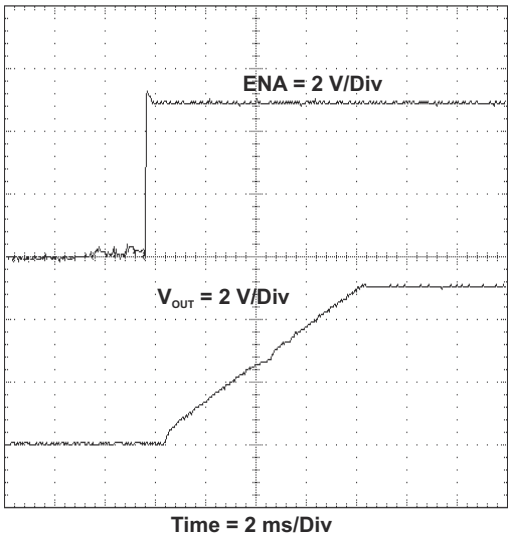

Figure 2-15. TPS5430 and TPS5431 Start-Up

3 Board Layout

This section provides a description of the TPS5430EVM-173 and TPS5431EVM-173 board layout and layer illustrations.

3.1 Layout

The board layout for the TPS5430EVM-173 and TPS5431EVM-173 is shown in Figure 3-1 through Figure 3-3. Both EVM circuits use the same printed-circuit board (HPA173). The topside layer of the EVM is laid out in a manner typical of a user application. The top and bottom layers are 2-oz. copper.

The top layer contains the main power traces for VIN, OUT, and VPHASE. Also on the top layer are connections for the remaining pins of the TPS5430 and a large area filled with ground. The bottom layer contains ground and signal routes for the ENA feature. The top and bottom and internal ground traces are connected with multiple vias placed around the board including four vias directly under the TPS5430 device to provide a thermal path from the PowerPAD™ land to ground.

The input decoupling capacitor (C1) and bootstrap capacitor (C2) are all located as close to the IC as possible. In addition, the voltage set-point resistor divider components are also kept close to the IC. The voltage divider network ties to the output voltage at the point of regulation, the copper Vout trace past the output capacitor C3. For the TPS5430, an additional input bypass capacitor (C4) is required.

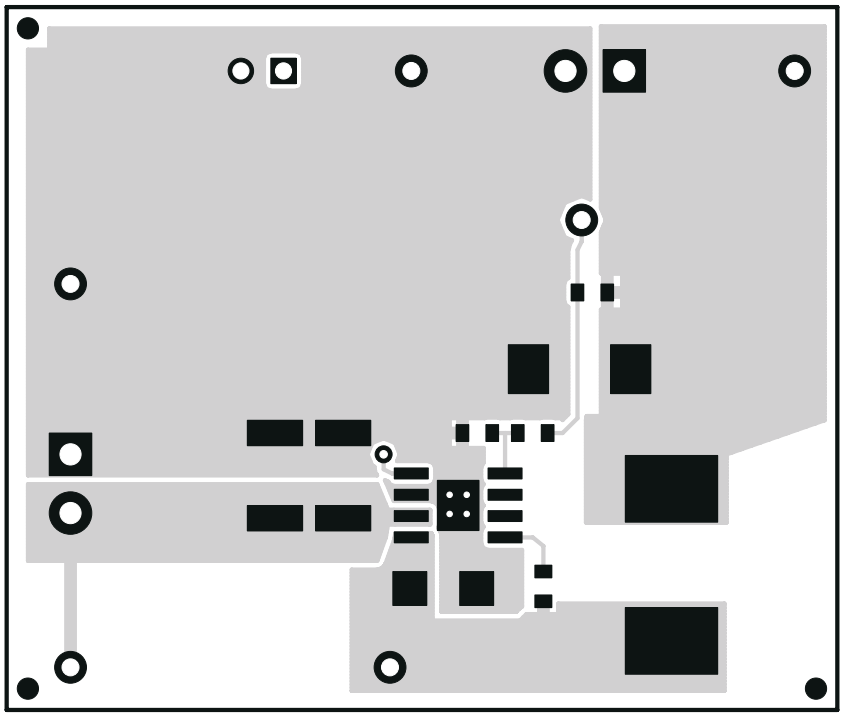

Figure 3-1. Top-Side Layout

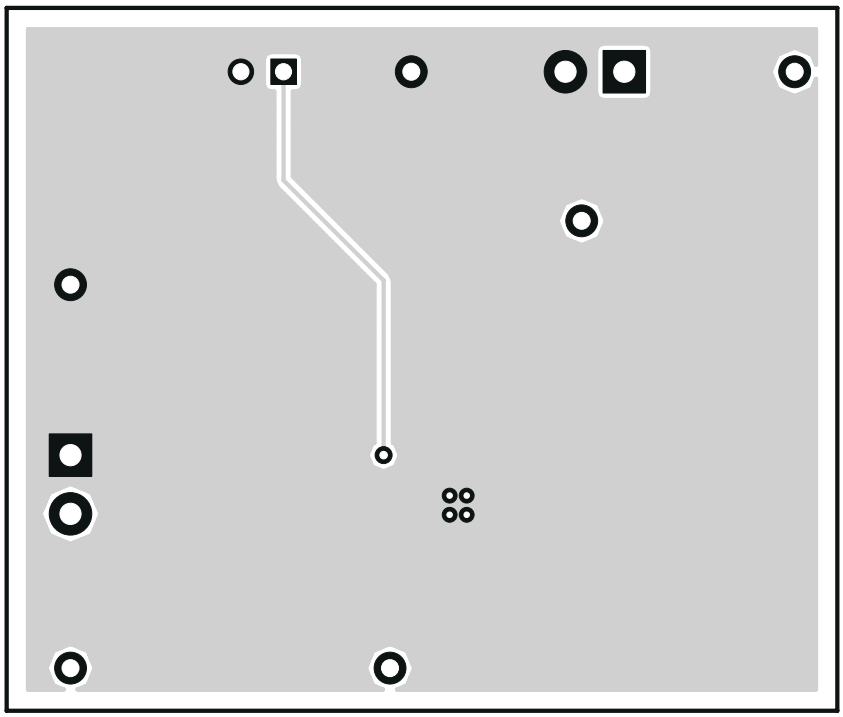

Figure 3-2. Bottom-Side Layout (Looking From Top Side)

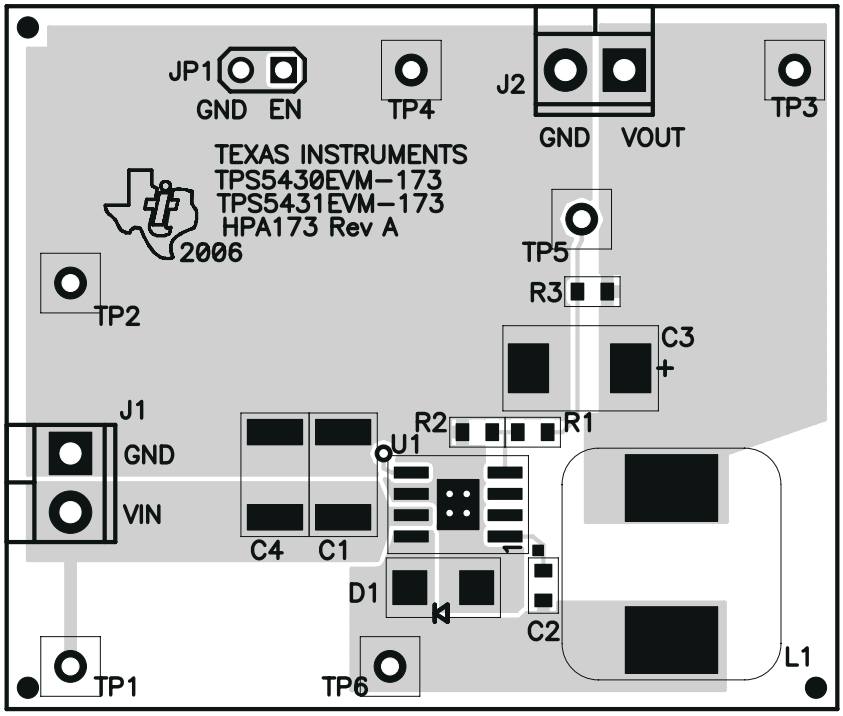

Figure 3-3. Top-Side Assembly

4 Schematic and Bill of Materials

The TPS5430EVM-173 and TPS5431EVM-173 schematic and bill of materials are presented in this section.

4.1 Schematic

The schematic for the TPS5430EVM-173 and TPS5431EVM-173is shown in Figure 4-1.

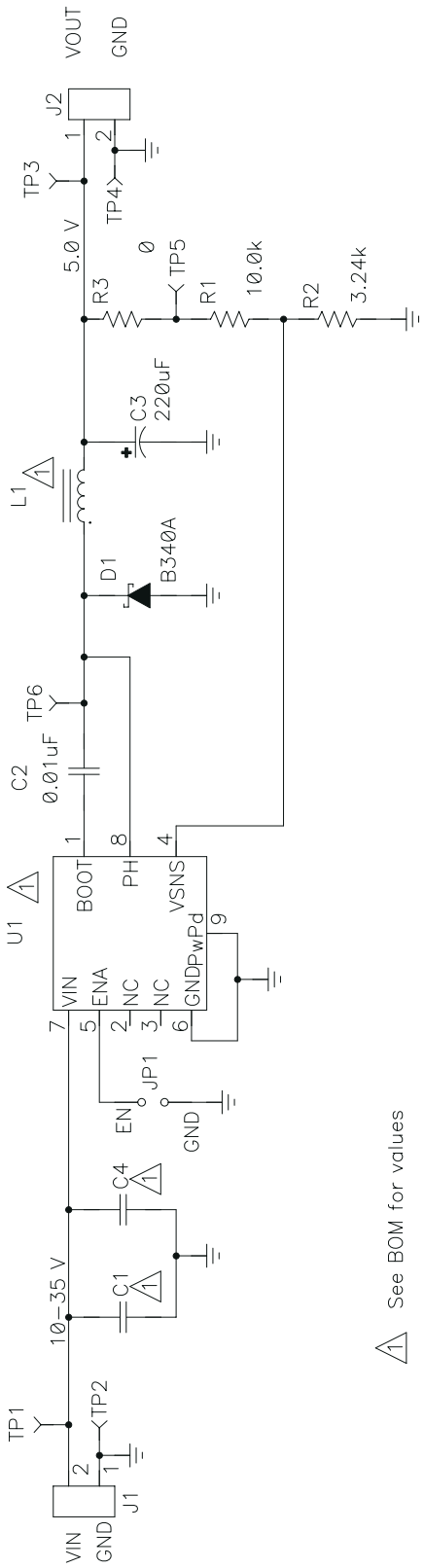

Figure 4-1. TPS5430EVM-173 Schematic

4.2 Bill of Materials

The bill of materials for the TPS5430EVM-173 and TPS5431EVM-173 is given by Table 4-1.

Table 4-1. TPS5430EVM-173 Bill of Materials

Count		RefDes	Value	Description	Size	Part Number	MFR
-001	-002						
1	0	C1	4.7 µF	Capacitor, Ceramic, 50V, X7R, 20%	1812	C4532X5R1H475MT	TDK
0	1		10 µF	Capacitor, Ceramic, 25V, X7R, 20%	1812	C4532X7R1E106KT	TDK
1	1	C2	0.01 µF	Capacitor, Ceramic, 50V, X7R, 10%	0603	C1608X7R1H103K	TDK
1	1	C3	220 µF	Capacitor, POSCAP, 10V, 40mΩ, 20%	7343(D)	10TPB220M	Sanyo
1	0	C4	4.7 µF	Capacitor, Ceramic, 50V, X5R, 20%	1812	C4532X5R1H475MT	TDK
1	1	D1		Diode, Schottky, 3A, 40V	SMA	B340A	Diode Inc
2	2	J1, J2		Terminal Block, 2-pin, 6-A, 3,5mm	0.27 × 0.25	ED1514	OST
1	1	JP1		Header, 2pin, 100mil spacing, (36-pin strip)	0.100 × 2	PTC36SAAN	Sullins
1	0	L1	22 µH	Inductor, Power, 3.6A, 50mΩ	0.484 × 0.484	MSS1278-223MLB	Coilcraft
0	1		18 µH	Inductor, Power, 4A, 43mΩ	0.484 × 0.484	MSS1278-183MLB	Coilcraft
1	1	R1	10.0k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	1	R2	3.24k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	1	R3	0	Resistor, Chip, 1/16W, 1%	0603	Std	Std
4	4	TP1, TP3, TP5, TP6		Test Point, Red, Thru Hole Color Keyed	0.100 × 0.100	5000	Keystone
2	2	TP2, TP4		Test Point, Black, Thru Hole Color Keyed	0.100 × 0.100	5001	Keystone
1	0	U1		IC, Switching Step-Down Regulator, 5.5V-36V, 3A	SO8[DDA]	TPS5430DDA	TI
0	1			IC, Switching Step-Down Regulator, 5.5V-23V, 3A	SO8[DDA]	TPS5431DDA	TI
1	1	—		PCB, 1.95 In × 1.65 In × 0.062 In		HPA173	Any
1	1	—		Shunt, 100mil, Black	0.100	929950-00	3M

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (March 2006) to Revision A (October 2021) **Page**

- Updated the numbering format for tables, figures, and cross-references throughout the document. 2
- Updated the user's guide title..... 2

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