

TPS54239 Step-Down Converter Evaluation Module User's Guide



ABSTRACT

This user's guide contains information for the TPS54239EVM-056 evaluation module as well as for the TPS54239. Included are the performance specifications, schematic, and the bill of materials of the TPS54239EVM-056.

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1 Introduction

The TPS54239 is a single, adaptive on-time, D-CAP2™-mode, synchronous buck converter requiring a low external component count. The D-CAP2™ control circuit is optimized for low-ESR output capacitors such as POSCAP, SP-CAP, or ceramic types and features fast transient response with no external compensation. The switching frequency is internally set at a nominal 600 kHz. The high-side and low-side switching MOSFETs are incorporated inside the TPS54239 package along with the gate-drive circuitry. The low drain-to-source on-resistance of the MOSFETs allows the TPS54239 to achieve high efficiencies and helps keep the junction temperature low at high-output currents. The TPS54239 dc/dc synchronous converter is designed to provide up to a 2-A output from an input voltage source of 4.5 V to 23 V. The output voltage range is from 0.76 V to 7 V. Rated input voltage and output current range for the evaluation module are given in [Table 1-1](#).

The TPS54239EVM-056 evaluation module circuit is a single, synchronous buck converter providing 1.05 V at 2 A from 4.5-V to 23-V input. This user's guide describes the TPS54239EVM-056 performance.

Table 1-1. Input Voltage and Output Current Summary

| EVM | Input Voltage Range | Output Current Range |
|-----------------|---|----------------------|
| TPS54239EVM-056 | $V_{IN} = 4.5 \text{ V to } 23 \text{ V}$ | 0 A to 2 A |

2 Performance Specification Summary

A summary of the TPS54239EVM-056 performance specifications is provided in [Table 2-1](#). Specifications are given for an input voltage of $V_{IN} = 12\text{ V}$ and an output voltage of 1.05 V , unless otherwise noted. The ambient temperature is 25°C for all measurement, unless otherwise noted.

Table 2-1. TPS54239EVM-056 Performance Specifications Summary

| Specifications | Test Conditions | Min | Typ | Max | Unit |
|----------------------------------|---|-----|------------|-----|------------------|
| Input voltage range (V_{IN}) | | 4.5 | 12 | 23 | V |
| Output voltage | | | 1.05 | | V |
| Operating frequency | $V_{IN} = 12\text{ V}$, $I_O = 1.5\text{ A}$ | | 600 | | kHz |
| Output current range | | 0 | | 2 | A |
| Line regulation | $I_O = 1\text{ A}$ | | +0.5/- 0.3 | | % |
| Load regulation | $V_{IN} = 12\text{ V}$ | | +/- 0.02 | | % |
| Overcurrent limit | $V_{IN} = 12\text{ V}$, $L_O = 2.2\text{ }\mu\text{H}$ | 2.5 | 3.1 | 4.6 | A |
| Output ripple voltage | $V_{IN} = 12\text{ V}$, $I_O = 2\text{ A}$ | | 10 | | mV _{PP} |
| Maximum efficiency | $V_{IN} = 5\text{ V}$, $I_O = 0.5\text{ A}$ | | 87.7 | | % |

3 Modifications

These evaluation modules are designed to provide access to the features of the TPS54239. Some modifications can be made to this module.

3.1 Output Voltage Setpoint

To change the output voltage of the EVMs, it is necessary to change the value of resistor R1. Changing the value of R1 can change the output voltage above 0.765 V. The value of R1 for a specific output voltage can be calculated using [Equation 1](#).

For output voltage from 0.76 V to 7 V:

$$V_O = 0.765 \times \left(1 + \frac{R_1}{R_2} \right) \quad (1)$$

[Table 3-1](#) lists the R1 values for some common output voltages. For higher output voltages of 1.8 V or above, a feedforward capacitor (C4) may be required to improve phase margin. Pads for this component (C4) are provided on the printed-circuit board (PCB). Note that the resistor values given in [Table 3-1](#) are standard values and not the exact value calculated using [Equation 1](#).

Table 3-1. Output Voltages

| Output Voltage (V) | R1 (kΩ) | R2 (kΩ) | C4 (pF) ⁽¹⁾ | | | L1 (μH) | | | C8 + C9 + C10 (μF) | |
|--------------------|---------|---------|------------------------|-----|-----|---------|-----|-----|--------------------|-----|
| | | | Min | Typ | Max | Min | Typ | Max | Min | Max |
| 1 | 6.81 | 22.1 | 5 | 150 | 220 | 1.5 | 2.2 | 4.7 | 22 | 68 |
| 1.05 | 8.25 | 22.1 | 5 | 150 | 220 | 1.5 | 2.2 | 4.7 | 22 | 68 |
| 1.2 | 12.7 | 22.1 | 5 | | 100 | 1.5 | 2.2 | 4.7 | 22 | 68 |
| 1.5 | 21.5 | 22.1 | 5 | | 68 | 1.5 | 2.2 | 4.7 | 22 | 68 |
| 1.8 | 30.1 | 22.1 | 5 | | 22 | 2.2 | 3.3 | 4.7 | 22 | 68 |
| 2.5 | 49.9 | 22.1 | 5 | | 22 | 2.2 | 3.3 | 4.7 | 22 | 68 |
| 3.3 | 73.2 | 22.1 | 5 | | 22 | 2.2 | 3.3 | 4.7 | 22 | 68 |
| 5 | 124 | 22.1 | 5 | | 22 | 3.3 | | 4.7 | 22 | 68 |
| 6.5 | 165 | 22.1 | 5 | | 22 | 3.3 | | 4.7 | 22 | 68 |

(1) Optional

3.2 Output Filter and Closed-Loop Response

The TPS54239 relies on the output filter characteristics to ensure stability of the control loop. The recommended output filter components for common output voltages are given in [Table 3-1](#). It may be possible for other output filter component values to provide acceptable closed-loop characteristics. R3 and TP4 are provided for convenience in breaking the control loop and measuring the closed-loop response.

4 Test Setup and Results

This section describes how to properly connect, set up, and use the TPS54239EVM-056. The section also includes test results typical for the evaluation modules and efficiency, output load regulation, output line regulation, load transient response, output voltage ripple, input voltage ripple, start-up, and switching frequency.

4.1 Input/Output Connections

The TPS54239EVM-056 is provided with input and output connectors and test points as shown in [Table 4-1](#). A power supply capable of supplying 2 A must be connected to J1 through a pair of 20 AWG wires. The load must be connected to J2 through a pair of 20 AWG wires. The maximum load current capability is 2 A. Wire lengths must be minimized to reduce losses in the wires. Test point TP1 provides a place to monitor the V_{IN} input voltages with TP2 providing a convenient ground reference. TP8 is used to monitor the output voltage with TP9 as the ground reference.

Table 4-1. Connection and Test Points

| Reference Designator | Function |
|----------------------|--|
| J1 | V_{IN} (see Table 1-1 for V_{IN} range) |
| J2 | V_{OUT} , 1.05 V at 2-A maximum |
| JP1 | EN control. Connect EN to OFF to disable, connect EN to ON to enable |
| TP1 | V_{IN} test point at V_{IN} connector |
| TP2 | GND test point at V_{IN} connector. |
| TP3 | EN test point |
| TP4 | Loop response measurement test point |
| TP5 | VREG5 test point |
| TP6 | Switch node test point |
| TP7 | Analog ground test point |
| TP8 | Output voltage test point at V_{OUT} connector |
| TP9 | Ground test point at V_{OUT} connector |

4.2 Start-Up Procedure

1. Ensure that the jumper at JP1 (Enable control) is set from EN to OFF.
2. Apply appropriate V_{IN} voltage to V_{IN} and PGND terminals at J1.
3. Move the jumper at JP1 (Enable control) to cover EN and ON. The EVM enables the output voltage.

4.3 Efficiency

Figure 4-1 shows the efficiency for the TPS54239EVM-056 at an ambient temperature of 25°C.

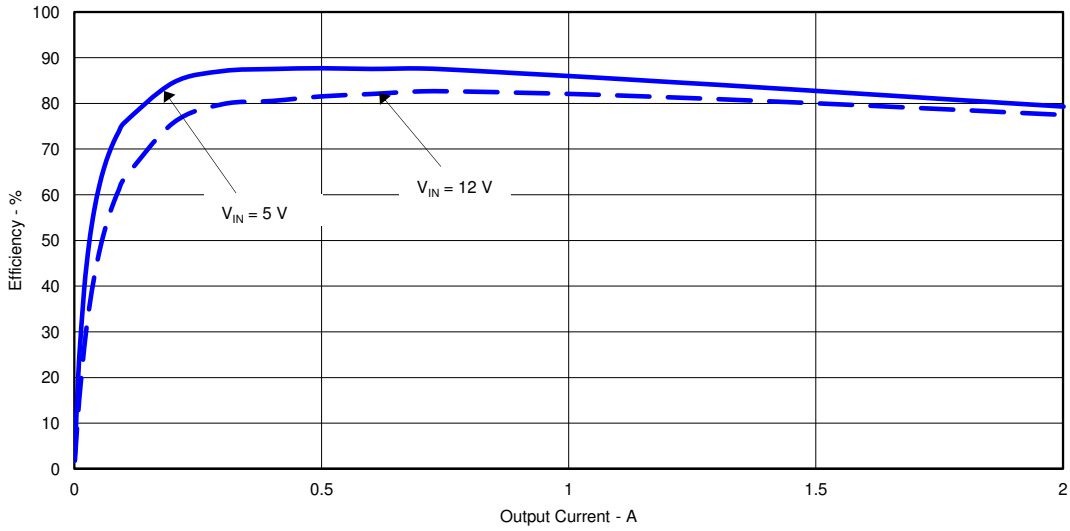


Figure 4-1. TPS54239EVM-056 Efficiency

Figure 4-2 shows the efficiency at light loads for the TPS54239EVM-056 at an ambient temperature of 25°C.

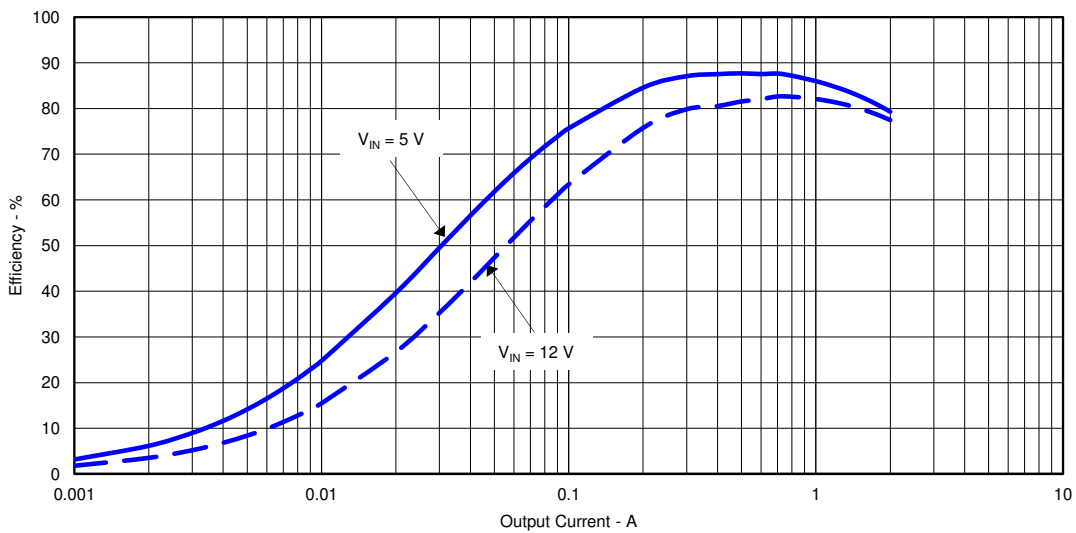


Figure 4-2. TPS54239EVM-056 Light-Load Efficiency

4.4 Load Regulation

The load regulation for the TPS54239EVM-056 is shown in Figure 4-3.

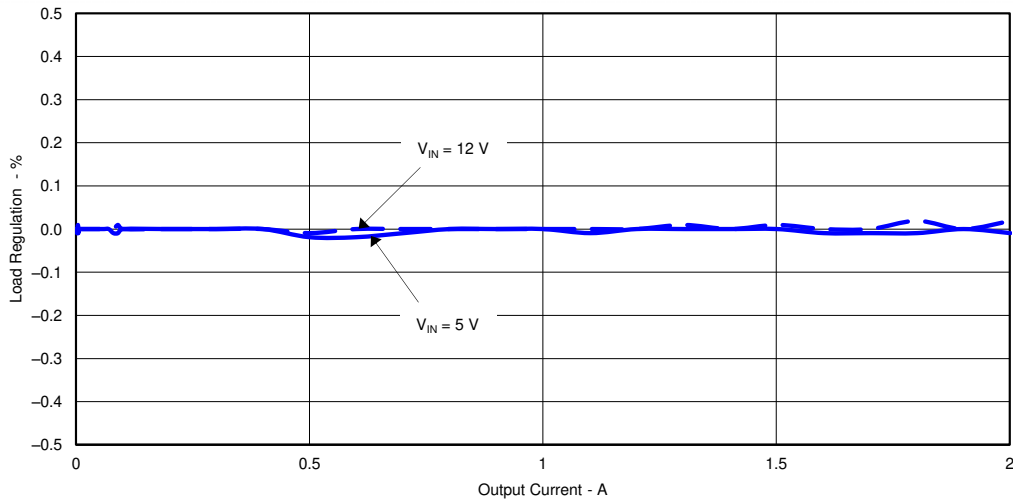


Figure 4-3. TPS54239EVM-056 Load Regulation, $V_{IN} = 5\text{ V}$ and $V_{IN} = 12\text{ V}$

4.5 Line Regulation

The line regulation for the TPS54239EVM-056 is shown in Figure 4-4.

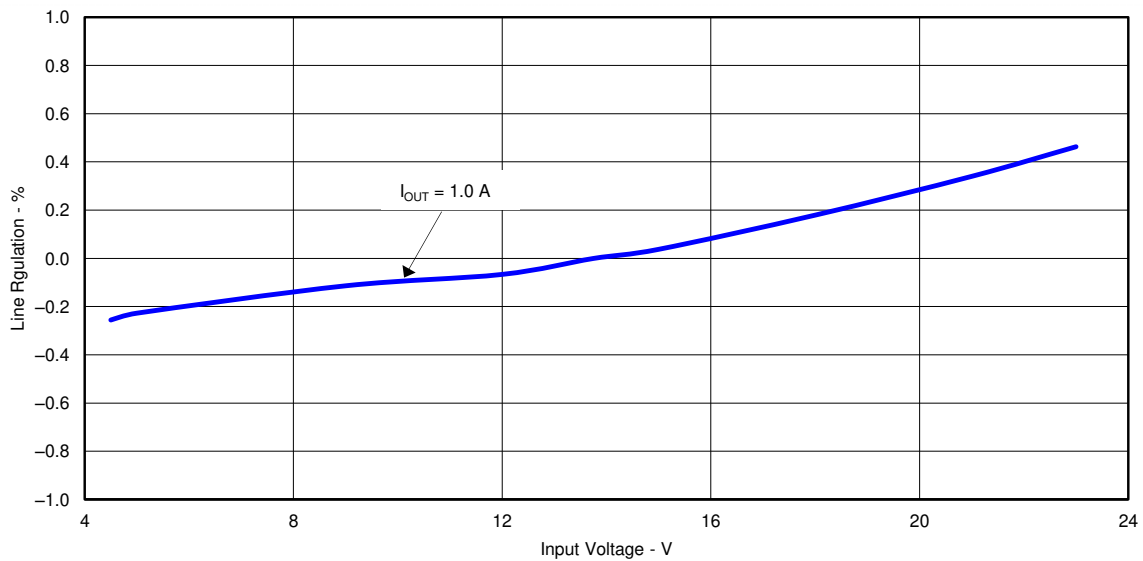


Figure 4-4. TPS54239EVM-056 Line Regulation

4.6 Load Transient Response

The TPS54239EVM-056 response to load transient is shown in Figure 4-5. The current step is from 0.5 A to 1.5 A. Total peak-to-peak voltage variation is as shown.

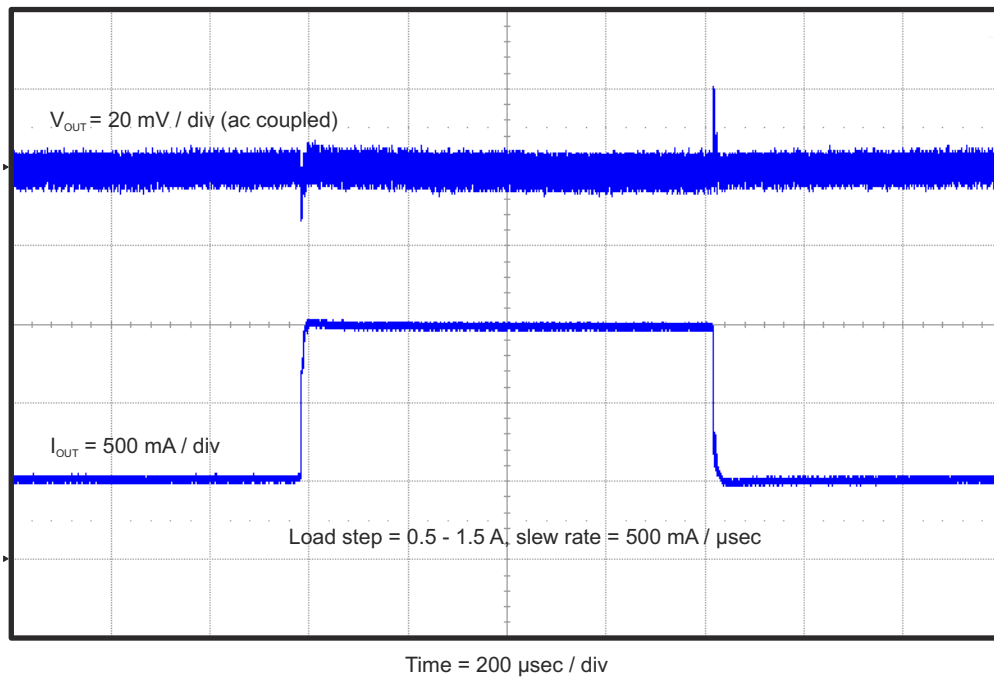


Figure 4-5. TPS54239EVM-056 Load Transient Response

4.7 Output Voltage Ripple

The TPS54239EVM-056 output voltage ripple is shown in Figure 4-6. The output current is the rated full load of 2 A.

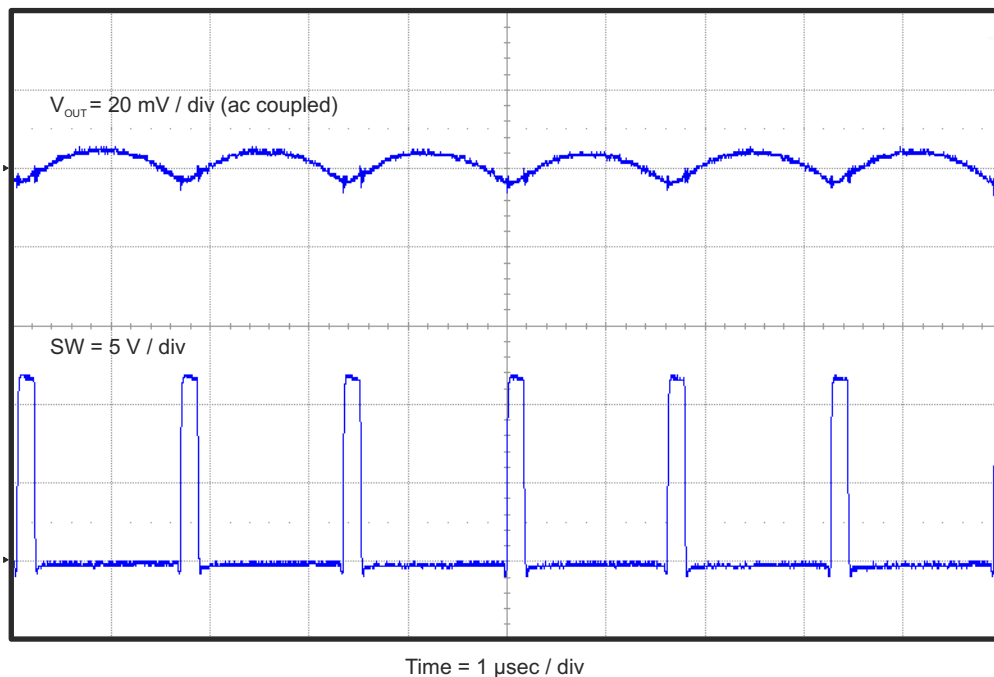


Figure 4-6. TPS54239EVM-056 Output Voltage Ripple ($I_{OUT} = 2 \text{ A}$)

The TPS54239EVM-056 output voltage ripple is shown in [Figure 4-7](#). The output current is 0 A (no load).

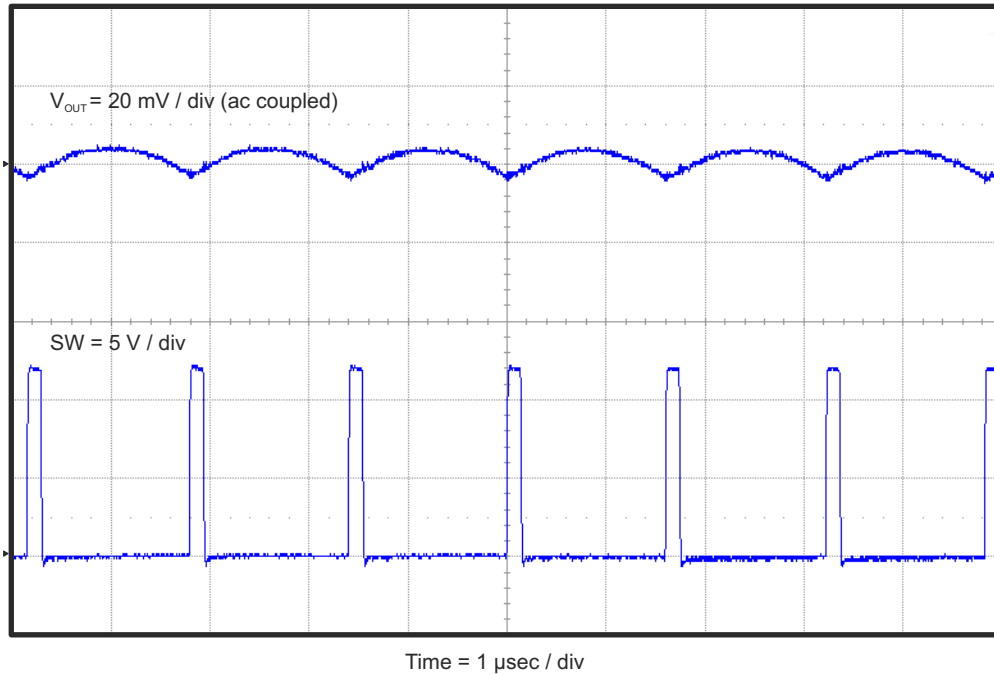


Figure 4-7. TPS54239EVM-056 Output Voltage Ripple ($I_{OUT} = 0 \text{ A}$)

4.8 Input Voltage Ripple

The TPS54239EVM-056 input voltage ripple is shown in [Figure 4-8](#). The output current is the rated full load of 2 A.

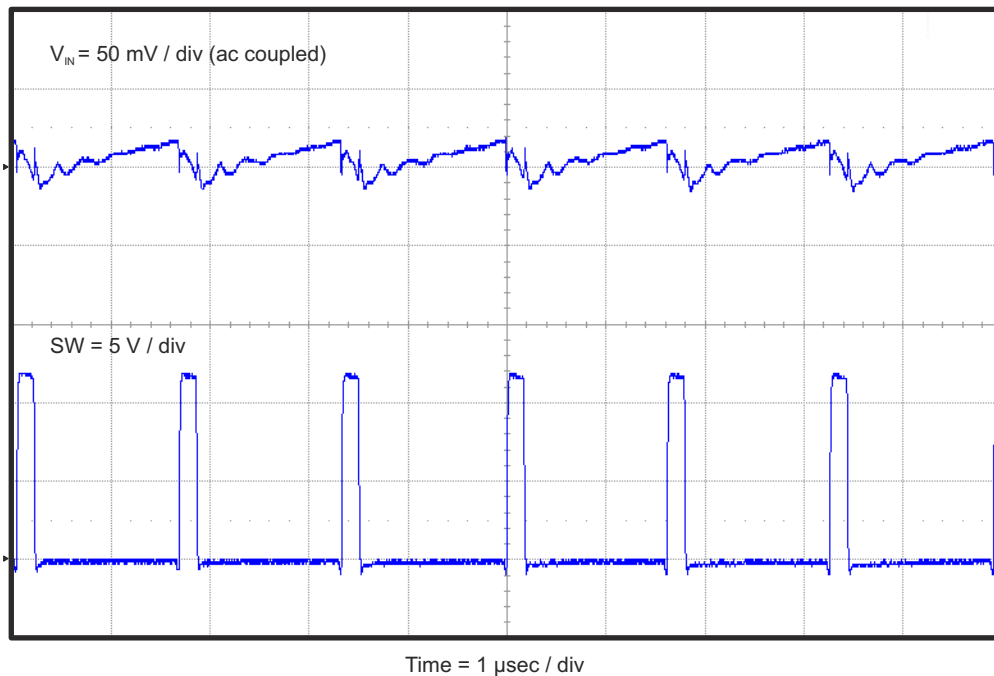


Figure 4-8. TPS54239EVM-056 Input Voltage Ripple

4.9 Start-Up

The TPS54239EVM-056 start-up waveforms relative to V_{IN} and EN are shown in Figure 4-9 and Figure 4-10. $R_{LOAD} = 1 \Omega$.

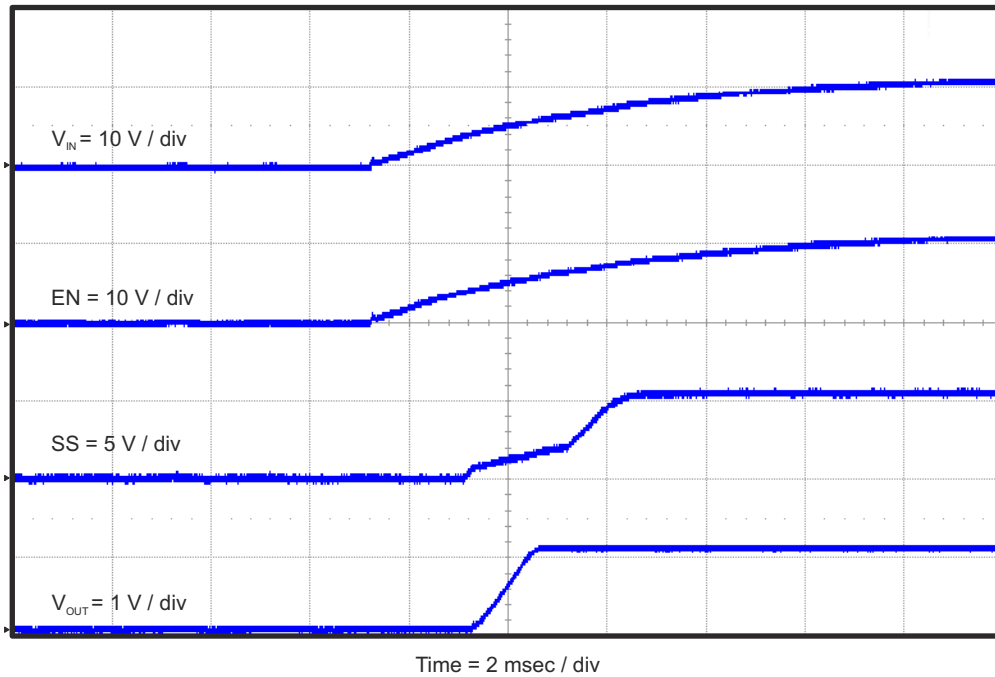


Figure 4-9. TPS54239EVM-056 Start-Up Relative to V_{IN} with SS

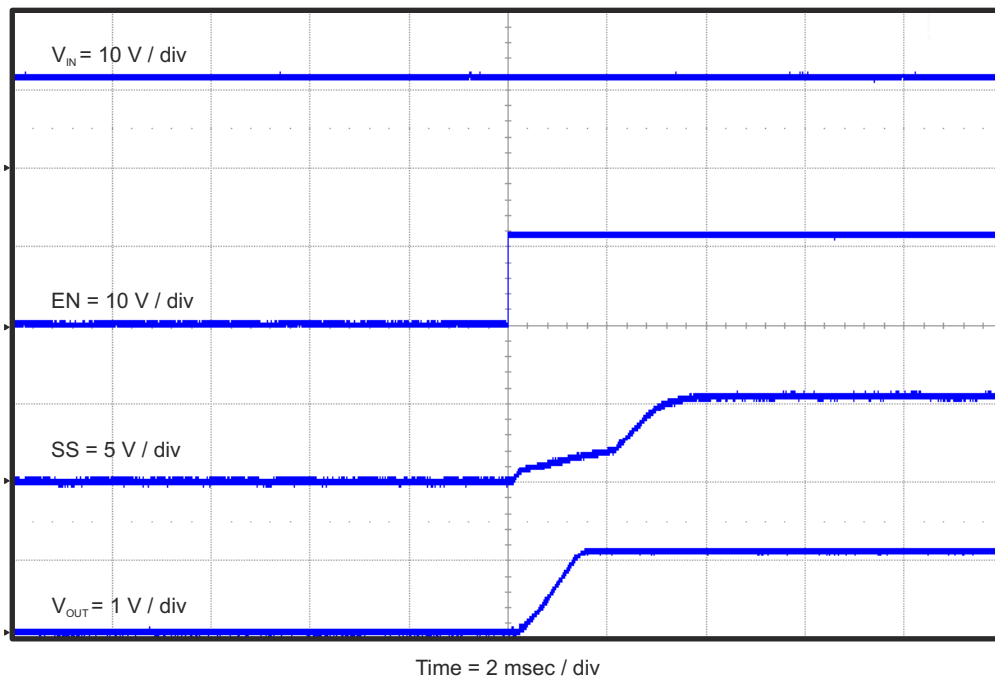


Figure 4-10. TPS54239EVM-056 Start-Up Relative to EN with SS

4.10 Shut-Down

The TPS54239EVM-056 shut-down waveforms relative to V_{IN} and EN are shown in Figure 4-11 and Figure 4-12. $R_{LOAD} = 1 \Omega$.

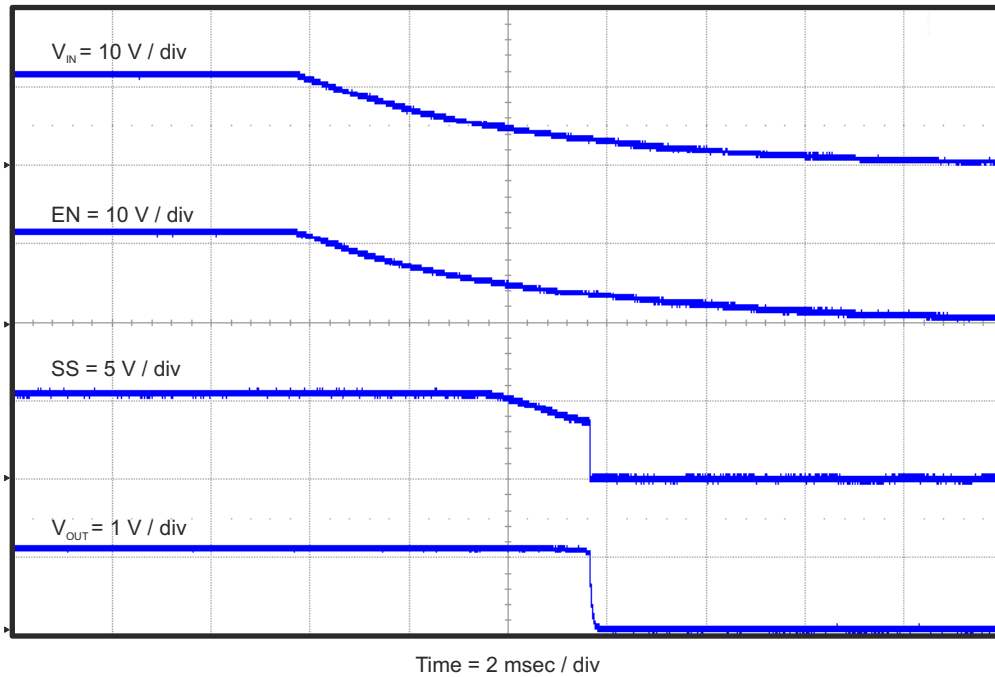


Figure 4-11. TPS54239EVM-056 Shut-Down Relative to V_{IN} with SS

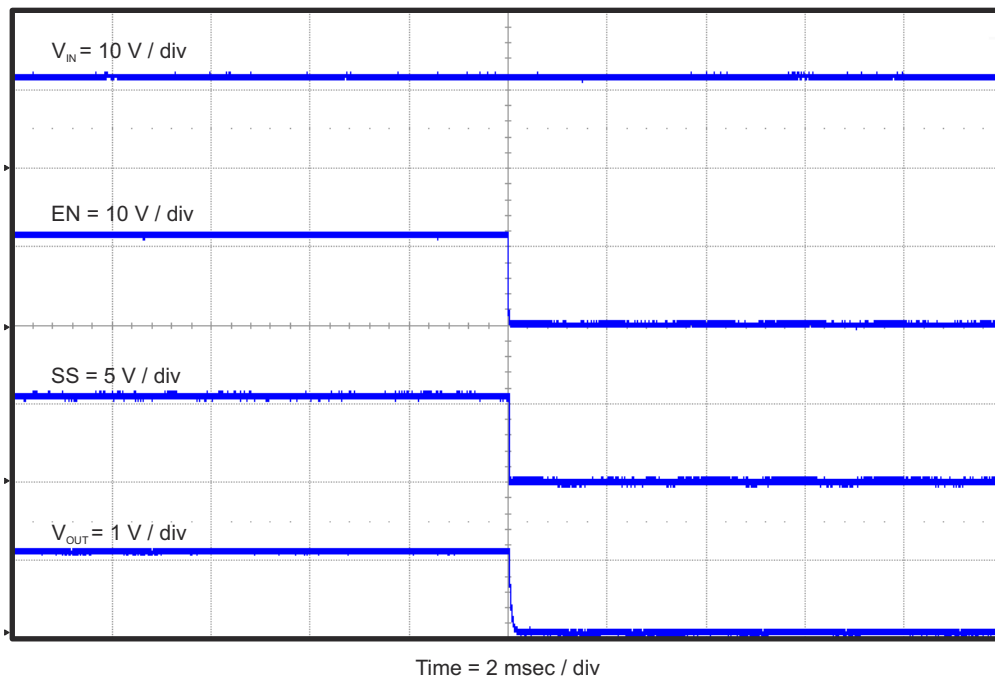


Figure 4-12. TPS54239EVM-056 Shut-Down Relative to EN with SS

5 Board Layout

This section provides description of the TPS54239EVM-056, board layout, and layer illustrations.

5.1 Layout

The board layout for the TPS54239EVM-056 is shown in [Figure 5-1](#) through [Figure 5-5](#). The top layer contains the main power traces for VIN, VO, and ground. Also on the top layer are connections for the pins of the TPS54239 and a large area filled with ground. Many of the signal traces also are located on the top side. The input decoupling capacitors are located as close to the IC as possible. The input and output connectors, test points, and all of the components are located on the top side. An analog ground (GND) area is provided on the top side. Analog ground (GND) and power ground (PGND) are connected at a single point on the top layer near C6. The two internal layers are completely dedicated to power ground planes. The bottom layer is primarily power ground. A copper pour area on the bottom layer is used to connect the switching node (SW) to the output inductor and the boost capacitor. Traces also connect enable control jumper, EN, VREG5, and LOOP test points, and the feedback trace from VOUT to the voltage setpoint divider network.

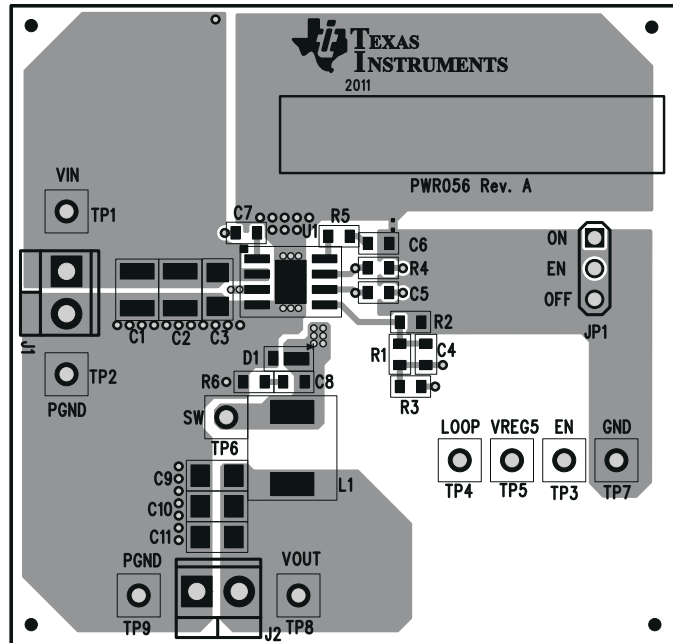


Figure 5-1. Top Assembly

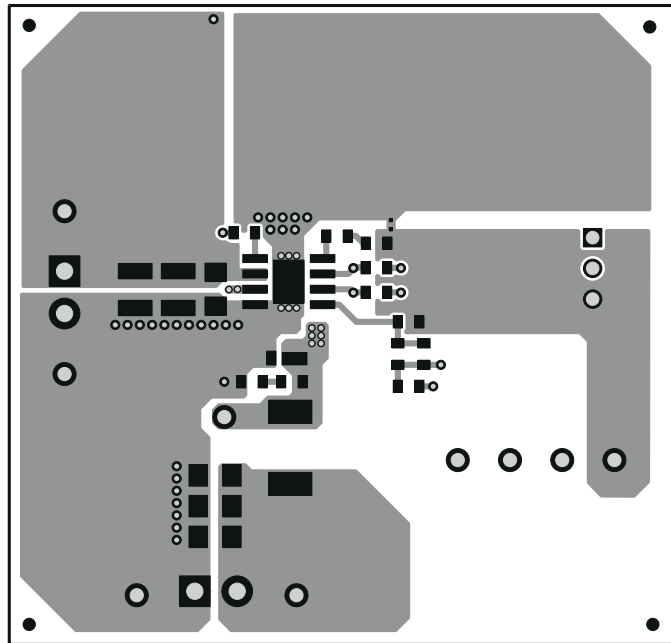


Figure 5-2. Top Layer

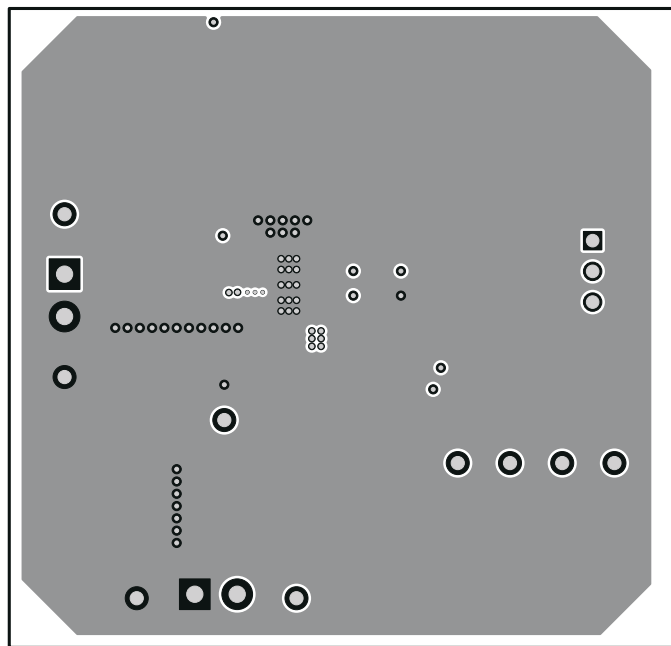


Figure 5-3. Internal Layer 1

6 Schematic, Bill of Materials, and Reference

6.1 Schematic

Figure 6-1 is the schematic for the TPS54239EVM-056.

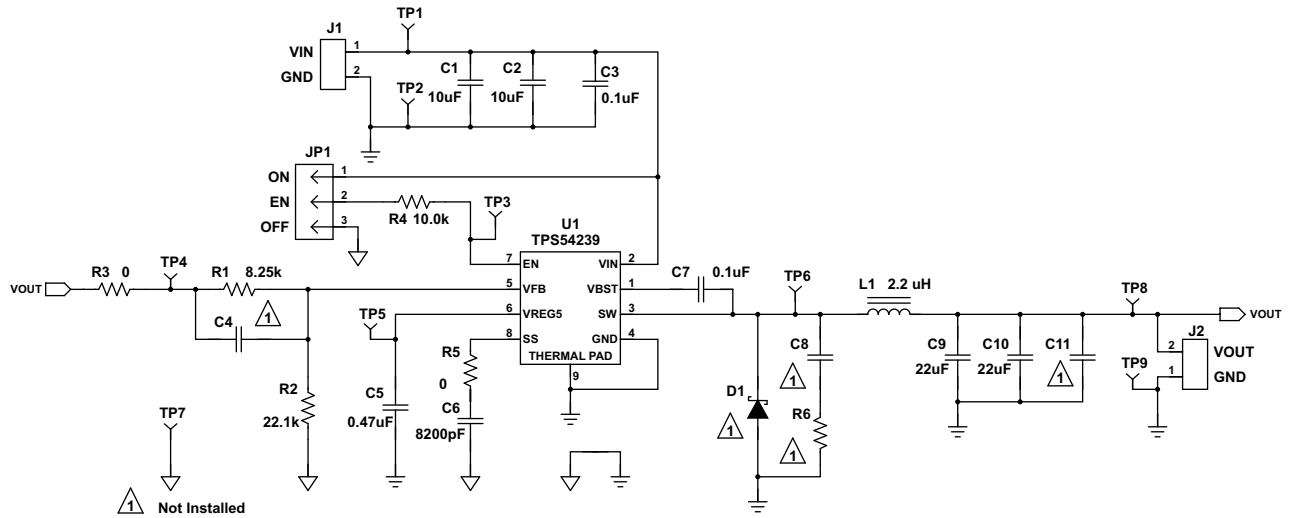


Figure 6-1. TPS54239EVM-056 Schematic Diagram

6.2 Bill of Materials

Table 6-1. Bill of Materials

| RefDes | Qty | Value | Description | Size | Part Number | MFR |
|------------------------------|-----|-------------|---|--------------------|----------------|----------|
| C1, C2 | 2 | 10uF | Capacitor, Ceramic, 25V, X5R, 20% | 1210 | Std | Std |
| C3 | 1 | 0.1uF | Capacitor, Ceramic, 50V, X7R, 10% | 1206 | Std | Std |
| C4, C8 | 0 | Open | Capacitor, Ceramic | 0603 | Std | Std |
| C5 | 1 | 0.47uF | Capacitor, Ceramic, 16V, X7R, 10% | 0603 | Std | Std |
| C6 | 1 | 8200pF | Capacitor, Ceramic, 25V, X7R, 10% | 0603 | Std | Std |
| C7 | 1 | 0.1uF | Capacitor, Ceramic, 50V, X7R, 10% | 0603 | Std | Std |
| C9, C10 | 2 | 22uF | Capacitor, Ceramic, 6.3V, X5R, 20% | 1206 | C3216X5R0J226M | TDK |
| C11 | 1 | Open | Capacitor, Ceramic | 1206 | Std | Std |
| D1 | 0 | Open | Diode, 0.5 A, 30 V, 2PIN | TUMD2 | RSX051VA-30 | Rohm |
| J1, J2 | 2 | ED555/2DS | Terminal Block, 2-pin, 6-A, 3.5mm | 0.27 x 0.25 inch | ED555/2DS | Sullins |
| JP1 | 1 | PEC03SAAN | Header, Male 3-pin, 100mil spacing | 0.100 inch x 3 | PEC03SAAN | Sullins |
| L1 | 1 | 2.2uH | Inductor, SMT, 5.5A, 14.6 mΩ | 0.256 x 0.280 inch | CLF7045T-2R2N | TDK |
| R1 | 1 | 8.25k | Resistor, Chip, 1/16W, 1% | 0603 | Std | Std |
| R2 | 1 | 22.1k | Resistor, Chip, 1/16W, 1% | 0603 | Std | Std |
| R3, R5 | 2 | 0 | Resistor, Chip, 1/16W, 1% | 0603 | Std | Std |
| R4 | 1 | 10.0k | Resistor, Chip, 1/16W, 1% | 0603 | Std | Std |
| R5 | 0 | Open | Resistor, Chip, 1/16W, 1% | 0603 | Std | Std |
| TP1, TP3, TP4, TP5, TP6, TP8 | 3 | 5000 | Test Point, Red, Thru Hole Color Keyed | 0.100 x 0.100 inch | 5000 | Keystone |
| TP2, TP7, TP9 | 3 | 5001 | Test Point, Black, Thru Hole Color Keyed | 0.100 x 0.100 inch | 5001 | Keystone |
| U1 | 1 | TPS54239DDA | IC, 4.5-23 V Input, 2-A Sync. Step-Down SWIFT Converter | SO8[DDA] | TPS54239DDA | TI |
| - | 1 | | Shunt, 100-mil, Black | 0.100 | 929950-00 | 3M |
| - | 1 | | PCB | | PWR056 | Any |

6.3 Reference

Texas Instruments, [TPS54239, 4.5-V to 23-V Input, 2-A Synchronous Step-Down SWIFT™ Converter Data Sheet](#)

7 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision * (January 2013) to Revision A (October 2021) | Page |
|--|------|
| • Updated user's guide title..... | 3 |
| • Updated the numbering format for tables, figures, and cross-references throughout the document. | 3 |

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