1 Startup

The startup waveform is shown in Figure 1. The input voltage is set at 12.0V, with no load on the 3.3V output.

Channel C1: **input voltage**
2V/div, 2ms/div

Channel C2: **output voltage**
1V/div, 2ms/div

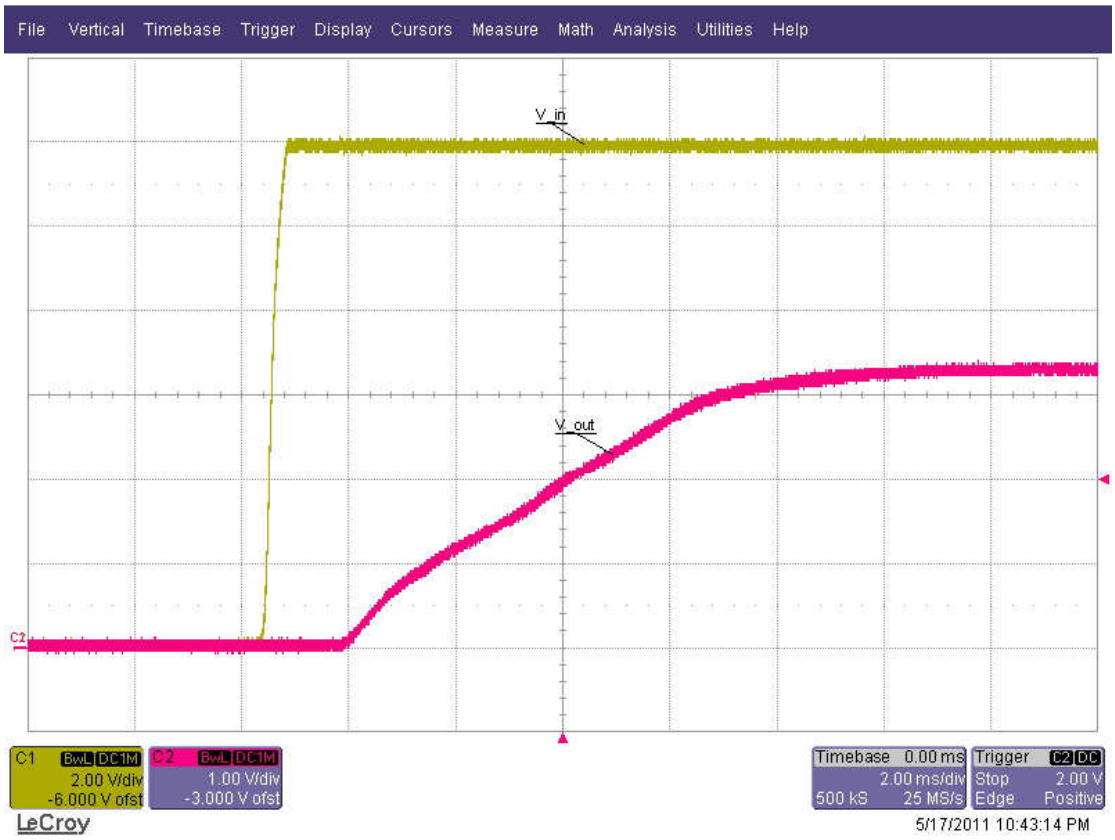

Figure 1

2 Shutdown

The shutdown waveform is shown in Figure 2. The input voltage is set at 3.3V with a 1.0A load on the 3.3V output.

Channel C1: **input voltage**
2V/div, 200us/div

Channel C2: **output voltage**
1V/div, 200us/div

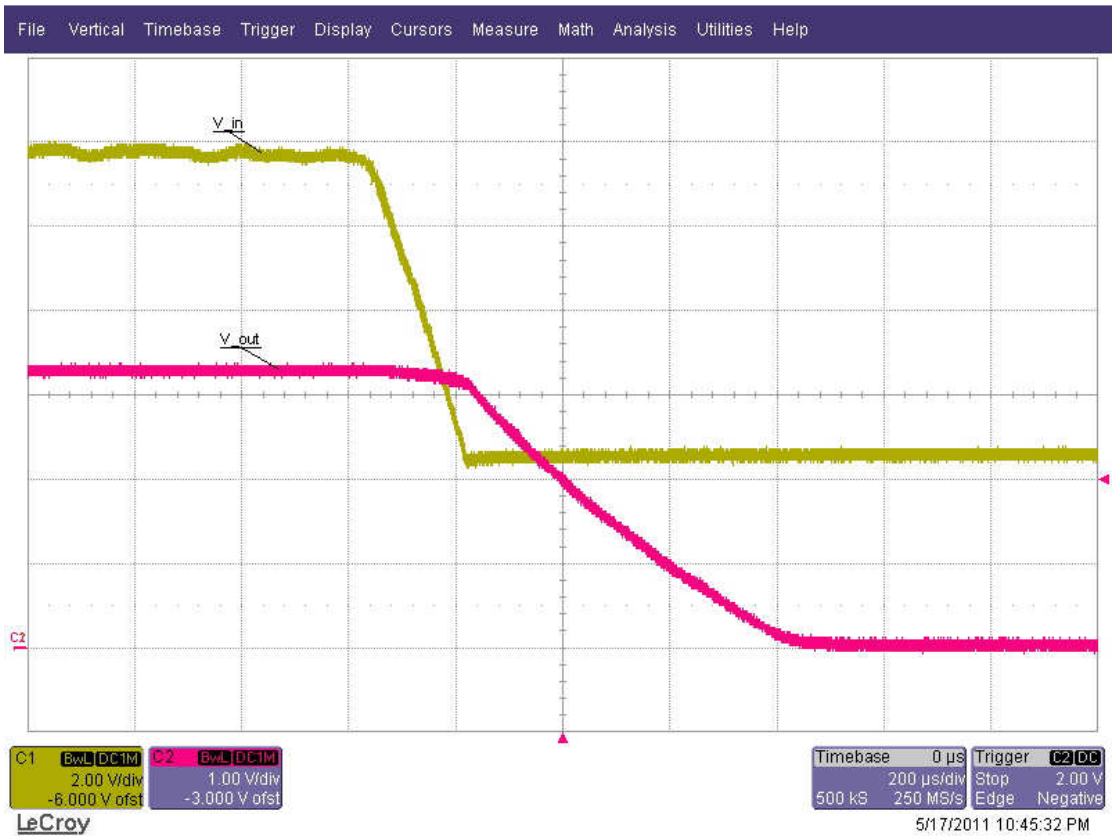

Figure 2

3 Efficiency

The efficiency is shown in Figure 3.

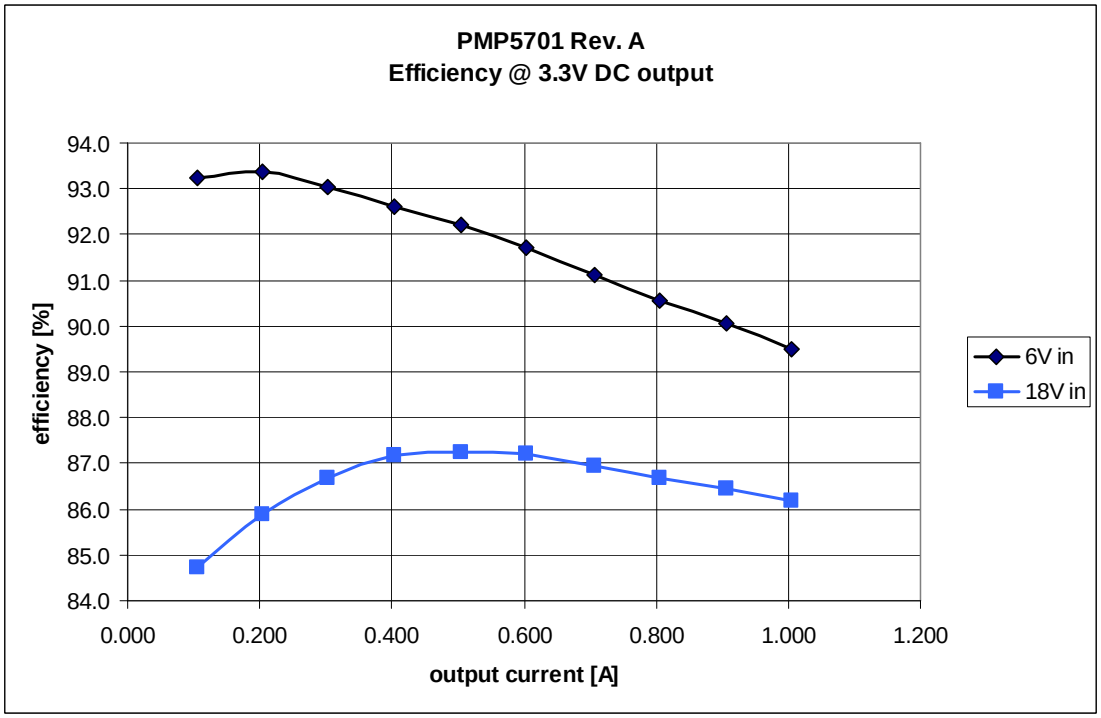

Figure 3

4 Load regulation

The load regulation of the 3.3V output is shown in Figure 4.

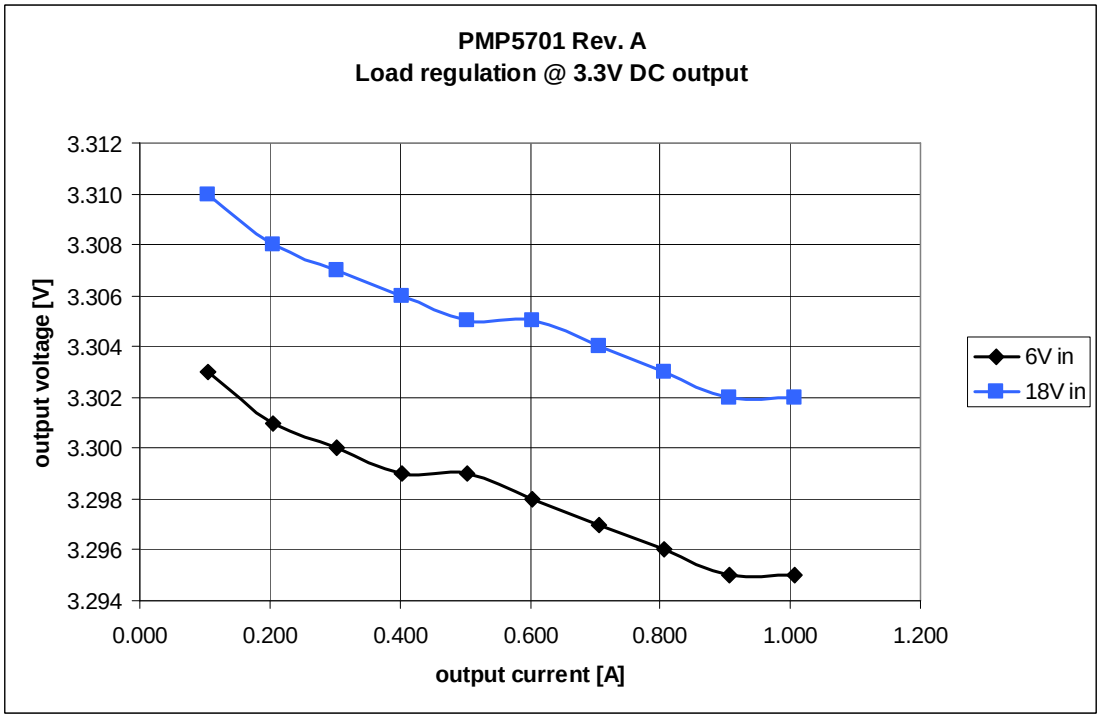

Figure 4

5 Output ripple voltage

The output ripple voltage at 1.0A load and 3.3V input voltage is shown in Figure 5.

Channel C2: **output voltage**, **no measurement possible**
20mV/div, 5us/div, AC coupled

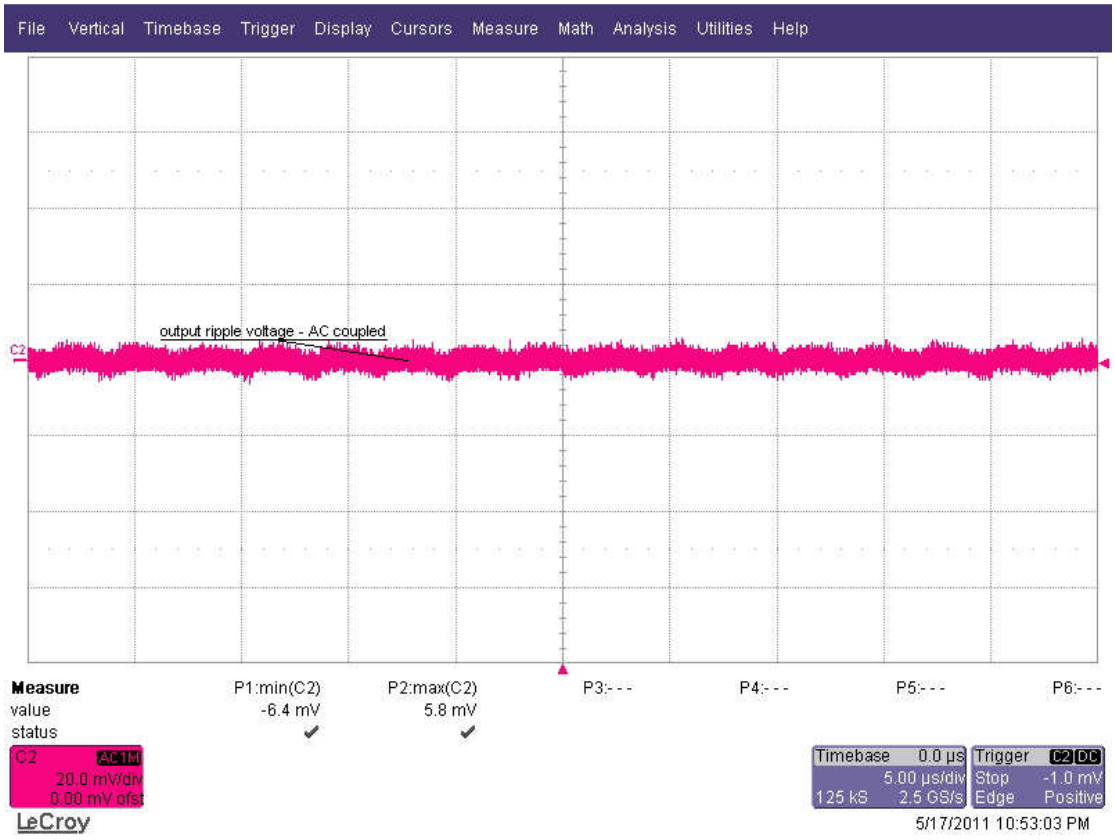

Figure 5

6 Load transients

The response to a load step and a load dump at an input voltage of 3.3V is shown in Figure 6 and Figure 7.

Channel C2: **output voltage**, -142mV undershoot
100mV/div, 200us/div, AC coupled

Channel C1: **load current**, load step 0.5A to 1.0A
500mA/div, 200us/div

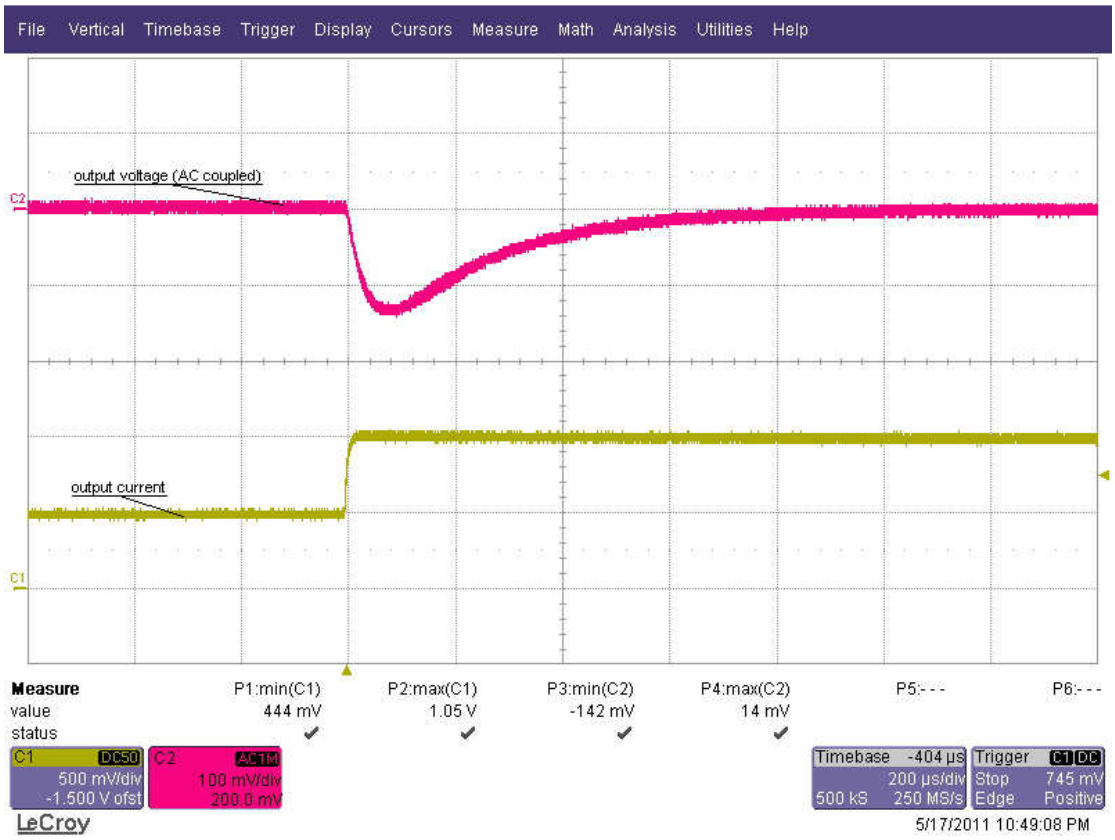

Figure 6

Channel C2: **output voltage**, 136mV overshoot
100mV/div, 200us/div, AC coupled

Channel C1: **load current**, load dump 1.0A to 0.5A
500mA/div, 200us/div

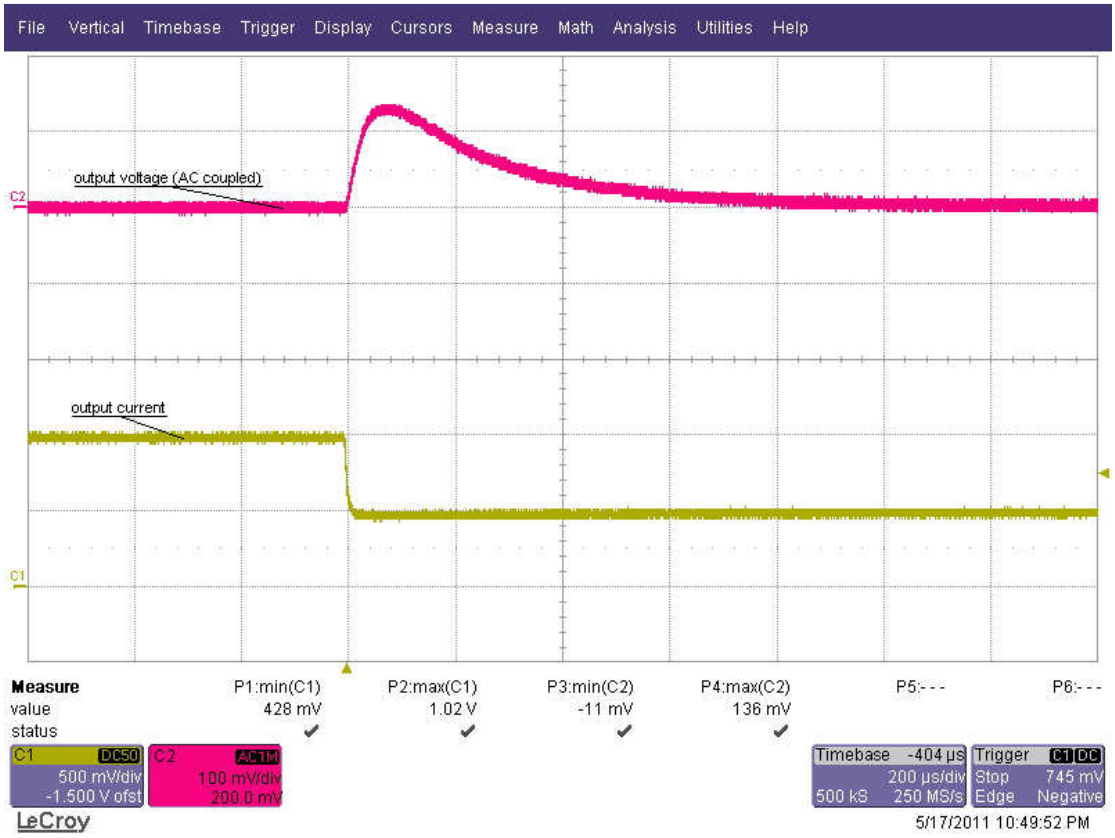

Figure 7

7 Frequency response

Figure 8 shows the loop response of the 3.3V output with 6V and 18Vinput voltage and a 1.0A load.

6V input: 68 deg phase margin @ crossover frequency 3.8 kHz
18V input: 76 deg phase margin @ crossover frequency 4.2 kHz

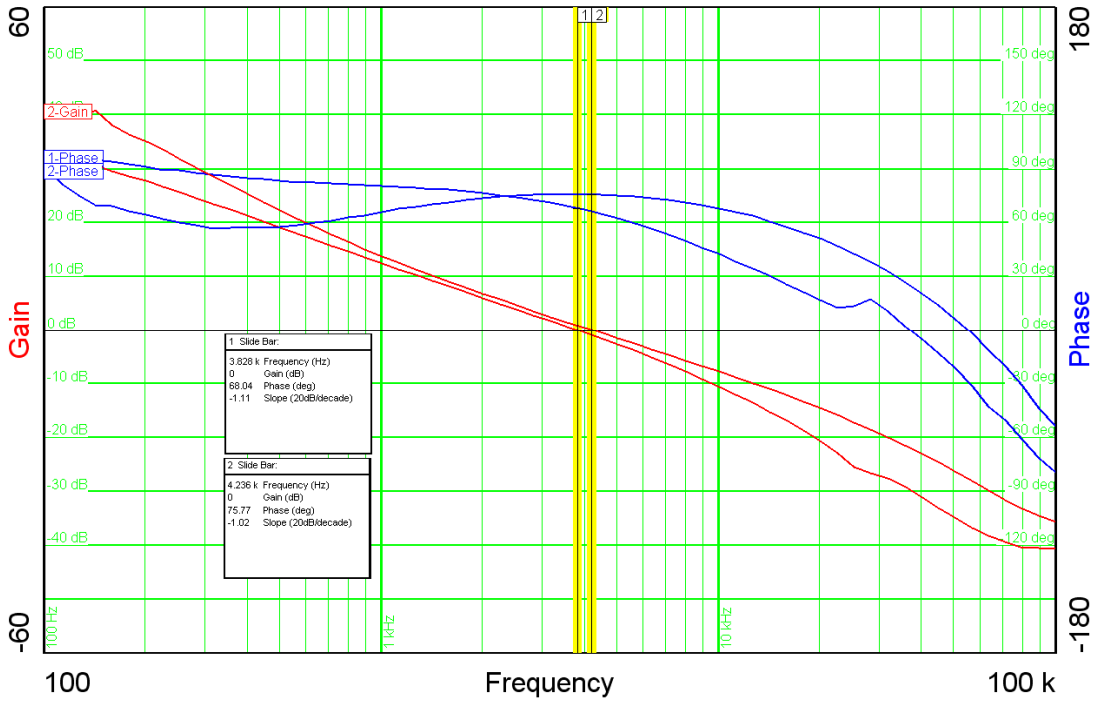

Figure 8

8 Miscellaneous waveforms

The drain-source voltage on the switching node is shown in Figure 9. The image was captured with a 18.0V input and a 1.0A load.

Channel C2: **drain-source voltage**, -1.5V minimum voltage, 18.7V maximum voltage
5V/div, 1us/div

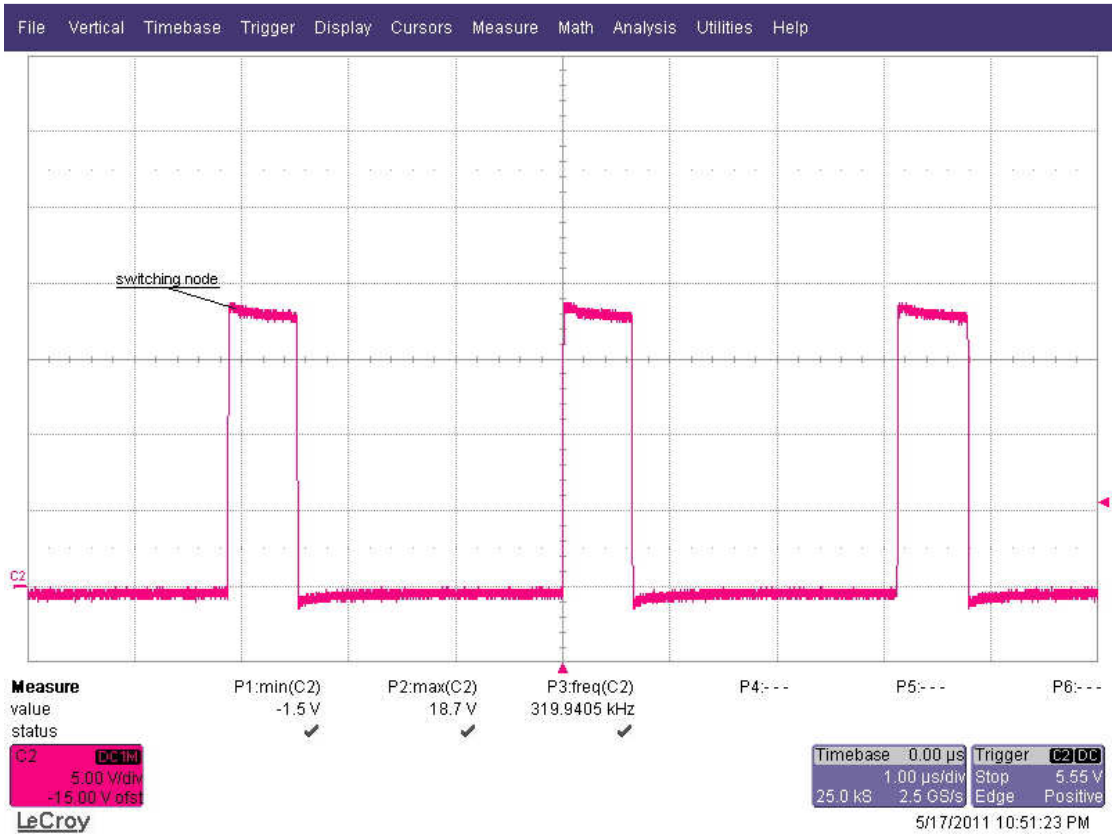

Figure 9

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