TPD4E110DPW Evaluation Module

This user's guide describes the characteristics, operation, and use of the TPD4E110DPWEVM evaluation module (EVM). This EVM includes 15 TPD4E110DPWs in various configurations for testing. Nine TPD4E110DPWs are configured for IEC61000-4-2 compliance testing, two TPD4E110DPW are configured for 4-port s-parameter analysis, and four are configured with USB 3.0 Type A connectors for throughput analysis. Additionally, one of the TPD4E110DPWs for ESD testing also allows the capture of clamping waveforms during an ESD event. This user's guide includes setup instructions, schematic diagrams, a bill of materials, and printed-circuit board layout drawings for the evaluation module.

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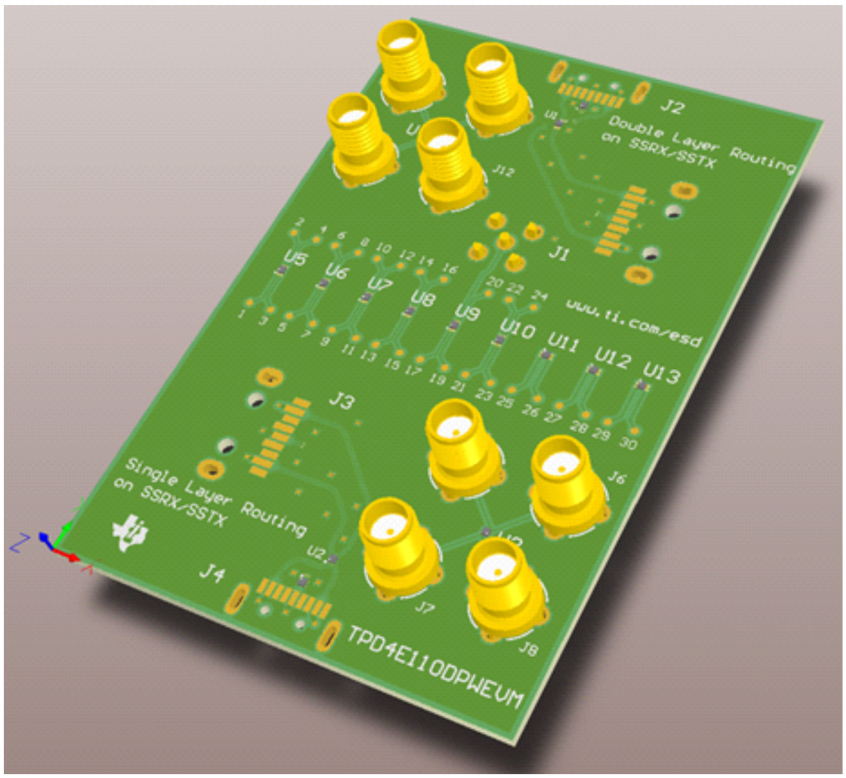
1 Introduction

The Texas Instruments TPD4E110DPW evaluation module helps designers evaluate the operation and performance of the TPD4E110DPW device. The TPD4E110DPW is a quad channel ESD protection device in a small DPW package. The device offers ICE61000-4-2 compliant ESD protection. The less than 0.5 pF line capacitance is suitable for a wide range of applications. The TPD4E110DPW is characterized for operation over an ambient air temperature range of –40°C to +125°C.



The EVM contains fifteen TPD4E110DPWs. Four TPD4E110DPWs (U1, U2, U14, and U15) are configured with USB 3.0 Type A connectors (J1 – J4) for capturing Eye Diagrams. Two TPD4E110DPWs (U3 and U4) are configured with 8 SMA (J5 – J12) connectors allowing 4-port analysis with a vector network analyzer. Nine TPD4E110DPWs (U5 – U13) are configured with test points for striking ESD to the protection pins, one of those (U9) also has an SMB (J13) connector for capturing clamping waveforms with an oscilloscope during an ESD test. Caution must be taken when capturing clamping waveforms during an ESD event so as not to damage the oscilloscope. A proper procedure is outlined in Section 3.5.1.

Table 1 shows the TPD4E110DPW EVM Configuration.

Table 1. EVM Configuration

Reference Designator	TI Part Number	Configuration
U1	TPD4E110DPW	USB 2.0 eye diagram
U2	TPD4E110DPW	S-parameters
U3 – U7	TPD4E110DPW	IEC61000-4-2 ESD tests
U5 & U6	TPD4E110DPW	ESD Clamping waveforms

2 Definitions

Contact Discharge — a method of testing in which the electrode of the ESD simulator is held in contact with the device-under-test (DUT).

Air Discharge — a method of testing in which the charged electrode of the ESD simulator approaches the DUT, and a spark to the DUT actuates the discharge.

ESD simulator — a device that outputs IEC61000-4-2 compliance ESD waveforms shown in Figure 1 with adjustable ranges shown in Table 2 and Table 3.

IEC61000-4-2 has 4 classes of protection levels. Classes 1 – 4 are shown in Table 2. Stress tests should be incrementally tested to level 4 as shown in Table 3 until the point of failure. If the DUT does not fail at 8-kV, testing can continue in 2-kV increments until failure.

Table 2. IEC61000-4-2 Test Levels

Contact Discharge Class	Test Voltage [± kV]	Air Discharge Class	Test Voltage [± kV]
1	2	1	2
2	4	2	4
3	6	3	8
4	8	4	15

Table 3. Waveform Parameters in Contact Discharge Mode

Stress Level Step	Simulator Voltage [kV]	Ipeak ±15% [A]	Rise Time ±25% [ns]	Current at 30 ns ±30% [A]	Current at 60 ns ±30% [A]
1	2	7.5	0.8	4	2
2	4	15	0.8	8	4
3	6	22.5	0.8	12	6
4	8	30	0.8	16	8

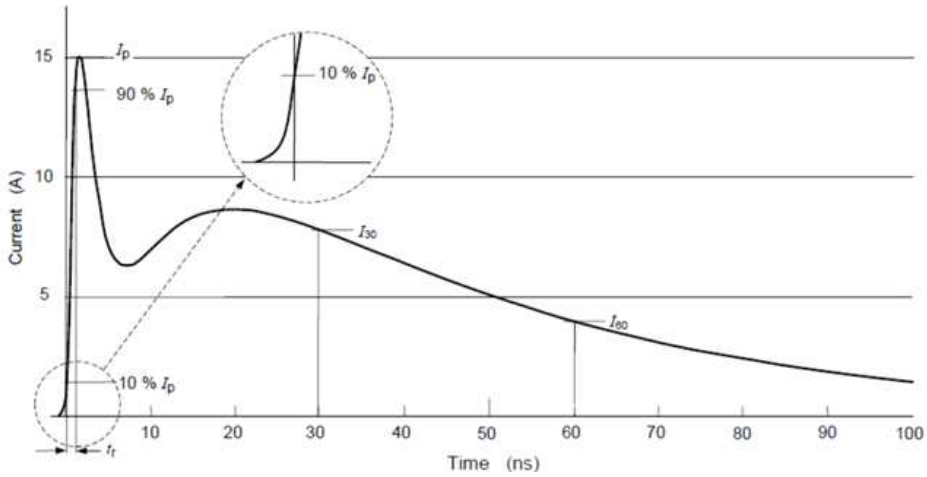


Figure 1. Ideal Contact Discharge Waveform of the Output Current of the ESD Simulator at 4-kV

3 Setup

This section describes the intended use of the EVM. A generalized outline of the procedure given in IEC-61000-4-2 is described here. IEC-61000-4-2 must be referred to for a more specific testing outline. Basic configurations for collecting S-parameters, Eye Diagrams, and ESD clamping waveforms are outlined as well.

3.1 Single Layer Routing on SSRX/SSTX

The two TPD4E110DPWs (U2 and U15) are configured with two USB 3.0 Type A male and female connectors (J3 & J4) for capturing Eye Diagrams. U2 is protecting the Super-Speed USB 3.0 Rx and Tx differential pairs and U15 is protecting the Hi-Speed D± pair. U15 uses two IO ports per signal line. Using J4 as input and J3 as output attach to a USB 3.0 compliant Eye Diagram tester setup for the intended application, either transmitter side or receiver side.

3.2 Double Layer Routing on SSRX/SSTX

The two TPD4E110DPWs (U1 and U14) are configured with two USB 3.0 Type A male and female connectors (J1 & J2) for capturing Eye Diagrams. U1 is protecting the Super-Speed USB 3.0 Rx and Tx differential pairs and U14 is protecting the Hi-Speed D± pair. U14 uses two IO ports per signal lines in the same fashion as U15. Using J2 as input and J1 as output attach to a USB 3.0 compliant Eye Diagram tester setup for the intended application, either transmitter side or receiver side.

3.3 U3 and U4

The two TPD4E110DPWs (U3 and U4) are each configured with 4 SMA connectors to allow 4-port analysis with a vector network analyzer. For U3 connect Port 1 to J5, Port 2 to J6, Port 3 to J7, and Port 4 to J8. For U4 connect Port 1 to J9, Port 2 to J10, Port 3 to J11, and Port 4 to J12. This configuration allows for the following terminology in 4 port analysis:

- S_{11}: Return loss
- S_{21}: Insertion loss
- S_{31}: Near end cross talk
- S_{41}: Far end cross talk

3.4 U5 – U13

The TPD4E110DPW (U5 – U13) can be used for destructive electrostatic discharge (ESD) pass-fail ESD strikes. Specifically, they can be used for both IEC-61000-4-2 air and contact discharge tests. The procedure in Section 3.4.1 ensures proper testing setup and method for both discharge tests. Each IO has a Test Pad (1 – 30) directly connected to it. U5 – U10 have each IO port pinned out separately. U11 – U13 have two IO ports connected in parallel per trace. This affords higher levels of ESD protection per signal line when the extra capacitance does not affect the signal integrity, as in USB 2.0 Hi-Speed signal lines.

3.4.1 Test Method and Set-Up

An example test setup is shown in Figure 2. Details of the testing table and ground planes can be found in the IEC 61000-4-2 test procedure. Ground the EVM using the banana connector labeled GND (J9). Discharge the ESD simulator on any of the Test Points TP1 – TP10. Contact and air-gap discharge are tested using the same simulator with the same discharge waveform. While the simulator is in direct contact with the test point during contact, it is not during air-gap.

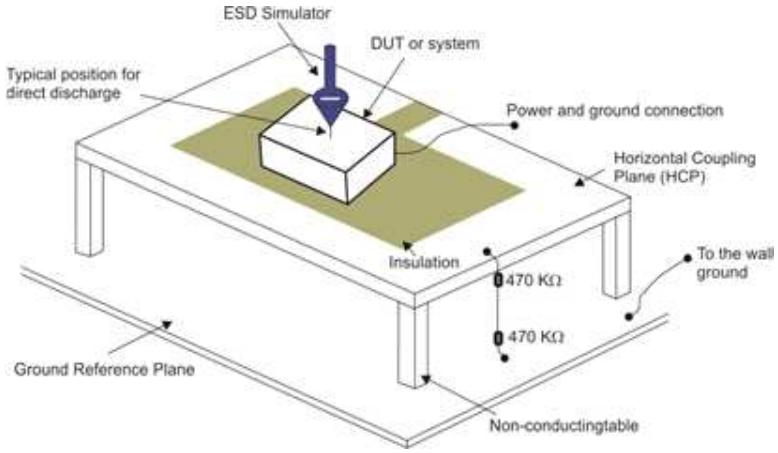


Figure 2. System Level ESD Test Setup

3.4.2 Evaluation of Test Results

Connect the tested device on the EVM to a curve tracer both before and after ESD testing. After each incremental level, if the IV curve of the ESD protection diode shifts ±0.1 V, or leakage current increases by a factor of ten, then the device is permanently damaged by ESD.

3.5 U9

One TPD4E110DPW (U9) also has an SMA (J13) connector for capturing clamping waveforms with an oscilloscope during an ESD strike. Caution must be taken when capturing clamping waveforms during an ESD event so as not to damage the oscilloscope.

3.5.1 Oscilloscope Setup

Capturing ESD clamping waveforms exposes the oscilloscope to potential voltages higher than the rating of the equipment. Proper methodology can mitigate any risk in this operation.

Recommended Equipment:

- Minimum of 1-GHz bandwidth oscilloscope.
- 1 10X 50Ω attenuator and 150 Ω resistor (already installed at R1).
- 50 Ω shielded SMB cable

Procedure:

In order to protect the oscilloscope, attenuation of the recorded signal is required. Here are two possible procedures for testing U5:

1. 1. Using one 10X attenuator:
   - Attach one 10X attenuator to the oscilloscope.
   - Attach the 50 Ω shielded SMB cable between J13 and the attenuator.
   - Set the scope attenuation factor to 30X.
   - Set the oscilloscope to trigger on a positive edge for (+) ESD and a negative edge for (–) ESD strikes. The magnitude must be set to 20 V.
   - Following Section 3.4.1, strike contact ESD to TP17.

   Recommended settings for the time axis is 20 ns/div and for the voltage axis is 5-V division.

   The voltage levels of the ESD applied to TP17 must not exceed ±8-kV while capturing clamping waveforms.

4 Board Layout

This section provides the TPD4E110DPWEVM board layout. The TPD4E110DPWEVM is a 4-layer board of FR-4 at 0.062” thickness. Layer 2 and 3 are ground planes and not shown here.

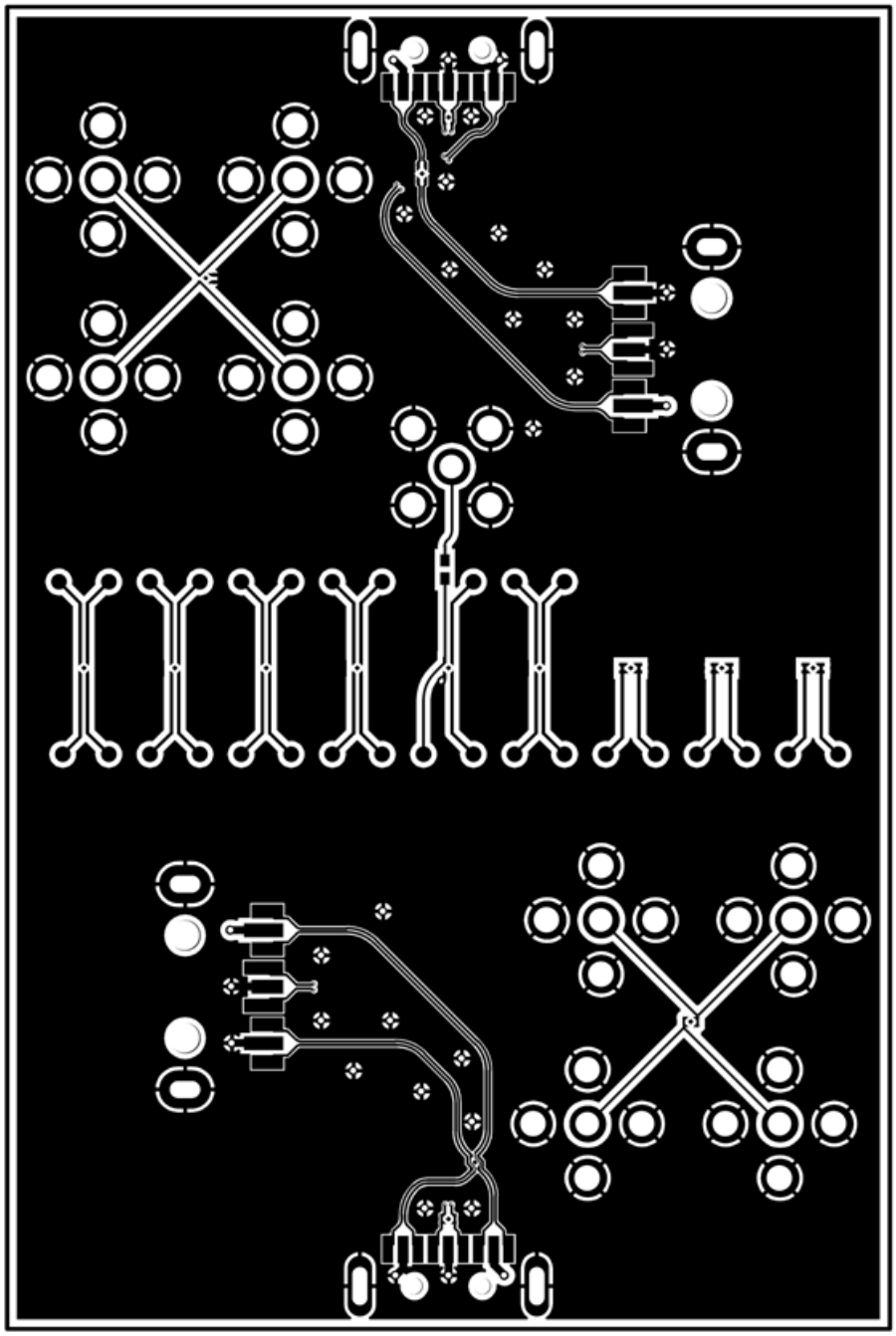


Figure 3. TPD4E110DPWEVM Top Layer

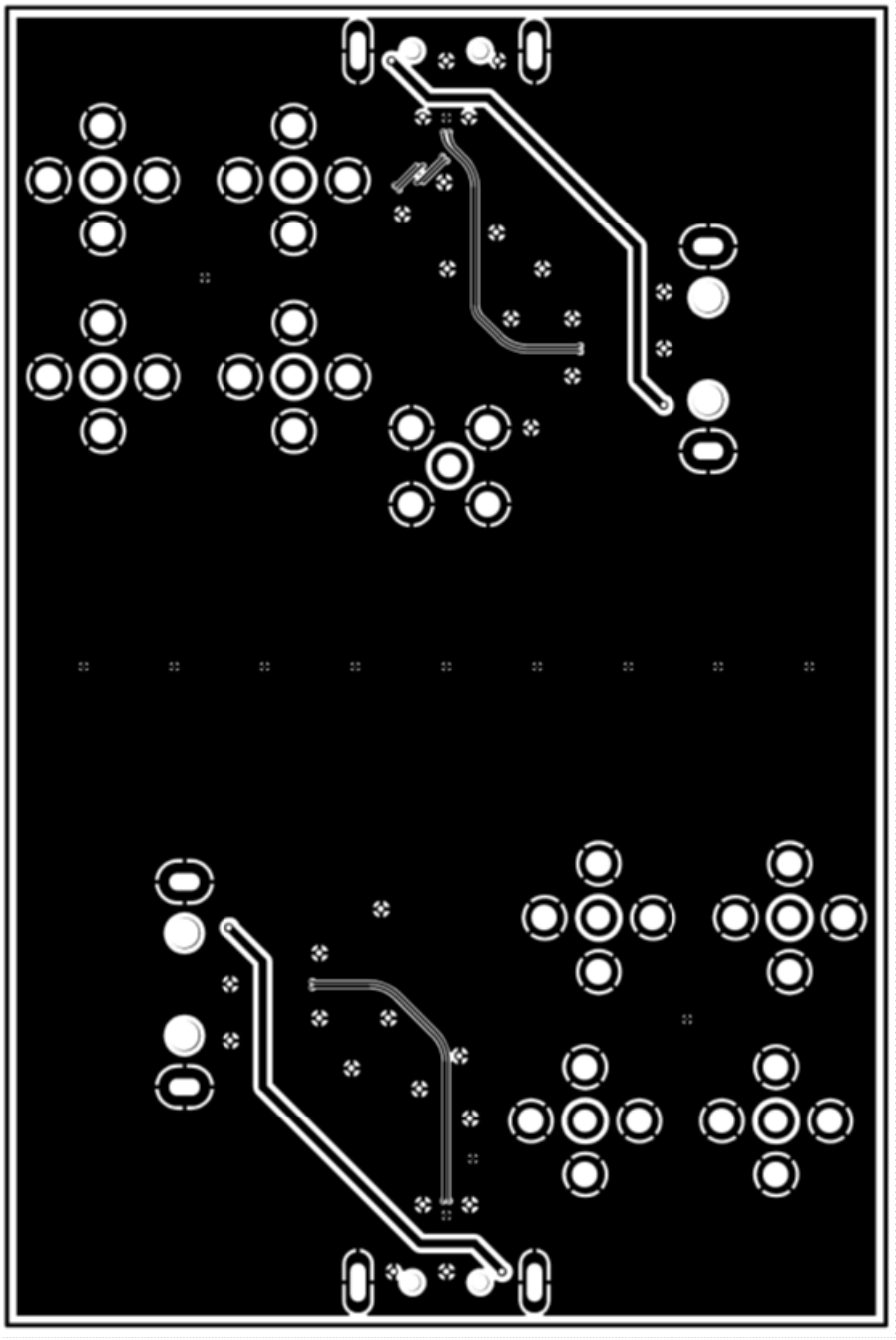


Figure 4. TPD4E110DPWEVM Bottom Layer

5 Schematic

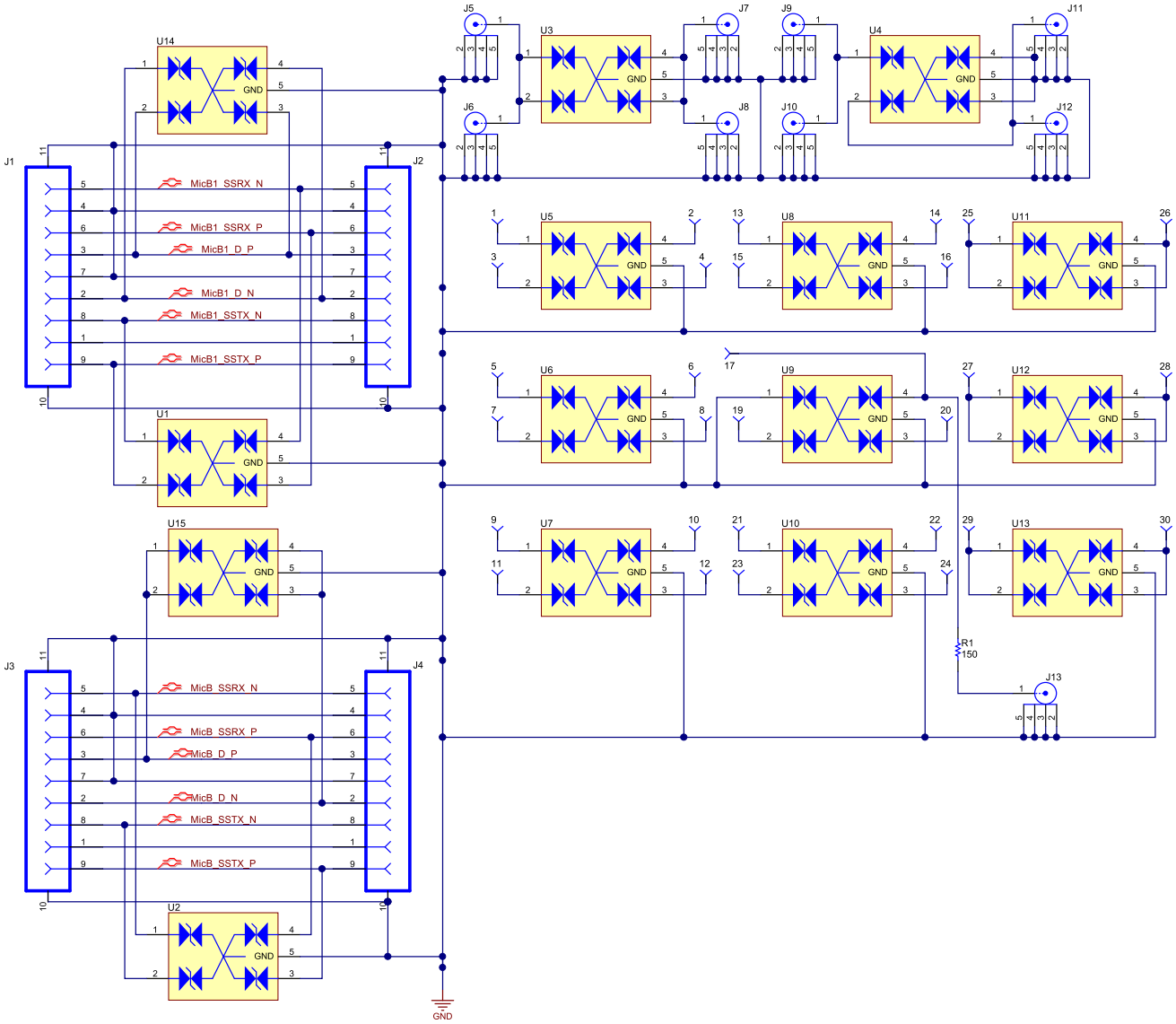


Figure 5. TPD4E110DPWEVM Schematic

6 Bill of Materials

Quantity	Reference Designator	Description	Size	Part Number	Manufacturer
2	J1, J3	Connector, SMT, USB 3.0 Horizontal Type A	12×15 mm	692 122 030 100	WE
2	J2, J4	Connector, SMT, USB 3.0 Plug With Clip Type A	12×21 mm	692 112 030 100	WE
9	J5, J6, J7, J8, J9, J10, J11, J12, J13	Connector, TH, SMA	6.4×9.5 mm	142-0701-231	Emerson Network Power
1	R1	RES, 150 Ω, 5%, 0.063 W, 0402	402	CRCW0402150 RJNED	Vishay-Dale
15	U1, U2, U3, U4, U5, U6, U7, U8, U9, U10, U11, U12, U13, U14, U15	4-CH Bidirectional Low Capacitance ESD Protection Device with 15-kV Contact and Ultra Low Clamping Voltage, DPW0004A	0.8×0.8 mm	TPD4E110DPW	Texas Instruments

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (March 2014) to A Revision **Page**

- Updated the Schematic in Section 5 8

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