

ABSTRACT

This user's guide describes the characteristics, operation, and use of the TPS65218 evaluation module (EVM). The TPS65218EVM is a fully assembled platform for evaluating the performance of the TPS65218 power management device. This document includes schematic diagrams, a printed-circuit-board (PCB) layout, and bill of materials (BOM).

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1 Introduction

The TPS65218 is a highly-integrated power management solution for ARM Cortex[®] Microprocessors. Features of the TPS65218 include:

- 2 battery backup supplies
- 3 Buck converters
- 1 Buck-Boost converter
- USB load switch
- General purpose LDO
- Low-voltage load switch
- High-voltage load switch

2 Requirements

2.1 Software

The EVM will power-up and operate without use of software. A GUI is supplied to provide a simple way to communicate to the device via I²C. The GUI can be downloaded from IPG-UI EVM GUI.

2.2 Host Computer

A computer with an available USB port is required to make use of the EVM software. The EVM software runs on the computer and communicates with the EVM via the USB2ANY interface.

2.3 Power Supply

A DC power supply capable of delivering up to 5 V and 3 A, and a coin cell battery or separate 3-V power supply for the backup supplies.



3 EVM Kit

The EVM kit (Figure 3-1) contains the following items:

- TPS65218 evaluation board
- USB2ANY adapter
- USB to USB micro cable
- 10-pin ribbon cable
- 30-pin ribbon cable



The 30-pin ribbon cable is not required for the TPS65218EVM.

Figure 3-1. TPS65218 EVM Kit

4 Schematic

Figure 4-1 illustrates the schematic for this EVM.



Figure 4-1. TPS65218 EVM Schematic



5 Terminal Block, Test Point, and Jumper Descriptions

Table 5-1. Terminal Block Descriptions						
Connector	Pin	Description	Note			
J1	GND	Ground	—			
	LS1	LS1 Output	—			
	EXT	External supply to LS1	Power Input (1.2 V – 3.3 V)			
J2	GND	Ground	—			
	IN_LS2	LS2 Input	Power Input (3.0 V – 5.5 V)			
	LS2	LS2 Output	—			
J3	GND	Ground	—			
	LDO1	LDO1 Output	Default 1.8 V			
	IN_LS3	LS3 Input	Power Input (1.8 V – 9.9 V)			
	LS3	LS3 Output	—			
J4	GND	Ground	—			
	GND	Ground	—			
	VSYS	DC Input	Power Input (2.7 V – 5.5 V)			
	CC	Coin Cell Battery Input	Power Input (2.2 V – 3.3 V)			
J5	GND	Ground	—			
	DC3	Buck 3 Output (DCDC3)	Default 1.2 V Output			
	DC2	Buck 2 Output (DCDC2)	Default 1.1 V Output			
	DC1	Buck 1 Output (DCDC1)	Default 1.1 V Output			
J6	GND	Ground	—			
	DC4	Buck-Boost Output (DCDC4)	Default 3.3 V Output			
	DC5	Battery Backup Supply Output (DCDC5)	1.0 V Output			
	DC6	Battery Backup Supply Output (DCDC6)	1.8 V Output			
J7	10-pin EVM connector for USB2ANY cable (I ² C communication)					

Table 5-2. Test Point Descriptions⁽¹⁾

	•
Test Point	Description
GND	Ground
INT_LDO	Internal bias voltage
nWAKEUP	Wakeup output signal
nINT	Interrupt output
nPFO	Power-fail comparator output
GPO2	General purpose output 2 or DDR reset output
GPIO3	General purpose output 3 or warm reset input
PGOOD	Power good
GPIO1	General purpose output 1
SYS_BU	Battery back-up power path output
PFI	Power-fail comparator input
IN_nCC	Output indicating power source for battery backup supplies
PGOOD_BU	Power good for backup supplies

(1) Test points are not designed to carry current, they are intended for measuring voltage.

Table 5-3. Jumper Descriptions

Jumper	Description	Default Position
JP1	Ties PWR_EN to VIO or GND	PWR_EN tied to VIO
JP2	Ties DC34_SEL pin to ground. Remove and jump with resistor for alternate voltage selections.	DC34_SEL tied to GND

Table 5-3. Jumper Descriptions (continued)

Jumper	Description	Default Position
JP3	Selects LS1 input between DCDC3 output and external supply from J1	IN_LS1 tied to DC3
JP4	Ties VIO to either DCDC4 output or 3.3-V supply from USB2ANY adaptor (J9). VIO supplies the pull-up voltage for the device I/Os.	VIO tied to V3p3
JP5	Ties AC_DET pin to either VSYS or GND. Tying to GND causes the device to start upon VSYS application.	AC_DET tied to VSYS



6 Setup

Figure 6-1 displays an example setup for using the TPS65218 EVM.





7



7 Software

7.1 Software Installation Instruction

A GUI is supplied to provide a simple way to communicate to the device via I²C. The GUI can be downloaded from: IPG-UI EVM GUI

Information on the installation of the IPG-UI can be found in the IPG-UI User's Guide.

You will also need to download the BOOSTXL-TPS65218 IPG-UI Device Support File. After you finish setting up the IPG-UI software, run the installer associated with your operating system to add the TPS65218 device file to your IPG-UI device library.

7.2 Using the TPS65218 GUI

Detailed information regarding the usage of the IPG-UI can also be found in the *IPG-UI User's Guide*. A brief overview is provided here for reference.

The proper device must first be selected from the "Select Devices" drop-down menu.

💈 IPGUI				- 0	ı x
	Open Project				
	Blank-12C-75R-1.0 File TPS56020-10 TPS56055-10 TPS560842-11 TPS560861-11 TPS560861-11	Open Recent Projects	X Clear Project History		
	TPS65030-1.0 TPS650341-1.1 Project TPS65217-1.2				
	TPS55218-1.1 TPS55218-1.2 TPS55291-8.1 TPS5591-0 TPS5591-1.0 TPS5912-1.1 Bank-12-7 Zhi-10 • C Create Project or I and Device Information from File	Create Project from Recent Devices	¥ Clear Device History		
	Select File				

Figure 7-1. GUI front Page

From there, the next screen is the device introduction page, which includes a brief overview as well as the functional block diagram for the device.

1PGUI - TPS65218D0		- a ×
File 👻 GUI Settings 👻	Report 💌	About 🥹
🗅 New Project 🕞 Open F	roject 🐵 Save Project 🐴 Save As Project	
Introduction	Introduction	Download Datasheet
Register Map	Introduction	
Single Register	The TPS65218D0 is a single chip power management IC, designed to support the Sitara AM437x processor and programmable to support a va characterized across a -40°C to 105°C temperature range, making it suitable for a wide range of industrial applications. TPS65218D0 comes i	iety of other processors in both portable (Li-lon battery) and line-powered (5-V supply) applications. The device is 1 a 48-pin QFN package (6-mm × 6-mm, .4-mm pitch) and a 48-pin QFP package (9-mm × 9-mm, 0.5-mm pitch).
Register Controls	Get Started	
Device Controls	TPS65218D0 Sitera AM335	× AM/37×
Adapter Controls	VSYS (2.7 V to 5.5 V) SYS BU	sor
Macros		
	+ CC DCDC5 25 mA CAP_VDD_RTC	
	GND Always-on back-up supplies	
	4/ IN_DCDCx 1.8 A 1.1 V	
	IN_LDO DCDC2	
	DCDC3 3.3 V	
	DCDC4 3.3V Analog and	/O
	400 mA 1.8 V	
	Regulators LDOT	
	Load Switches	
	from DCDC3 IN_LS1 0 LS1 380 mA VDDS_DDR	
	up to 5 V IN_LS2 LS2 500 mA LS3	
	1.8 V to 10 V IN LS3 O LS3 500 mA	
	AC_DET SCL SDA	
	PGOOD PWRONRSTn	
Transaction History		Hardware Connected Changes Written Hardware Source Changes Written

Figure 7-2. GUI Device Introduction

Finally, clicking on "Get Started" or on "Register Map" takes you to the I²C controls for the device sorted by register address.

1PGUI - TPS65218D0				- a ×
File 🔻 GUI Settings 👻	Report 👻			About 🕄
🗋 New Project 🛛 🗁 Open P	roject 🖺 Save Project 🖺 Save As Project			
Introduction	Read ALL Mills ALL Hadata Mada Magual + Autoroad Off +]	Q. Search
Register Map		Blue Boxes Indicate		
Single Register		Updated values		ENARI E1
Register Controls	I2C Address 0x24 • Read Group Write Group Order By address •	Pi		This register contains the device enable controls
Device Controls	Register Name	Adress 7 6 5 4	3 2 1 0 Value W R 10 s	DC6_EN R W
Adapter Controls	* CHIPID	0 0 0 0 0 0 0	0 1 0 1 05 R	
Macros	★ INT1	0x01 0 0 0 0	0 0 0 0 00 R	This group enables the DCDC6 converter
	★ INT2	0x02 0x0 0 0	0 0 0 0 00 R	DC5_EN R W
	★ INT_MASK1	0x03 0 0 0 0	0 0 0 0 00 W R	This group enables the DCDC5 converter
	★ INT_MASK2	0x04 0 0 0	000000 W R	DC4_EN R W
	★ STATUS	0x05 0 0 0 0	1000 <mark>08</mark> R	
	* CONTROL	0x06 0 0 0 0	0 0 0 0 00 W R	This group enables the DCDC4 converter
	★ FLAG	0x07 0 0 0 0	0 0 0 0 00 R	DC3_EN R W
	* PASSWORD	0×10 0 0 0 0	0 0 0 0 00 W R	This group enables the DCDC4 converter
	★ ENABLE1	0x11 0 0 1 1	1111 <mark>12E</mark> WR	DC2 EN R W
	★ ENABLE2	0x12 0 0 0 1	0 0 1 1 13 W R	
	★ CONFIG1	0x13 0 1 0 0	1 1 0 0 4C W R	This group enables the DCDC2 converter
	★ CONFIG2	0x14 1 1 0 0	0 0 0 0 CO W R	DC1_EN R W
	★ CONFIG3	0x15 0 0 0 0	0 0 0 0 00 W R	This group enables the DCDC1 converter
	* DCDC1	0x16 1 0 1 1	1 1 0 0 BC W R	
	* DCDC2	0x17 1 0 0 1	1 0 0 1 99 W R	
	+ DCDC3	0x18 1 0 0 0	1 1 0 0 8C W R	
	* DCDC4	0x19 1 0 1 1	0 0 1 0 B2 W R	
Dir: R ProtoAddr: 24 RegAddr	26 Data: 03 Seq: 2 🔺		Hardware Con	nnected Changes Written TEXAS INSTRUMENTS





1PGUI - TPS65218D0									– 🗆 ×
File 👻 GUI Settings 👻	Report 👻								About 🕄
🗅 New Project 🛛 🗁 Open Pr	roject 🖺 Save Project 🖺 Save	As Project							
Introduction	Lindata Mada Manual 🔹 Au	torood Off T Display Register M							
Register Map	ID Interrupt Statue C	Control Flag Config DCDC	Sequencer						
Single Register	ib interrupt Status C	Control Hag Coning DCDC	Sequencer						
Register Controls	PFM1 AR R W	DCDC1 🗆 AR R W	PFM2 AR R W	DCDC2 C AR R W	PFM3 AR R W	DCDC3 AR RW			Read ALL Write ALL
Device Controls	Enabled (lorde PWM)	- 1.600 V +	Enabled	- 1.100 V -	Enabled	- 1.200 V +	Register Name	Address 7 6	Bits 5 4 3 2 1 0 Value
Adapter Controls	This group controls DCDC1 pulse frequency modulation	This group controls DCDC1	This group controls DCDC2 pulse frequency modulation	This group controls DCDC2	This group controls LDO1 pulse frequency modulation	This group controls DCDC3	DCDC1	0x16 1 0	1 1 1 1 0 0 BC
Macros		ourput vonage setting		output vonage setting		output vonage setting	DCDC2	0x17 1 0	0 1 1 0 0 1 99
	Disabled (force PWM)	DCDC4 AR R W	O O A R W No Change	GODSBL AR R W Enabled	SLEW AR R W		DCDC3	0x18 1 0	0 0 1 1 0 0 8C
	Enabled This group controls DCDC4	- 3.300 V +	 Initiate change from present state to new setting. 	 Disabled. DCDC1 and DCDC2 output voltage changes 	This group controls the output	- 1.800 V +	DCDC4	0x19 1 0	1 1 0 0 1 0 B2
	pulse frequency modulation	This group controls DCDC4 output voltage setting	SLEW setting does apply This group controls DCDC1 and	without having to write the GO bit. SLEW setting does apply	slew rate setting	This group controls LDO1 output voltage setting	SLEW	0x1A 0 0	0 0 0 1 1 0 06
			DCDC2 output voltage	This group controls GO bit			LD01	0x1B 0 0	0 1 1 1 1 1 IF
Dir: R ProtoAddr: 24 RegAddr:	: 26 Data: 03 Seq: 2 🔺					Hardware Co	nnected Char	iges Written ●	👋 Texas Instruments

Figure 7-4. GUI Register Controls

With this information, it is possible to begin evaluating the TPS65218 device.





8 Bill of Materials

Table 8-1 lists the BOM for this EVM.

Designator	Description	Value	Voltage Rating	Dielectric	Footprint	Qty.	Manufacturer	Manufacturer PN
C1, C3, C4	Capacitor	10µ	16V	X5R	805	3	MuRata	GRM21BR61C106KE15L
C8	Capacitor	10µ	6.3 V	X7R	805	1	ток	C2012X7R0J106K125AB
C2, C5–C7, C11, C12, C14, C17– C19	Capacitor	4.7µ	10V	X7R	805	10	ТDК	C2012X7R1A475K125AC
C10, C16, C23– C26	Capacitor	10µ	10V	X7R	805	6	TDK	C2012X7R1A106K125AC
C9, C21, C22	Capacitor	100n	100V	X5R	805	3	ток	C2012X5R2A104K125AA
C13	Capacitor	4.7µ	25V	X5R	805	1	ТDК	C2012X5R1E475K125AB
C15	Capacitor	10µ	16V	X7R	805	1	Samsung	CL21B106KOQNNNE
C28	Capacitor	47µ	10V	X5R	805	1	ТDК	C2012X5R1A476M125AC
C20	Capacitor	1μ	10V	X7R	805	1	ТDК	C2012X7R1A105K
C27	Capacitor	470µ	25V		CAP_EEE Size G	0	Panasonic	EEE1EA471UAP
C29, C30, C31, C32	Capacitor	68µ	16V		6032	0	Kemet	B45197A3686+30
L1, L2, L3, L4	Inductor	1.5µ			IND_SPM3012	4	ТDК	SPM3012T-1R5M
L5, L6	Inductor	10µ			805	2	ток	MLZ2012N100LT
R1, R2, R4, R6, R9, R10, R12, R19, R20, R21	Resistor	100K			603	10	Vishay-Dale	CRCW0603100KFKEA
R3, R5, R7, R8, R11, R23, R24	Resistor	0			805	7	Vishay-Dale	CRCW08050000Z0EAHP
R13–R18	Resistor	1K			603	0	Vishay-Dale	CRCW06031K00FKEA
R22	Resistor	10			603	1	Vishay-Dale	CRCW060310R0JNEAHP
R25, R26	Resistor	4.75K			603	2	Vishay-Dale	CRCW06034K75FKEA
S1	Switch		32V		6.3x5.36x6.6 mm	1	C&K Components	KT11P2JM34LFS
U1	PMIC				RSL (S-PQFP-N48) 0.4 pitch	1	Texas Instruments	TPS65218D0

Table 8-1. Bill of Materials



9 Layout

Figure 9-1 through Figure 9-6 illustrate the PCB layouts for the evaluation module.



Figure 9-1. Top Layer Silkscreen



Figure 9-2. Top Layer



Figure 9-3. Ground Plane



Figure 9-4. Mid Layer





Figure 9-5. Bottom Layer



Figure 9-6. Bottom Layer Silkscreen

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (August 2022) to Revision B (October 2022)		Page
•	Updated EVM Schematic	4
•	Updated Bill of Materials	11
Changes from Revision * (November 2014) to Revision A (August 2022)		Page
•	Updated the numbering format for tables, figures, and cross-references throughout the document	1
•	Changed GUI description	2
•	Updated link to software	2
•	Changed links to GUI and supporting hardware	8
•	Updated descriptions	8
•	Changed topic title	8
•	Changed steps to use GUI	8
•	Added new images	8
•	Updated software links	8

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