User's Guide

TPS54334 Step-Down Converter Evaluation Module User's Guide

ABSTRACT

This user's guide contains background information for the TPS54334 as well as support documentation for the TPS54334EVM-722 evaluation module (PWR722-001). The user's guide also includes performance specifications, the schematic, and the bill of materials for the TPS54334EVM-722.

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1 Introduction

This user's guide contains background information for the TPS54334 as well as support documentation for the TPS54334EVM-722 evaluation module (PWR722-001). Also included are the performance specifications, the schematic, and the bill of materials for the TPS54334EVM-722.

1.1 Background

The TPS54334 dc/dc converter is designed to provide up to a 3-A output from an input voltage source of 4.2 V to 28 V. Rated input voltage and output current range for the evaluation module are given in Table 1-1. This evaluation module is designed to demonstrate the small printed-circuit-board areas that may be achieved when designing with the TPS54334 regulator. The switching frequency is externally set at a nominal 570 kHz. The high-side and low-side MOSFETs are incorporated inside the TPS54334 package along with the gate-drive circuitry. The low drain-to-source on resistance of the MOSFETs allow the TPS54334 to achieve high efficiencies and helps keep the junction temperature low at high output currents. The compensation components are external to the integrated circuit (IC), and an external divider allows for an adjustable output voltage. Additionally, the TPS54334 provides an adjustable undervoltage lockout input. The absolute maximum input voltage is 30 V for the TPS54334EVM-722.

Table 1-1. Input Voltage and Output Current Summary

EVM	INPUT VOLTAGE RANGE	OUTPUT CURRENT RANGE
TPS54334EVM-722	VIN = 4.2 V to 28 V	0 A to 3 A

1.2 Performance Specification Summary

A summary of the TPS54334EVM-722 performance specifications is provided in Table 1-2. Specifications are given for an input voltage of V_{IN} = 24 V and an output voltage of 5.0 V, unless otherwise specified. The TPS54334EVM-722 is designed and tested for V_{IN} = 4.2 V to 28 V. The ambient temperature is 25°C for all measurements, unless otherwise noted.

Table 1-2. TPS54334EVM-722 Performance Specification Summary

Specification	Test Conditions		MIN	TYP	MAX	Unit
V_{IN} operating voltage range			4.2	24	28	V
V_{IN} start voltage				4.1		V
V_{IN} stop voltage				3.9		V
Output voltage set point				3.3		V
Output current range(1)	V_{IN} = 4.2 V to 28 V		0		3	A
Line regulation	I_O = 1.5 A, V_{IN} = 4.2 V to 28 V			±0.05%		
Load regulation	V_{IN} = 12 V, I_O = 0 A to 3 A			±0.2%		
Load transient response	I_O = 0.75 A to 2.25 A	Voltage change		–190		mV
		Recovery time		150		µs
	I_O = 2.25 A to 0.75 A	Voltage change		190		mV
		Recovery time		150		µs
Loop bandwidth	V_{IN} = 24 V, I_O = 1.5 A			54.26		kHz
Phase margin	V_{IN} = 24 V , I_O = 1.5 A			82		°
Input ripple voltage	I_O = 3 A			400		mV_{PP}
Output ripple voltage	I_O = 3 A			<30		mV_{PP}
Output rise time				2		ms
Operating frequency				570		kHz
Maximum Efficiency	TPS54334EVM-722, V_{IN} = 12 V, I_O = 1 A			91.38%		

(1) When V_{IN} = 4.2 V, maximum I_{OUT} is 2 A.

1.3 Modifications

These evaluation modules are designed to provide access to the features of the TPS54334. Some modifications can be made to this module.

1.3.1 Output Voltage Set Point

The voltage divider, R5 and R6, is used to set the output voltage. To change the output voltage of the EVM, it is necessary to change the value of resistor R6. Changing the value of R6 can change the output voltage above 0.8 V. The value of R6 for a specific output voltage can be calculated using Equation 1. Use 31.6 kΩ for R5.

$$R6 = \frac{R5 \times 0.8\ V}{V_{OUT} - 0.8\ V} \tag{1}$$

Table 1-3 lists the R5 and R6 values for some common output voltages. Note that V_{IN} must be in a range so that the minimum on-time is greater than 145 ns, and the maximum duty cycle is less than 100%. The values given in Table 1-3 are standard values, not the exact value calculated using Equation 1.

Table 1-3. Output Voltages Available

Output Voltage (V)	R5 Value (kΩ)	R6 Value (kΩ)
1.8	31.6	25.5
2.5	31.6	15
3.3	31.6	10

1.3.2 Adjustable UVLO

The under voltage lock out (UVLO) can be adjusted externally using R1 and R2. The EVM is set for a start voltage of 4.1 V and a stop voltage of 3.23 V using R1 = 220 kΩ and R2 = 84.5 kΩ. Use Equation 2 and Equation 3 to calculate required resistor values for different start and stop voltages. Considering the V_{IN} UVLO, the stop voltage is set to 3.9 V.

$$R1 = \frac{V_{START}\left(\frac{V_{ENFALLING}}{V_{ENRISING}}\right) - V_{STOP}}{I_p\left(1 - \frac{V_{ENFALLING}}{V_{ENRISING}}\right) + I_h} \tag{2}$$

$$R2 = \frac{R1 \times V_{ENFALLING}}{V_{STOP} - V_{ENFALLING} + R1\left(I_p + I_h\right)} \tag{3}$$

I_p = 1.15 µA, I_h = 3.3 µA, $V_{ENFALLING}$ = 1.17 V and $V_{ENRISING}$ = 1.21 V

2 Test Setup and Results

This section describes how to properly connect, set up, and use the TPS54334EVM-722 evaluation module. The section also includes test results typical for the evaluation module and covers efficiency, output voltage regulation, load transients, loop response, output ripple, input ripple, and start-up.

2.1 Input/Output Connections

The TPS54334EVM-722 is provided with input/output connectors and test points as shown in Table 2-1. A power supply capable of supplying 2 A must be connected to J1 through a pair of 20-AWG wires. The load must be connected to J4 through a pair of 20-AWG wires. The maximum load current capability must be at least 4 A to use the full capability of this EVM. Wire lengths must be minimized to reduce losses in the wires. Test-point TP1 provides a place to monitor the V_{IN} input voltages with TP2 providing a convenient ground reference. TP6 is used to monitor the output voltage with TP7 as the ground reference.

Table 2-1. EVM Connectors and Test Points

Reference Designator	Function
J1	VIN (see Table 1-1 for V_{IN} range)
J2	VOUT, 3.3 V at 3 A maximum
JP1	2-pin header for enable. Connect EN to ground to disable, open to enable.
JP2	2-pin header for V_{DD}. Connect VOUT to V_{DD} as the power supply.
TP1	V_{IN} test point at VIN connector
TP2	GND test point at VIN
TP3	PGOOD test point
TP4	PH test point
TP5	Test point between voltage divider network and output. Used for loop response measurements.
TP6	Output voltage test point at OUT connector
TP7	GND test point at VOUT connector
TP8	V_{DD} test point at the VDD connector
TP9	GND test point at the VDD connector
TP10	EN test point

2.2 Efficiency

The efficiency of this EVM peaks at a load current of about 0.5 A – 1 A, and then decreases as the load current increases towards full load. Figure 2-1 shows the efficiency for the TPS54334EVM-722 at an ambient temperature of 25°C.

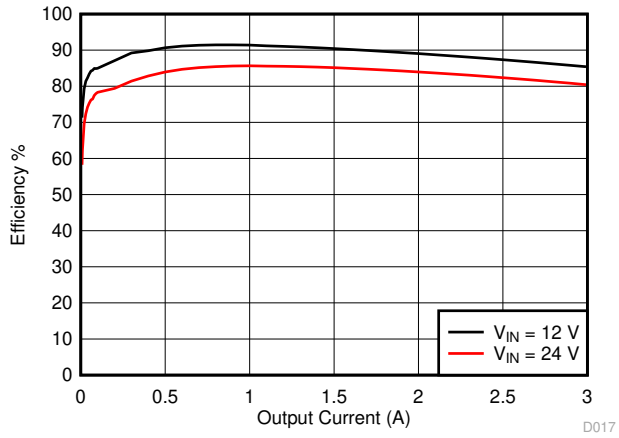

Figure 2-1. TPS54334EVM-722 Efficiency

Figure 2-2 shows the efficiency for the TPS54334EVM-722 on a semi-log scale to better show light load efficiency. The ambient temperature is 25°C.

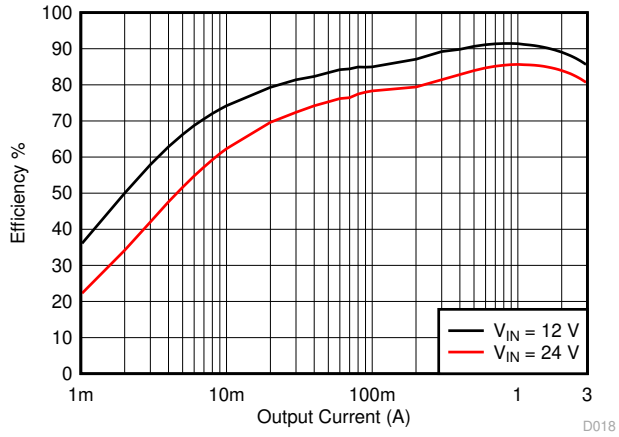

Figure 2-2. TPS54334EVM-722 Low Current Efficiency

The efficiency may be lower at higher ambient temperatures, due to temperature variation in the drain-to-source resistance of the internal MOSFET.

2.3 Output Voltage Load Regulation

Figure 2-3 shows the load regulation for the TPS54334EVM-722.

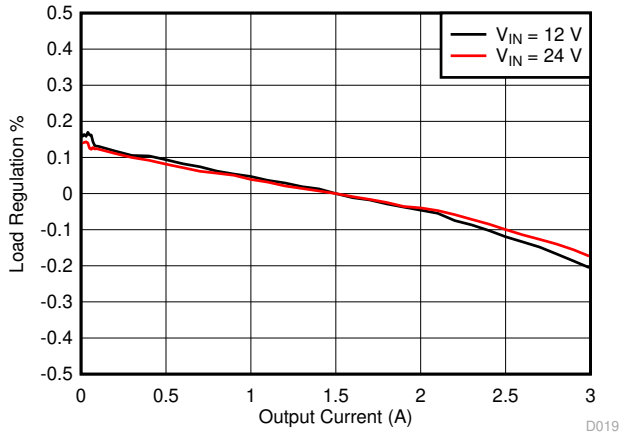

Figure 2-3. TPS54334EVM-722 Load Regulation

Measurements are given for an ambient temperature of 25°C.

2.4 Output Voltage Line Regulation

Figure 2-4 shows the line regulation for the TPS54334EVM-722.

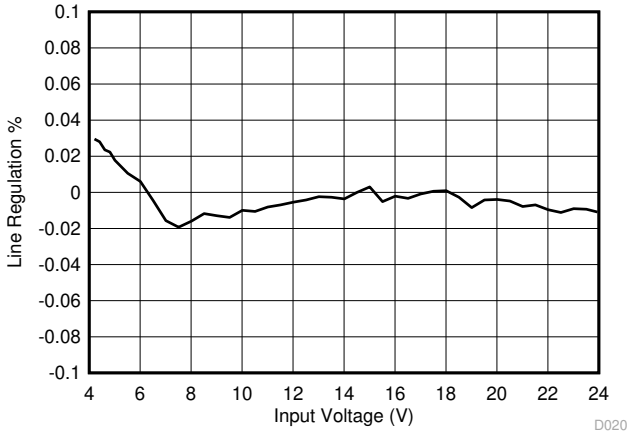

Figure 2-4. TPS54334EVM-722 Line Regulation

2.5 Load Transients

Figure 2-5 shows the TPS54334EVM-722 response to load transients. The current step is from 25% to 75% of maximum rated load at 12-V input. Total peak-to-peak voltage variation is as shown, including ripple and noise on the output.

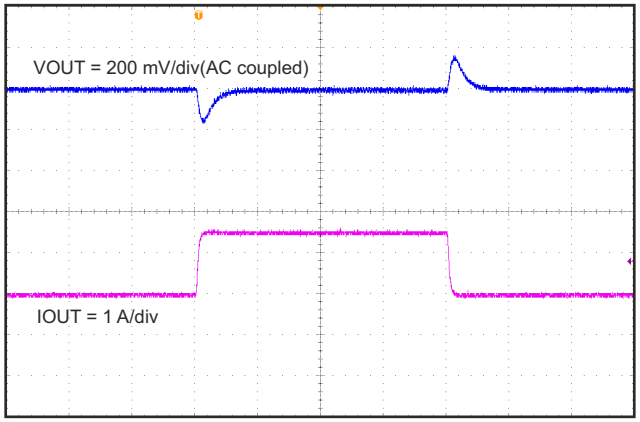

Figure 2-5. TPS54334EVM-722 Transient Response

2.6 Loop Characteristics

Figure 2-6 shows the TPS54334EVM-722 loop-response characteristics. Gain and phase plots are shown for V_{IN} voltage of 24 V. Load current for the measurement is 1.5 A.

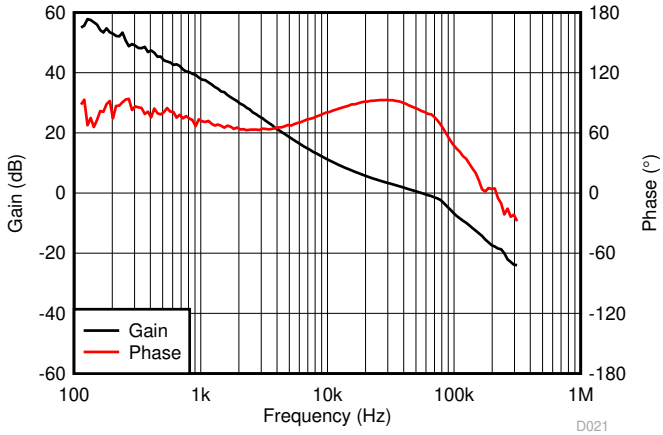

Figure 2-6. TPS54334EVM-722 Loop Response

2.7 Output Voltage Ripple

Figure 2-7, Figure 2-8, and Figure 2-9 show the TPS54334EVM-722 output voltage ripple for full load, light load, and skip mode operation. V_{IN} = 12 V. The output The ripple voltage is measured directly across the output capacitors.

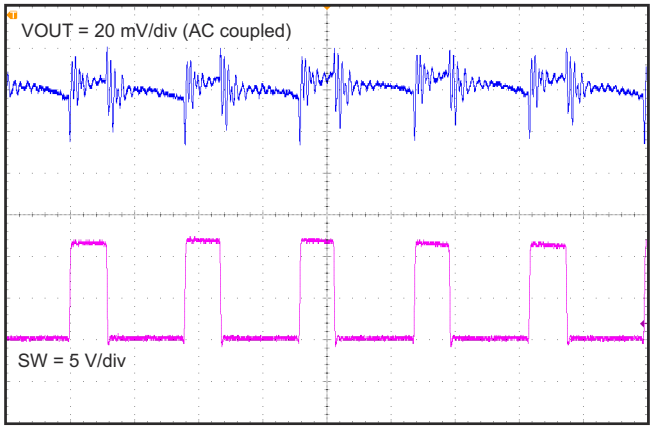

Figure 2-7. TPS54334EVM-722 Output Ripple, I_{OUT} = 3 A

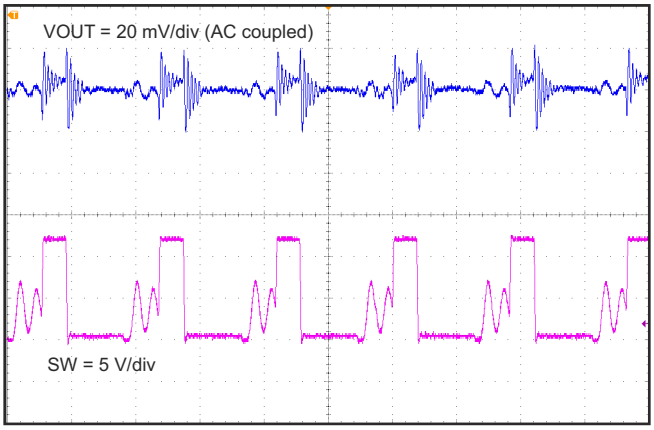

Figure 2-8. TPS54334EVM-722 Output Ripple, I_{OUT} = 200 mA

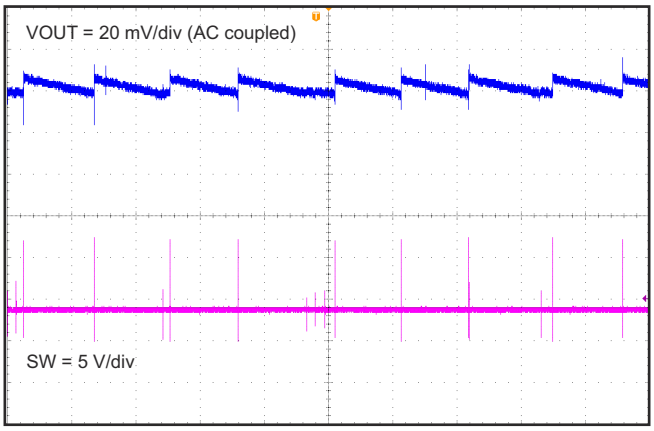

Figure 2-9. TPS54334EVM-722 Output Ripple, I_{OUT} = 0 A

2.8 Input Voltage Ripple

Figure 2-10 shows the TPS54334EVM-722 input voltage ripple. The output current is the rated full load of 3 A and V_{IN} = 12 V. The ripple voltage is measured directly across the input capacitors.

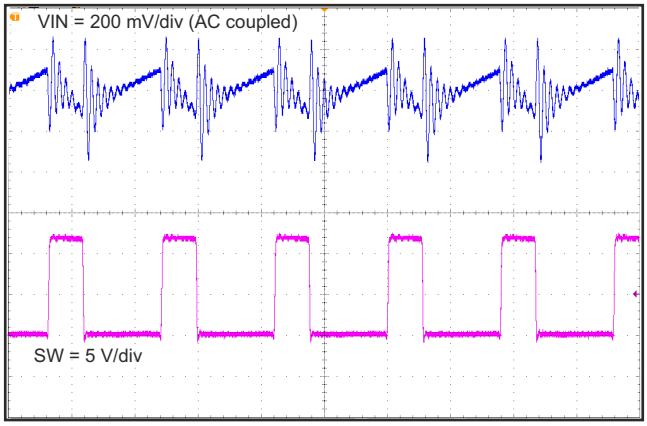

Figure 2-10. TPS54334EVM-722 Input Ripple

2.9 Powering Up

Figure 2-11 and Figure 2-12 show the start-up waveforms for the TPS54334EVM-722. In Figure 2-11, the output voltage ramps up as soon as the input voltage reaches the UVLO threshold as set by the R1and R2 resistor divider network. In Figure 2-12, the input voltage is initially applied and the output is inhibited by using a jumper at JP1 to tie EN to GND. When the jumper is removed, EN is released. When the EN voltage reaches the enable-threshold voltage, the start-up sequence begins and the output voltage ramps up to the externally set value of 3.3 V. The input voltage for these plots is 12 V and the load is 5 Ω.

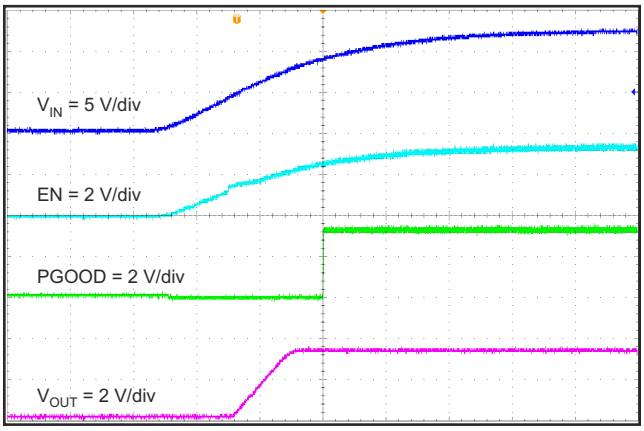

Figure 2-11. TPS54334EVM-722 Startup Relative to V_{IN}

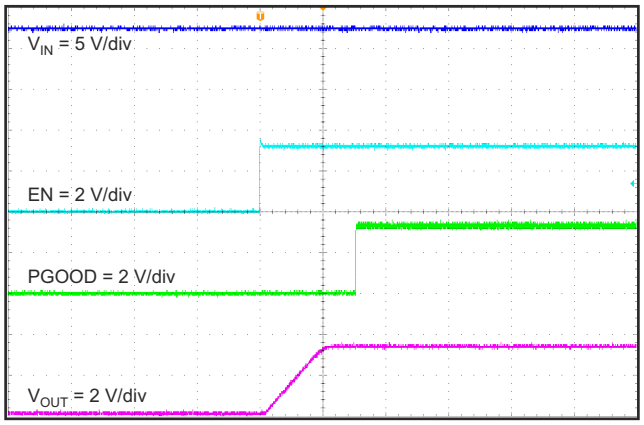

Figure 2-12. TPS54334EVM-722 Startup Relative to Enable

2.10 Powering Down

Figure 2-13 and Figure 2-14 show the start-up waveforms for the TPS54334EVM-722. In Figure 2-13, the output voltage ramps down as soon as the input voltage falls below the UVLO stop threshold as set by the R1 and R2 resistor divider network. In Figure 2-14, the output is inhibited by using a jumper at JP1 to tie EN to GND. The input voltage for these plots is 12 V and the load is 2.2 Ω.

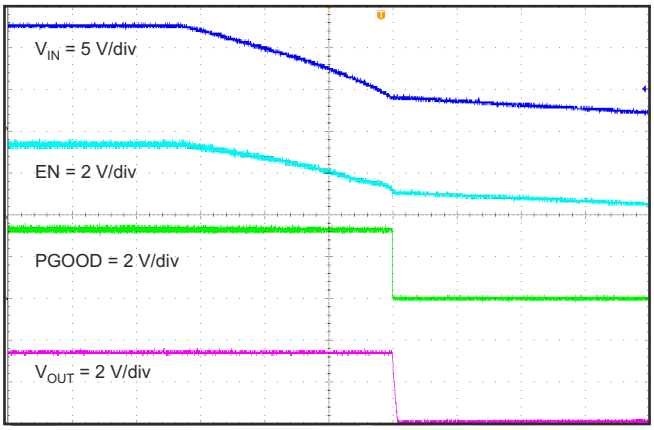

Figure 2-13. TPS54334EVM-722 Shutdown Relative to V_{IN}

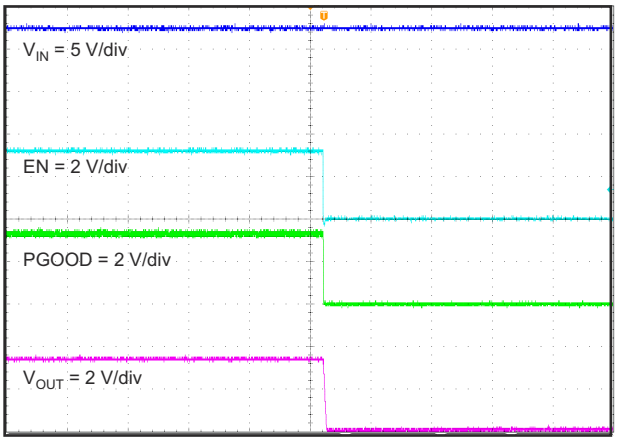

Figure 2-14. TPS54334EVM-722 Shutdown Relative to EN

3 Board Layout

This section provides a description of the TPS54334EVM-722, board layout, and layer illustrations.

3.1 Layout

Figure 3-1 through Figure 3-3 show the board layout for the TPS54334EVM-722. The topside layer of the EVM is laid out in a manner typical of a user application. The top and bottom layers are 2-oz. copper.

The top layer contains the main power traces for V_{IN}, V_{OUT}, and VPHASE. Also on the top layer are connections for the remaining pins of the TPS54334 and a large area filled with ground. To facilitate the placement of the main input bypass capacitor as close to the V_{IN} and GND pins as possible, the trace for VPHASE is routed to the bottom layer immediately at the pin 3 connection. It is routed back to the top layer at the L1 inductor and C3 BOOT capacitor. The bottom layer contains a ground plane plus a copper fill area for VPHASE, an etch run to connect the upper resistor of the voltage set point divider to the regulation point at the J2 output connector, and a trace to connect the upper resistor of the UVLO set point divider network to V_{IN}. The top-side ground areas are connected to the bottom and internal ground planes with multiple vias placed around the board including four vias directly under the TPS54334 device to provide a thermal path from the top-side ground area to the bottom-side and internal ground planes.

The input decoupling capacitors (C2, and C1) and bootstrap capacitor (C3) are all located as close to the IC as possible. In addition, the voltage set-point resistor divider components are also kept close to the IC. For the TPS54334, an additional input bulk capacitor may be required, depending on the EVM connection to the input supply.

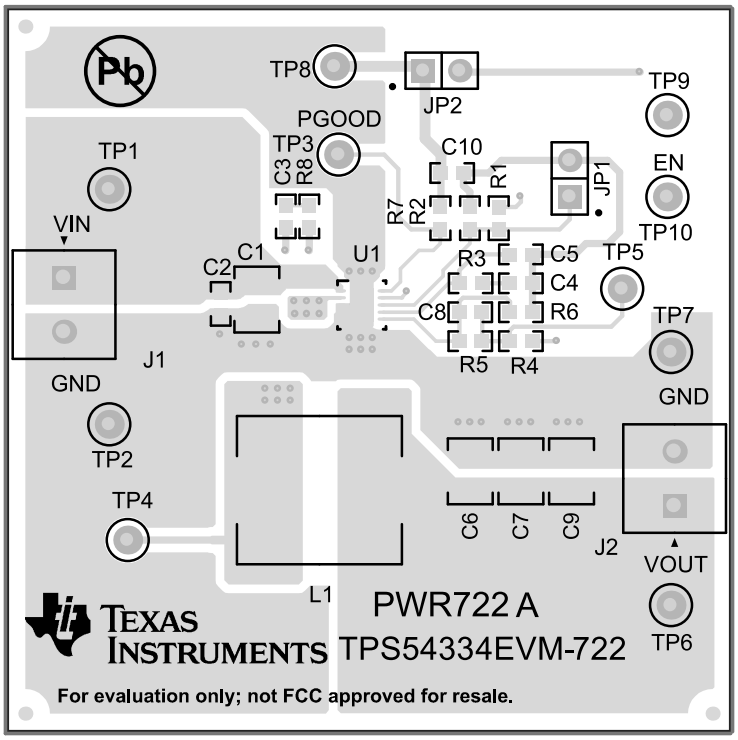

Figure 3-1. TPS54334EVM-722 Top-Side Assembly

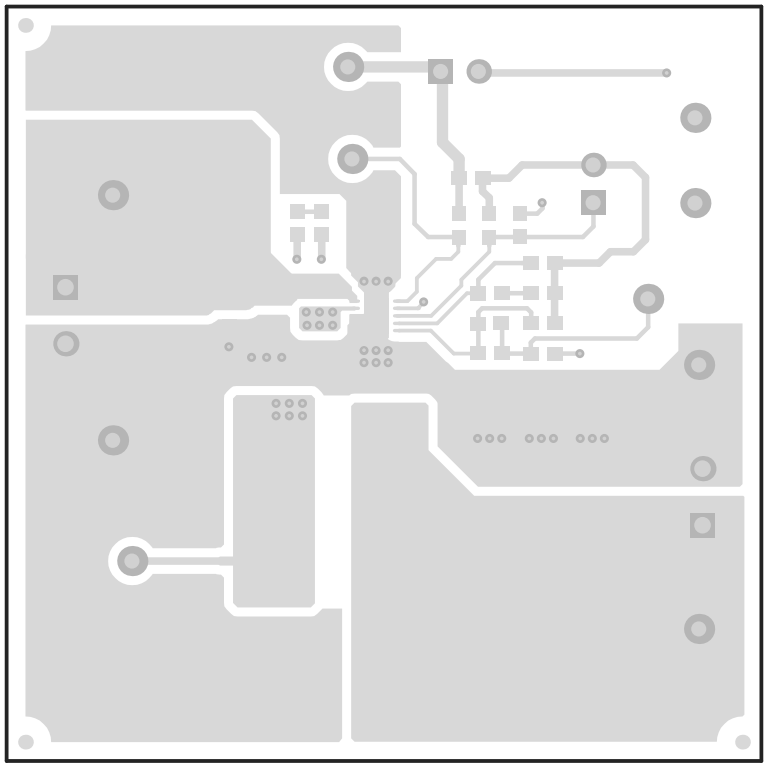

Figure 3-2. TPS54334EVM-722 Top-Side Layout 3

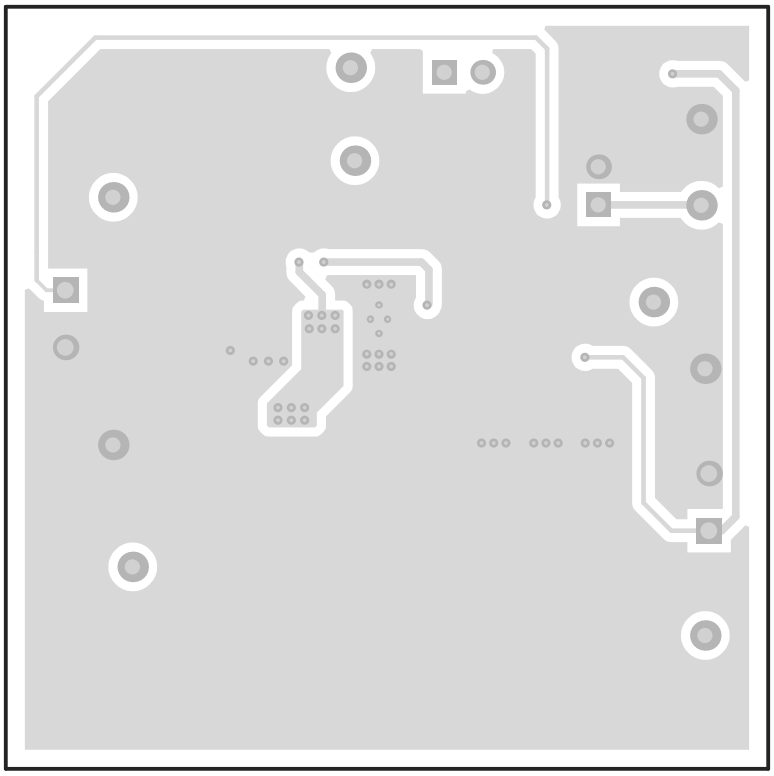

Figure 3-3. TPS54334EVM-722 Bottom-Side Layout

4 Schematic and Bill of Materials

This section presents the TPS54334EVM-722 schematic and bill of materials.

4.1 Schematic

Figure 4-1 is the schematic for the TPS54334EVM-722.

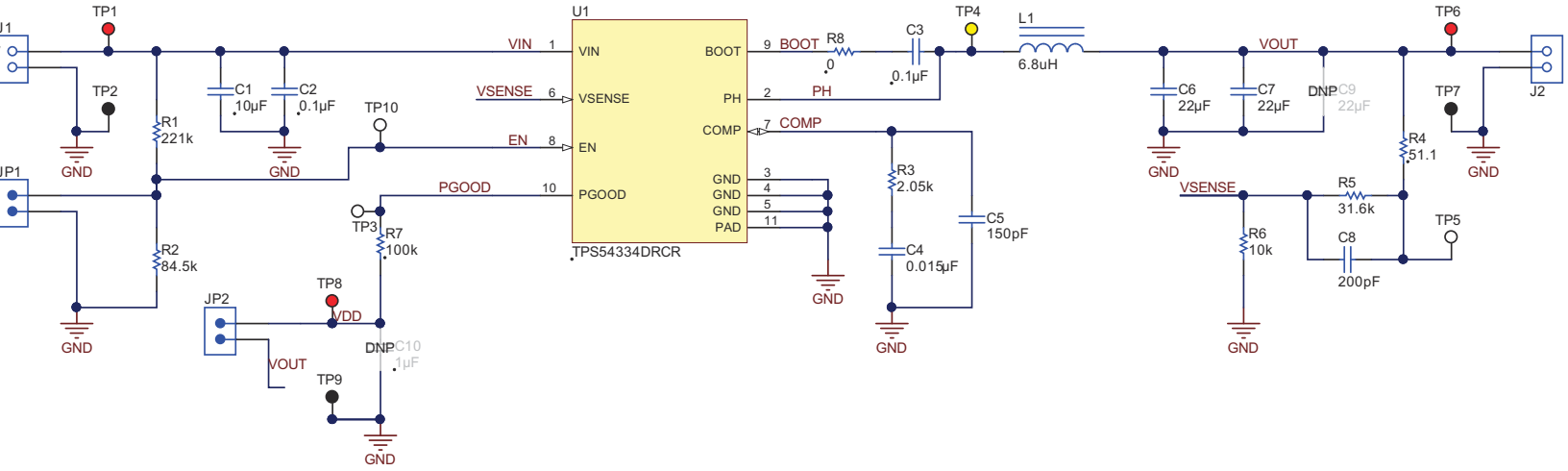

Figure 4-1. TPS54334EVM-722 Schematic

4.2 Bill of Materials

Table 4-1 presents the bill of materials for the TPS54334EVM-722.

Table 4-1. TPS54334EVM-722 Bill of Materials

Designator	Qty	Value	Description	Package Reference	Part Number	Manufacturer
C1	1	10 µF	CAP, CERM, 10 µF, 35 V, ±10%, X7R, 1210	1210	GRM32ER7YA106KA12L	Murata
C2, C3	2	0.1 µF	CAP, CERM, 0.1 µF, 50 V, ±10%, X7R, 0603	0603	GRM188R71H104KA93D	Murata
C4	1	0.015 µF	CAP, CERM, 0.015 µF, 50 V, ±10%, X7R, 0603	0603	GRM188R71H153KA01D	Murata
C5	1	150 pF	CAP, CERM, 150 pF, 50 V, ±5%, C0G/NP0, 0603	0603	GRM1885C1H151JA01D	Murata
C6, C7	2	22 µF	CAP, CERM, 22 µF, 25 V, ±10%, X7R, 1210	1210	GRM32ER71E226KE15L	Murata
C8	1	200pF	CAP, CERM, 200 pF, 50 V, ±5%, C0G/NP0, 0603	0603	GRM1885C1H201JA01D	Murata
J1, J2	2	2 × 1	Conn Term Block, 2POS, 3.81 mm, TH	PhoenixConact_1727010	1727010	Phoenix Contact
JP1, JP2	2		Header, TH, 100mil, 2 × 1, Gold plated, 230 mil above insulator	TSW-102-07-G-S	TSW-102-07-G-S	Samtec, Inc.
L1	1	6.8 µH	Inductor, Shielded, Powdered Iron, 6.8 µH, 8 A, 0.0233 Ω, SMD	IHLP-4040DZ	IHLP4040DZER6R8M01	Vishay-Dale
R1	1	221 k	RES, 221 k, 1%, 0.1 W, 0603	0603	RC0603FR-07221KL	Yageo America
R2	1	84.5 k	RES, 84.5 k, 1%, 0.1 W, 0603	0603	CRCW060384K5FKEA	Vishay-Dale
R3	1	2.05 k	RES, 2.05 k, 1%, 0.1 W, 0603	0603	CRCW06032K05FKEA	Vishay-Dale
R4	1	51.1	RES, 51.1 Ω, 1%, 0.1W, 0603	0603	CRCW060351R1FKEA	Vishay-Dale
R5	1	31.6 k	RES, 31.6 k, 1%, 0.1 W, 0603	0603	CRCW060331K6FKEA	Vishay-Dale
R6	1	10 k	RES, 10 k, 5%, 0.1 W, 0603	0603	CRCW060310K0JNEA	Vishay-Dale
R7	1	100 k	RES, 100 k, 0.1%, 0.063 W, 0603	0603	CPF0603B100KE	TE Connectivity
R8	1	0	RES, 0 Ω, 5%, 0.1W, 0603	0603	CRCW06030000Z0EA	Vishay-Dale
SH-JP1	1	1 × 2	Shunt, 100mil, Gold plated, Black		382811-6	AMP
TP1, TP6, TP8	3	Red	Test Point, TH, Miniature, Red	Keystone5000	5000	Keystone
TP2, TP7, TP9	3	Black	Test Point, TH, Miniature, Black	Keystone5001	5001	Keystone
TP3, TP5, TP10	3	White	Test Point, TH, Miniature, White	Keystone5002	5002	Keystone
TP4	1	Yellow	Test Point, TH, Miniature, Yellow	Keystone5004	5004	Keystone
U1	1		4.2-V TO 28-V INPUT, 3A OUTPUT, SYNCHRONOUS SWIFT™ STEP DOWN VOLTAGE CONVERTER, DRC0010J	DRC0010J	TPS54334DRCR	Texas Instruments
C9	0	22 µF	CAP, CERM, 22 µF, 25 V, ± 10%, X7R, 1210	1210	GRM32ER71E226KE15L	Murata
C10	0	1 µF	CAP, CERM, 1 µF, 50 V, ± 10%, X5R, 0603	0603	GRM188R61H105KAALD	Murata
FID1, FID2, FID3	0		Fiducial mark. There is nothing to buy or mount.	Fiducial	N/A	N/A

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (August 2015) to Revision A (October 2021)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document.	3
• Updated the user's guide title.	3

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