# TPSM265R1EVM
# 3-V to 65-V Input Voltage 100-mA Output Current

# User's Guide

Literature Number: SLVUBP6
August 2019

# Contents






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# List of Figures



# List of Tables




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# Evaluating the TPSM265R1EVM

## About This Manual

This guide provides information on the correct usage of the TPSM265R1EVM and explains the test points on the board. This evaluation module (EVM) is designed as an easy-to-use platform that facilitates an extensive evaluation of the features and performance of the TPSM265R1 power module.

## Glossary

*TI Glossary* —This glossary lists and explains terms, acronyms, and definitions.

## Related Documentation From Texas Instruments

For product information, visit the Texas Instruments website at http://www.ti.com.

**SNVSBF6 —**TPSM265R1, 100 mA Power Module Data Sheet

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## Board History

| PCB Revision | History |
|---|---|
| Rev E1 | Early evaluation EVM release |
| Rev A | Production EVM release |

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# Evaluation Module (EVM) Hardware

## 1 Introduction

The TPSM265R1EVM features the TPSM265R1 synchronous-buck power module configured for operation with typical 3-V to 65-V input bus applications. The output voltage is set to one of five popular values by using a configuration jumper. The EVM supplies the full output current rating of the device. Input and output capacitors are included to accommodate the entire range of input voltage and the selectable output voltages on the EVM. Monitoring test points are provided to allow measurement of the following:

- Efficiency
- Power dissipation
- Input ripple
- Output ripple
- Line and load regulation
- Transient response

Control test points, component footprints, and jumpers are provided for use of the following features of the TPSM265R1 device:

- Enable (EN)
- Undervoltage lockout (UVLO)
- Soft-start (SS)
- Power-good (PG)

The recommended PCB layout of the EVM showcases the minimal solution size, maximizes thermal performance, and minimizes output ripple and noise.

## 2 Getting Started

Figure 1 highlights the user interface items associated with the EVM. The *VIN Power* terminal block (J1) or test points TP1 and TP2 are used for connection to the host input supply. The *VOUT Power* terminal block (J2) or test points TP3 and TP4 are used for connection to the load. The terminal blocks accept up to 20-AWG wire.

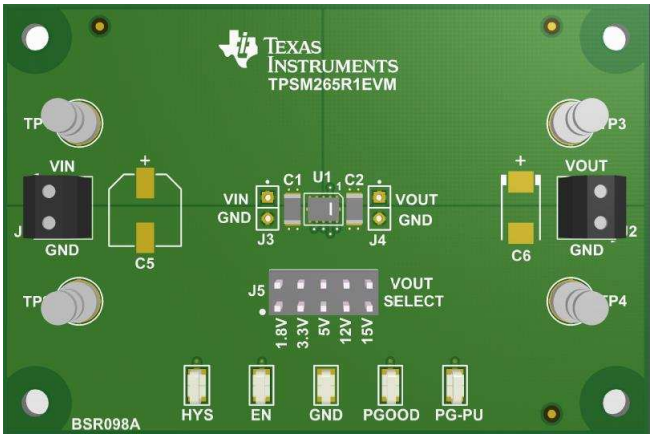


**Figure 1. TPSM265R1EVM User Interface**


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Use the VIN and VOUT MONITOR test points (TP1, TP2, TP3, and TP4), located near the power terminal blocks, as voltage monitoring points where voltmeters can be connected to measure VIN and VOUT.

Use the VIN scope (J3) and VOUT scope (J4) sockets to monitor VIN and VOUT waveforms with an oscilloscope. These test points are intended to use un-hooded scope probes outfitted with a low-inductance ground lead (ground spring) mounted to the scope probe barrel. The two sockets of each test point are on 0.1 inch centers. Connect the scope probe tip to the socket labeled VIN or VOUT, and connect the scope ground lead to the socket labeled GND.

The control test points located near the bottom of the EVM test the features of the device. Refer to the *Test Points Descriptions* section of this guide for more information on the individual control test points.

The VOUT SELECT jumper (J5) is provided to select the desired output voltage. Before applying power to the EVM, make sure that the jumper is present and properly positioned for the intended output voltage. Always remove input power before changing the jumper settings. The output voltages that can be selected using J5 are 1.8 V, 3.3 V, 5 V, 12 V, and 15 V.

The Enable (EN) and Hysteresis (HYS) features can be monitored using the test points near the bottom of the EVM. The device can be disabled by connecting the EN test point to GND. Additionally, resistors R1, R2, and R3, on the back side of the EVM can be adjusted to set an external UVLO with adjustable hysteresis.

The Power Good feature can be monitored using the PGOOD test point. The PGOOD Pullup (PG-PU) test point is provided to make it easy to apply a pullup voltage for PGOOD. A 100-kΩ resistor is connected between PG-PU and PGOOD on the EVM.

A capacitor footprint, C7, is located on the back side of the EVM for adjusting the soft-start timing of the TPSM265R1. Consult the data sheet for recommended soft-start capacitor values.

When testing the EVM, it is recommended to use a resistive load on the output. Using an electronic load can cause undesired start-up behavior or even an overcurrent condition. However, if you are using an electronic load, set the load to constant resistive mode, but continue to monitor the load behavior.

## 3 Test Point Descriptions

Wire-loop test points and scope probe sockets are included for digital voltmeters (DVM) or oscilloscope probes to aid in the evaluation of the device. Table 1 shows a description of each test point.

**Table 1. Test Point Descriptions(1)**

| | |
|---|---|
| **VIN MONITOR (TP1)** | Input voltage monitor. Connect the positive lead of a DVM to this point for measuring efficiency. |
| **VOUT MONITOR (TP3)** | Output voltage monitor. Connect the positive lead of a DVM to this point for measuring efficiency, line regulation, and load regulation. |
| **GND (TP2 and TP4)** | Ground test point. Connect the negative lead of a DVM to this point when measuring efficiency, line regulation, and load regulation. |
| **VIN Scope (J3)** | Input voltage scope monitor. Connect an oscilloscope to this set of points to measure input ripple voltage. |
| **VOUT Scope (J4)** | Output voltage scope monitor. Connect an oscilloscope to this set of points to measure output ripple voltage and transient response. |
| **HYS** | Hysteresis test point |
| **EN** | Enable test point. Connect this test point to GND to disable the device. |
| **PGOOD** | Power Good test point. Monitors the power good signal of the device. This is an open-drain signal. A 100-kΩ resistor is connected to this pin and the PG_PU pin on the EVM. |
| **PG_PU** | PGOOD pullup pin. Apply a voltage to this pin to use as a pullup voltage for the PGOOD signal. A 100-kΩ resistor is connected to this pin and the PGOOD pin. The recommended pullup voltage is ≤ 12 V. |

(1) Refer to the TPSM265R1 data sheet for absolute maximum ratings associated with above features.



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# 4 Performance Data

The following section demonstrates the TPSM265R1EVM performance.

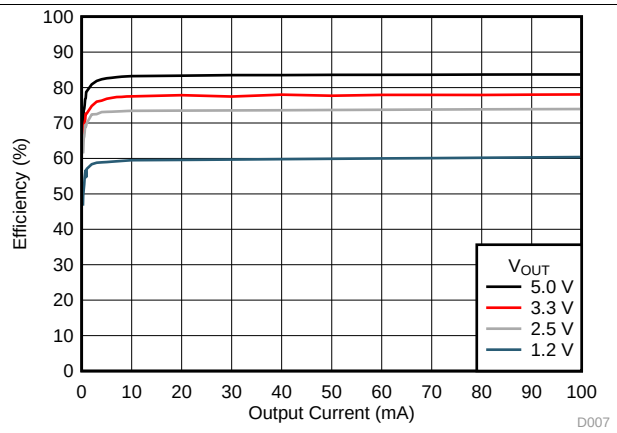



**Figure 2. Efficiency for $V_{IN}$ = 12 V**

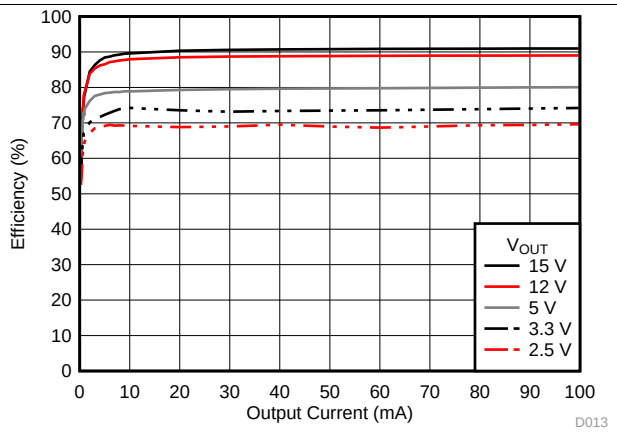



**Figure 3. Efficiency for $V_{IN}$ = 24 V**

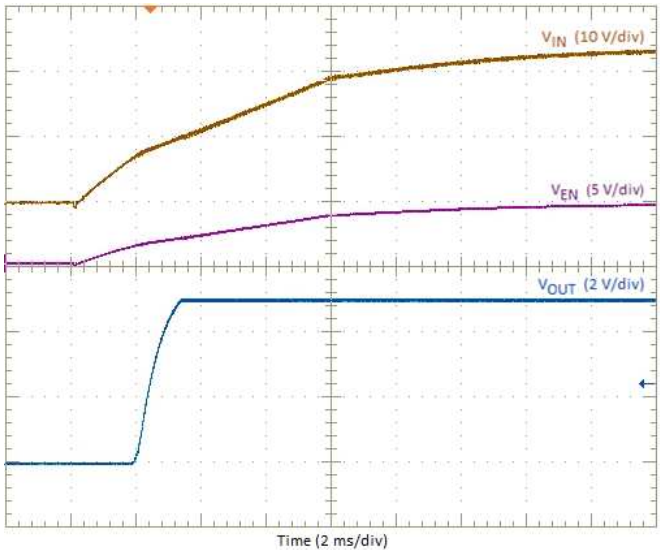
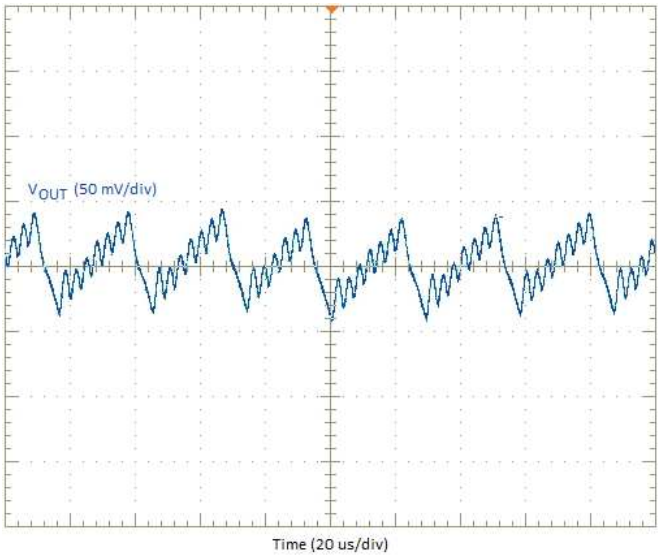



**Figure 4. Start-up Waveform**




$V_{IN}$ = 24 V $V_{OUT}$ = 5 V $I_{OUT}$ = 100 mA 20 MHz BW

**Figure 5. Output Ripple for $V_{OUT}$ = 5 V**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# 5 EVM Board Physical Specifications

This section includes the layout, schematic, and Bill of Materials (BOM) of the TPSM265R1EVM board.

## 5.1 Board Layout

The TPSM265R1EVM board dimensions are 50 mm × 75 mm. The EVM layers are provided in Figure 6 through Figure 11.

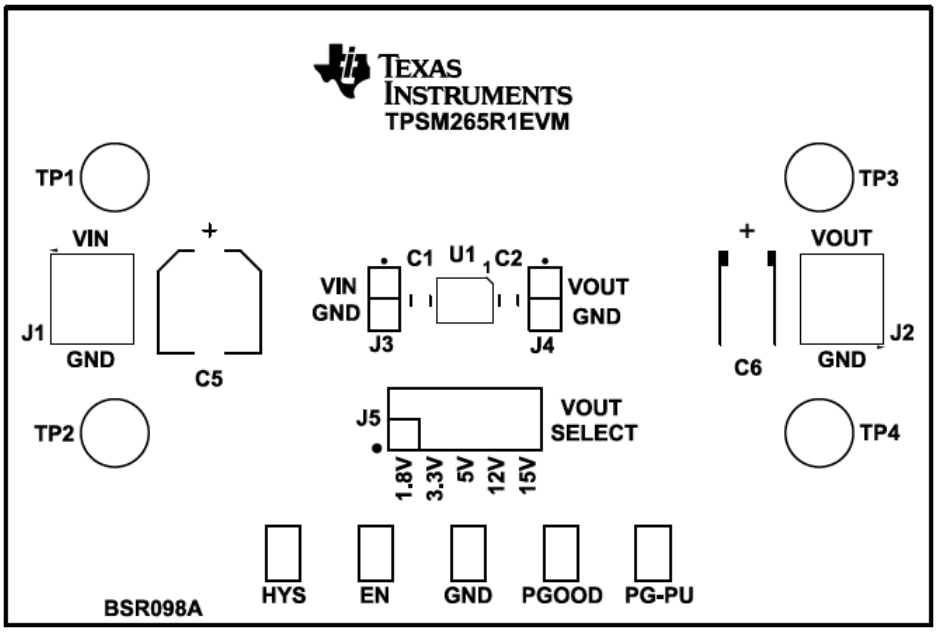


**Figure 6. Top Silk Screen**

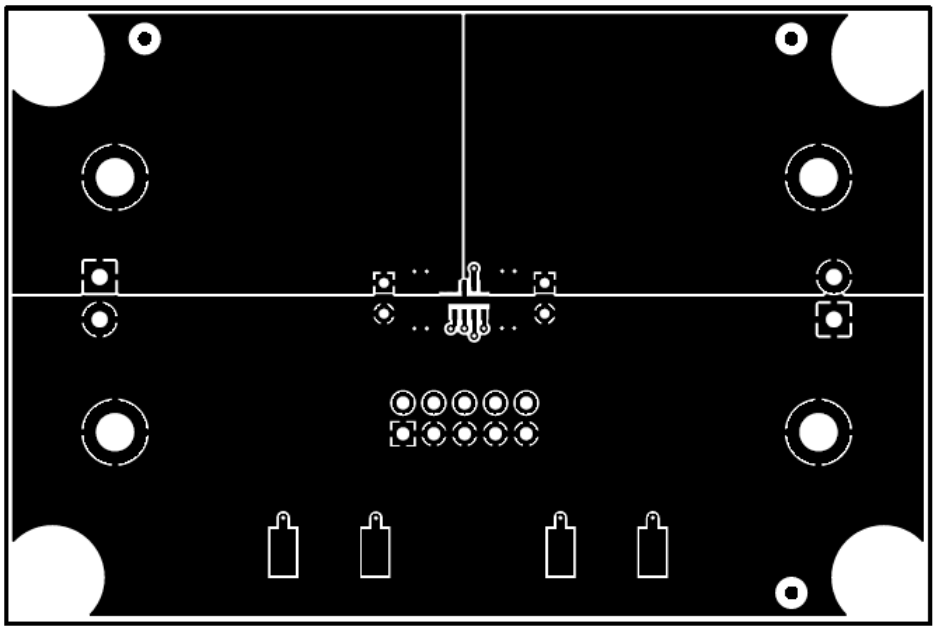

**Figure 7. Top Copper Layer**



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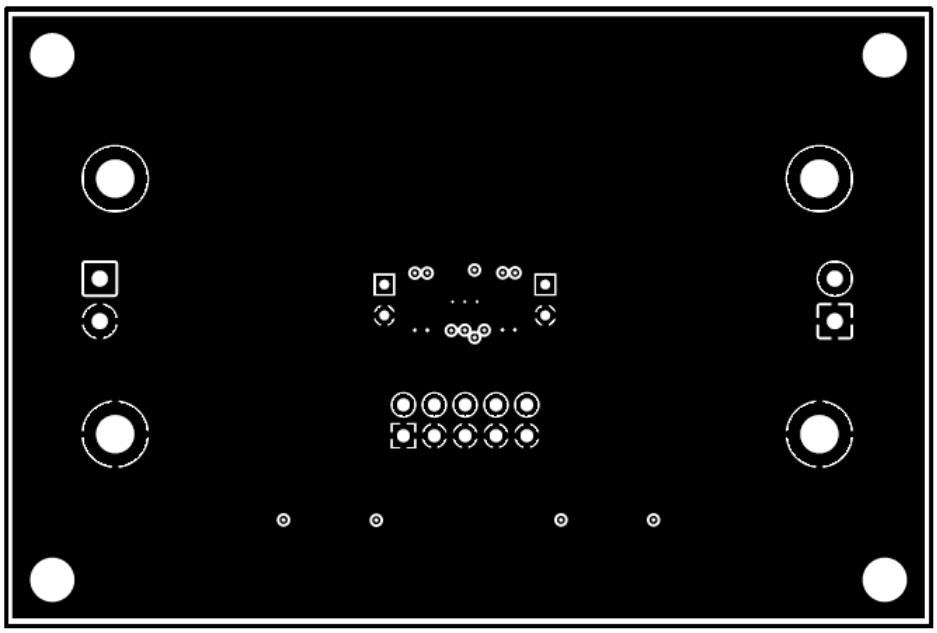

**Figure 8. Layer 2 Copper**

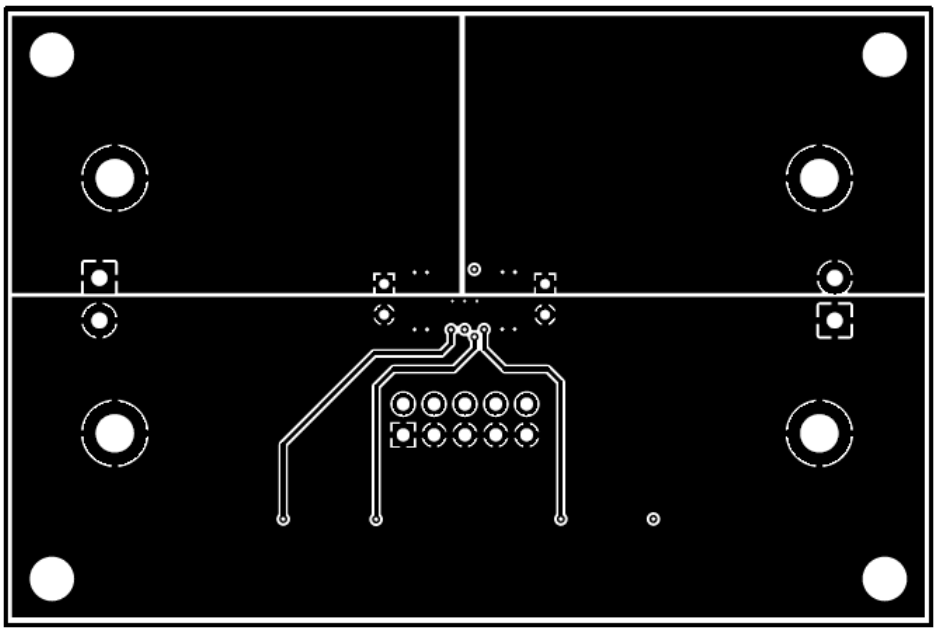

**Figure 9. Layer 3 Copper**


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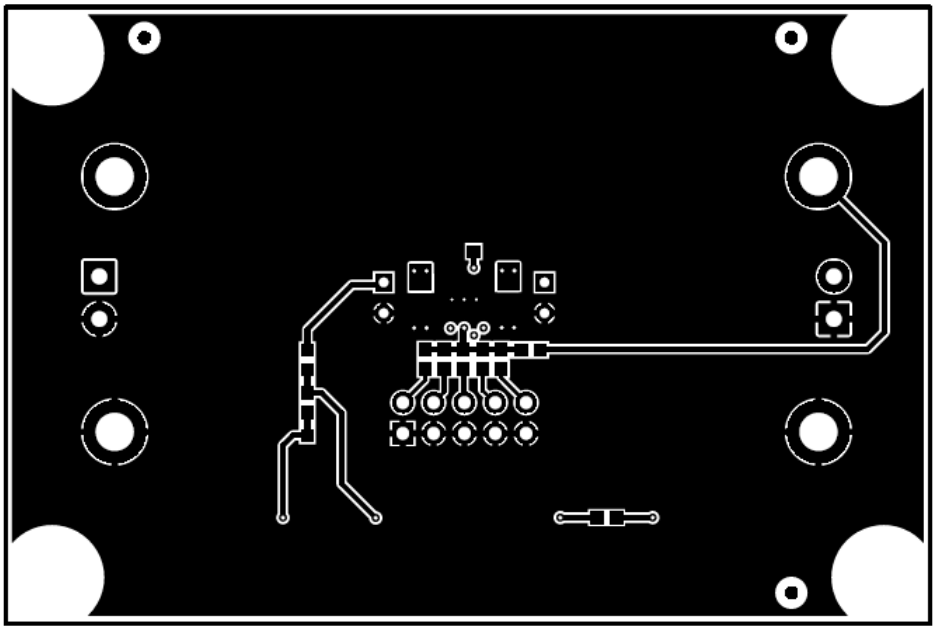

**Figure 10. Bottom Copper Layer**

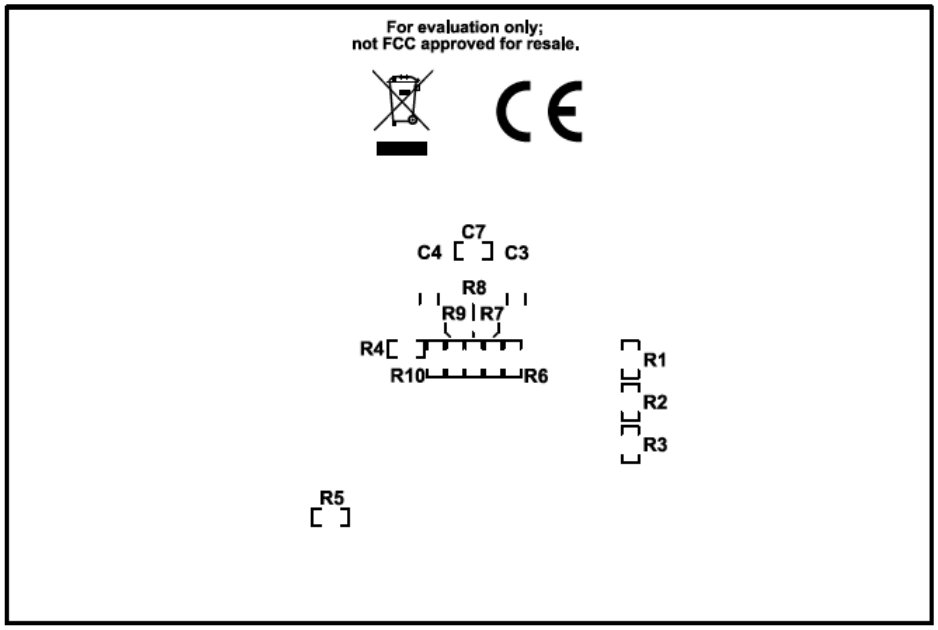


**Figure 11. Bottom Layer Silk Screen (Bottom View)**



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## 5.2 EVM Schematic

Figure 12 shows the TPSM265R1EVM schematic.

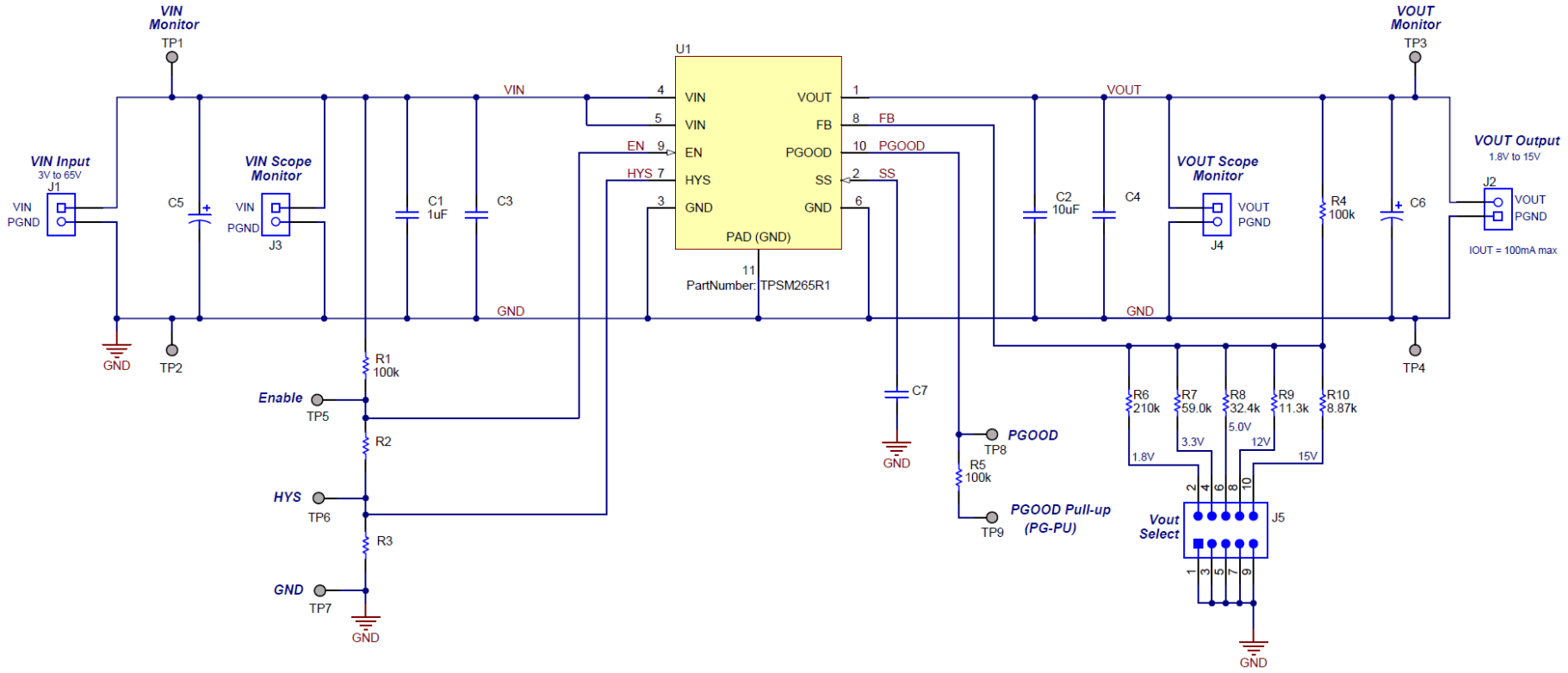


**Figure 12. TPSM265R1EVM Schematic**

## 5.3 Bill of Materials (BOM)

Table 2 shows the TPSM265R1EVM BOM.

**Table 2. TPSM265R1EVM Bill of Materials**

| DESIGNATOR | QUANTITY | VALUE | DESCRIPTION | PACKAGE REFERENCE | PART NUMBER |
|---|---|---|---|---|---|
| C1 | 1 | 1 µF | CAP, Ceramic, 1 µF, 100 V ±10%, X7R, 1206 | 1206 | C3216X7R2A105K160AA |



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**Table 2. TPSM265R1EVM Bill of Materials (continued)**

| DESIGNATOR | QUANTITY | VALUE | DESCRIPTION | PACKAGE REFERENCE | PART NUMBER |
|---|---|---|---|---|---|
| C2 | 1 | 10 µF | 'CAP, Ceramic, 10 µF, 25 V, ±10%, X7R, 1206 | 1206 | GRM31CR71E106KA12L |
| J1, J2 | 2 | | Terminal Block, 3.5 mm Pitch, 2×1, TH | 7.0 × 8.2 × 5 mm | ED555/2DS |
| J5 | 1 | | Header, 100 mil, 5×2, Tin, TH | Header, 5×2, 100 mil, Tin | PEC05DAAN |
| R1, R4, R5 | 3 | 100 k | RES, 100 k, 1%, 0.1 W, 0603 | 0603 | CRCW0603100KFKEA |
| R6 | 1 | 210 k | RES 210 k, 1%, 0.1 W, 0603 | 0603 | CRCW0603210KFKEA |
| R7 | 1 | 59.0 k | RES, 59.0 k, 1%, 0.1 W, 0603 | 0603 | CRCW060359K0FKEA |
| R8 | 1 | 32.4 k | RES 32.4 k, 1%, 0.1 W, 0603 | 0603 | CRCW060332K4FKEA |
| R9 | 1 | 11.3 k | RES, 11.3 k, 1%, 0.1 W, 0603 | 0603 | CRCW060311K3FKEA |
| R10 | 1 | 8.87 k | RES, 8.87 k, 1%, 0.1 W, 0603 | 0603 | CRCW06038K87FKEA |
| TP1, TP2, TP3, TP4 | 4 | | Terminal, Turret, TH, Double | Keystone 1503-2 | 1503-2 |
| TP5, TP6, TP7, TP8, TP9 | 5 | | Test Point, Miniature, SMT | Test Point, Miniature, SMT | 5019 |
| U1 | 1 | | 65 V Input, 100-mA Power Module | SIL0010C | TPSM265R1 |
| **Not Loaded** | | | | | |
| C3, C4 | 0 | | | 1206 | |
| C5 | 0 | | | D8 × L12mm | |
| C6 | 0 | | | 7.3 × 4.3 mm | |
| C7 | 0 | | | 0603 | |
| J3, J4 | 0 | | | Socket Strip, 100 mil | |
| R2, R3 | 0 | | | 0603 | |



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