User's Guide

TPS61094EVM-066 User's Guide

ABSTRACT

This user's guide describes the schematic, layout, bill of materials (BOM), and setup of the evaluation module (EVM) for the TPS61094EVM-066. It can supply the Vout to programed target from 2.7 V~5.4 V with Vin low to 1.8 V. The TPS61094EVM-066 supports four operating modes with different jumpers configuration, including force bypass, true shotdown, force buck, and auto buck or Boost.

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1 Introduction

1.1 Performance Specification

Table 1-1 and Table 1-2 provide a summary of the TPS61094EVM performance specifications. All specification are given for an ambient temperature of 25℃.

Table 1-1. Performance Specification Summary(Boost converter with bypass)

Parameter	Test Condition	MIN	TYP	MAX	Unit
Vin		0.7	3.3	5.5	V
Vout		2.7	3.6	5.4	V
Default Switching Frequency			1		MHz
Iout	Vin=3.3 V		500		mA

Table 1-2. Performance Specification Summary (Boost converter with Automatic Buck or Boost)

Parameter	Test Condition	MIN	TYP	MAX	Unit
Vin		0.7	5	5.5	V
Vout			3.3		V
Vsup target		1.7	2.6	5.4	V
Iout	IC Enabled, Vin=5 V, Vsup=2.6 V		250		mA

1.2 Modification

The printed-circuit board (PCB) for this EVM is designed to accommodate some modifications by the user. The external component can be changed according to the real application.

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2 Connector, Test Point and Jumper Descriptions

This section describes how to properly connect, set up, and use the TPS61094EVM-066.

2.1 Connector and Test Point Descriptions

This EVM includes I/O connectors and test points as shown in Table 2-1.

Table 2-1. Connectors and test Points

Reference Designator	Description
J1	Input voltage positive connection
J2	Input voltage positive and negative sense connection
J3	Vout positive connection
J4	Output voltage positive and negative sense connection
J5, J6, J9, J10	GND connection
J7	SUP port positive connection
J8	Sup port positive and negative sense connection

2.2 Jumper Configuration

The TPS61094EVM-066 can support different operating modes by the varied jumper combinations. And in this paper, it will show two typical application circuits.

One typical application circuit is the pure boost with bypass function, as shown in Figure 2-1, which connects the SUP pin and VIN pin together. The jumper configuration for this application is shown in Table 2-2.

The other typical application circuit is the supercap backup application, which separates the SUP pin and VIN pin, as shown in Figure 2-2, which can charge supercap or boost supercap to power the output. The jumper configuration for this application is shown in Table 2-3

2.2.1 Boost Converter with Bypass

In this section, it shows how to set the EVM to support *Boost converter with bypass* application. The sketch schematic is shown in Figure 2-1, while the jumper configuration is shown in Table 2-2

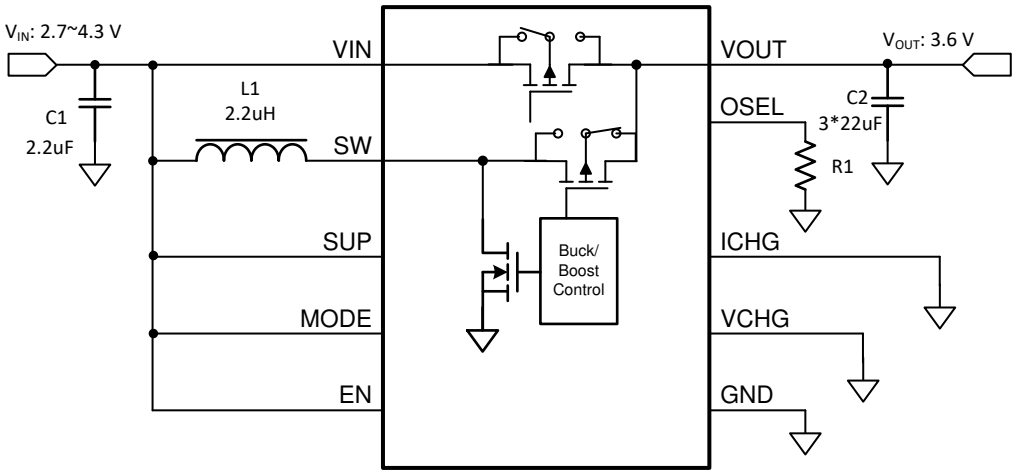

Figure 2-1. Boost Converter with Bypass

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Table 2-2. Jumpers Configuration for Boost Converter with Bypass

Reference Designator	Description	Configuration
JP1 ， JP2	Short 1-2 :connect the SUP pin to the Vin port Short 2-3: connect the SUP pin to the SUP port	Short 1-2
JP3	Sup termination voltage selection	-
JP4	Changing current selection	-
JP5	Output voltage target selection	At mark 3.6 V
J11, J12	Operating mode selection pin. The MODE pin and EN pin work together to set device operation mode.	Set High to select auto Buck or boost mode

2.2.2 Boost Converter with Automatic Buck or Boost Function

In this section, it shows the how to set the EVM support *Boost converter with automatic buck or boost* application. The sketch schematic is shown in Figure 2-2, while the jumper configuration is shown in Table 2-3

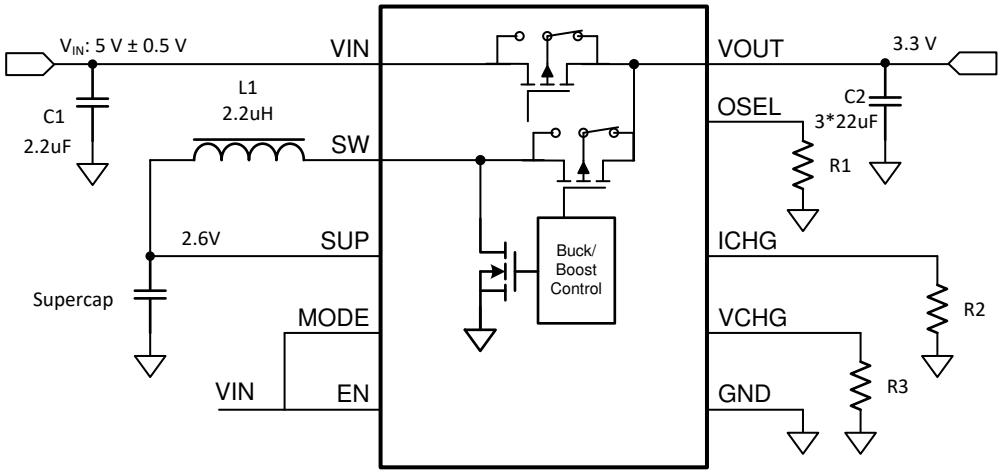

Figure 2-2. Boost Converter with Automatic Buck or Boost

Table 2-3. Jumpers Configuration for Boost Converter with Automatic Buck or Boost

Reference Designator	Description	Configuration
JP1 ， JP2	Short 1-2: connect the SUP pin to the Vin port Short 2-3: connect the SUP pin to the SUP port	Short 2-3
JP3	Sup termination voltage selection	At the mark 2.6 V
JP4	Changing current selection	At the mark *250 mA*
JP5	Output voltage target selection	At mark *3.6 V*
J11, J12	Operating mode selection pin. The MODE pin and EN pin work together to set device operation mode.	Set High to select auto Buck or boost mode

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3 Schematic, Bill of Materials, and Board Layout

This section provides the TPS61094EVM-066 schematic, bill of materials (BOM), and board layout.

3.1 Schematics

Figure 3-1 shows the TPS61094EVM-066 schematic.

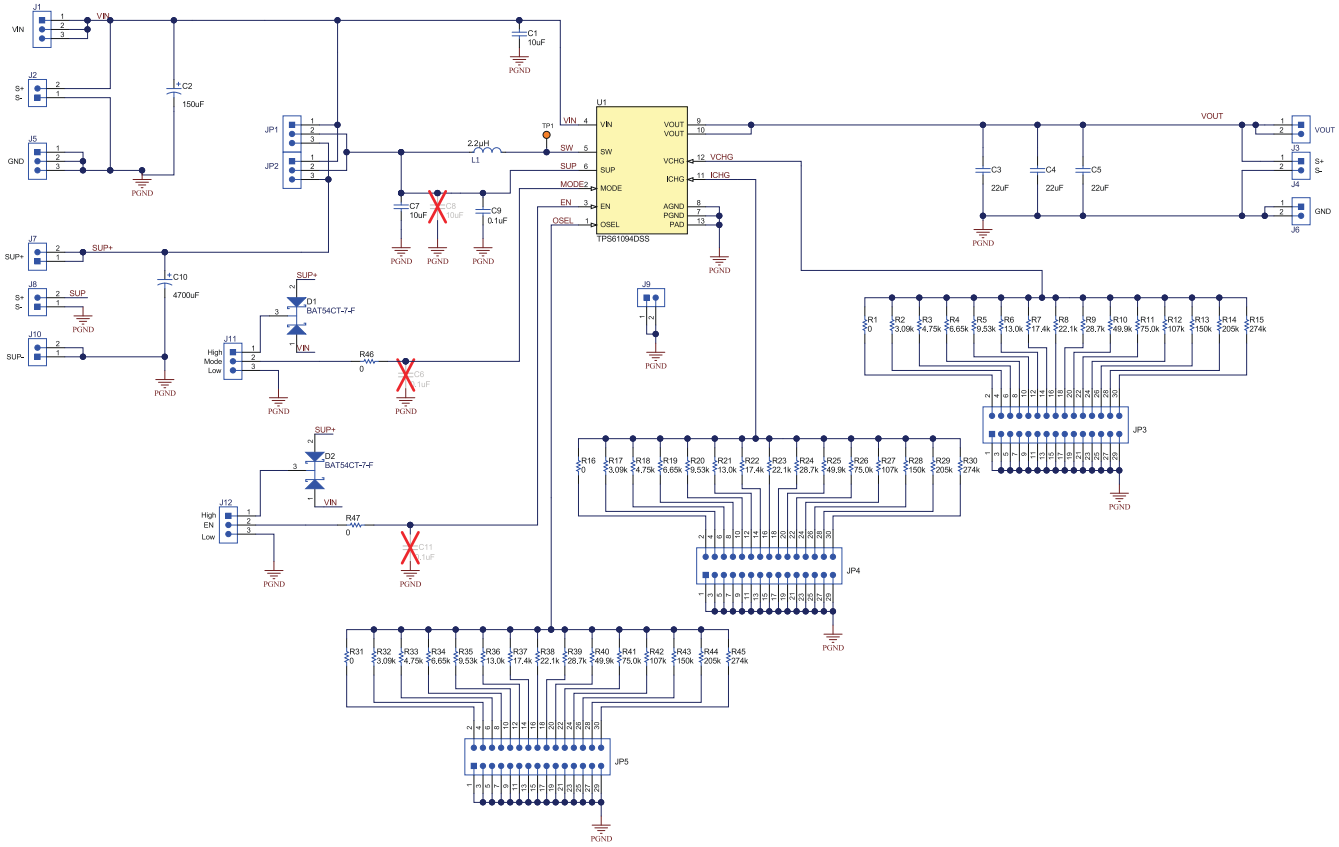

Figure 3-1. TPS61094EVM-066 Schematic

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3.2 Bill of Materials

Table 3-1 lists the BOM of the TPS61094EVM-066.

Table 3-1. Bill of Materials

Designator	Qty	Value	Description	Package Reference	PartNumber	Manufacturer
C1, C7	2	10uF	CAP, CERM, 10 uF, 10 V, +/- 20%, X5R, 0603	0603	GRM188R61A106ME69D	MuRata
C2	1	150uF	CAP, TA, 150 uF, 10 V, +/- 10%, 0.1 ohm, SMD	7343-31	T495D157K010ATE100	Kemet
C3, C4, C5	3	22uF	CAP, CERM, 22 uF, 10 V, +/- 20%, X5R, 0805	0805	GRM21BR61A226ME44L	MuRata
C9	1	0.1uF	CAP, CERM, 0.1 uF, 50 V, +/- 10%, X7R, AEC-Q200 Grade 1, 0402	0402	CGA2B3X7R1H104K050BB	TDK
C10	1	4700uF	CAP, AL, 4700 uF, 6.3 V, +/- 20%, 0.015 ohm, TH	12.5x25mm	EEUFR0J472	Panasonic
D1, D2	2	30 V	Diode, Schottky, 30 V, 0.2 A, SOT-523	SOT-523	BAT54CT-7-F	Diodes Inc.
J1, J5, J11, J12	4		Header, 100mil, 3x1, Tin, TH	Header, 3 PIN, 100mil, Tin	PEC03SAAN	Sullins Connector Solutions
J2, J3, J4, J6, J7, J8, J9, J10	8		Header, 100mil, 2x1, Gold, TH	Header, 100mil, 2x1, TH	HTSW-102-07-G-S	Samtec
JP1, JP2	2		Header, 100mil, 3x1, Gold, TH	Header, 100mil, 3x1, TH	HTSW-103-07-G-S	Samtec
JP3, JP4, JP5	3		Conn Unshrouded Header HDR 30 POS 2.54mm Solder ST Thru-Hole	HDR30	HMTSW-115-07-G-D-240	Samtec
L1	1		Shielded Power Inductors	SMT_4MM0_4MM0	XGL4020-222MEC	Coilcraft
R1, R16, R31, R46, R47	5	0	RES, 0, 5%, 0.063 W, 0402	0402	RC0402JR-070RL	Yageo America
R2, R17, R32	3	3.09k	RES, 3.09 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW04023K09FKED	Vishay-Dale
R3, R18, R33	3	4.75k	RES, 4.75 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW04024K75FKED	Vishay-Dale
R4, R19, R34	3	6.65k	RES, 6.65 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW04026K65FKED	Vishay-Dale
R5, R20, R35	3	9.53k	RES, 9.53 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW04029K53FKED	Vishay-Dale
R6, R21, R36	3	13.0k	RES, 13.0 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW040213K0FKED	Vishay-Dale
R7, R22, R37	3	17.4k	RES, 17.4 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW040217K4FKED	Vishay-Dale
R8, R23, R38	3	22.1k	RES, 22.1 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW040222K1FKED	Vishay-Dale
R9, R24, R39	3	28.7k	RES, 28.7 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW040228K7FKED	Vishay-Dale
R10, R25, R40	3	49.9k	RES, 49.9 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW040249K9FKED	Vishay-Dale
R11, R26, R41	3	75.0k	RES, 75.0 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW040275K0FKED	Vishay-Dale
R12, R27, R42	3	107k	RES, 107 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW0402107KFKED	Vishay-Dale
R13, R28, R43	3	150k	RES, 150 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW0402150KFKED	Vishay-Dale
R14, R29, R44	3	205k	RES, 205 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW0402205KFKED	Vishay-Dale

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Table 3-1. Bill of Materials (continued)

Designator	Qty	Value	Description	Package Reference	PartNumber	Manufacturer
R15, R30, R45	3	274k	RES, 274 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW0402274KFKED	Vishay-Dale
TP1	1		Test Point, Miniature, Orange, TH	Orange Miniature Testpoint	5003	Keystone
U1	1		100-nA QUIESCENT CURRENT BI-DIRECTIONAL BUCK/ BOOST CONVERTER WITH BYPASS MODE, DSS0012B (WSON-12)	DSS0012B	TPS61094DSS	Texas Instruments
C6, C11	0	0.1uF	CAP, CERM, 0.1 uF, 50 V, +/- 10%, X7R, AEC-Q200 Grade 1, 0402	0402	CGA2B3X7R1H104K050BB	TDK
C8	0	10uF	CAP, CERM, 10 uF, 10 V, +/- 20%, X5R, 0603	0603	GRM188R61A106ME69D	MuRata

3.3 PCB Layouts

The TPS61094EVM board is a 4-layer PCB. The top and bottom layers copper thickness is 2-oz. The two inner layers copper thickness is 1-oz.Figure 3-2 and Figure 3-5 show the top view and bottom view, respectively. Figure 3-3 and Figure 3-4 show the inner layer 1 and inner layer 2, respectively.

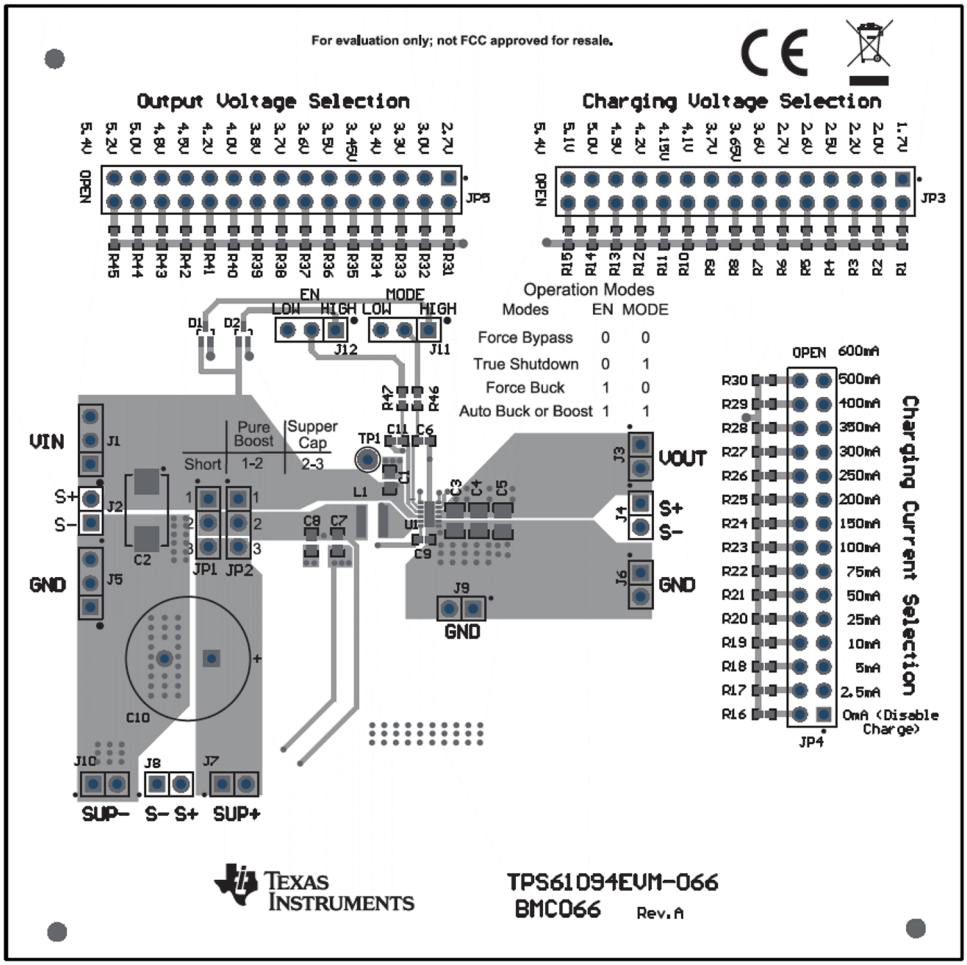

Figure 3-2. TPS61094EVM-066 Top-Side Layout

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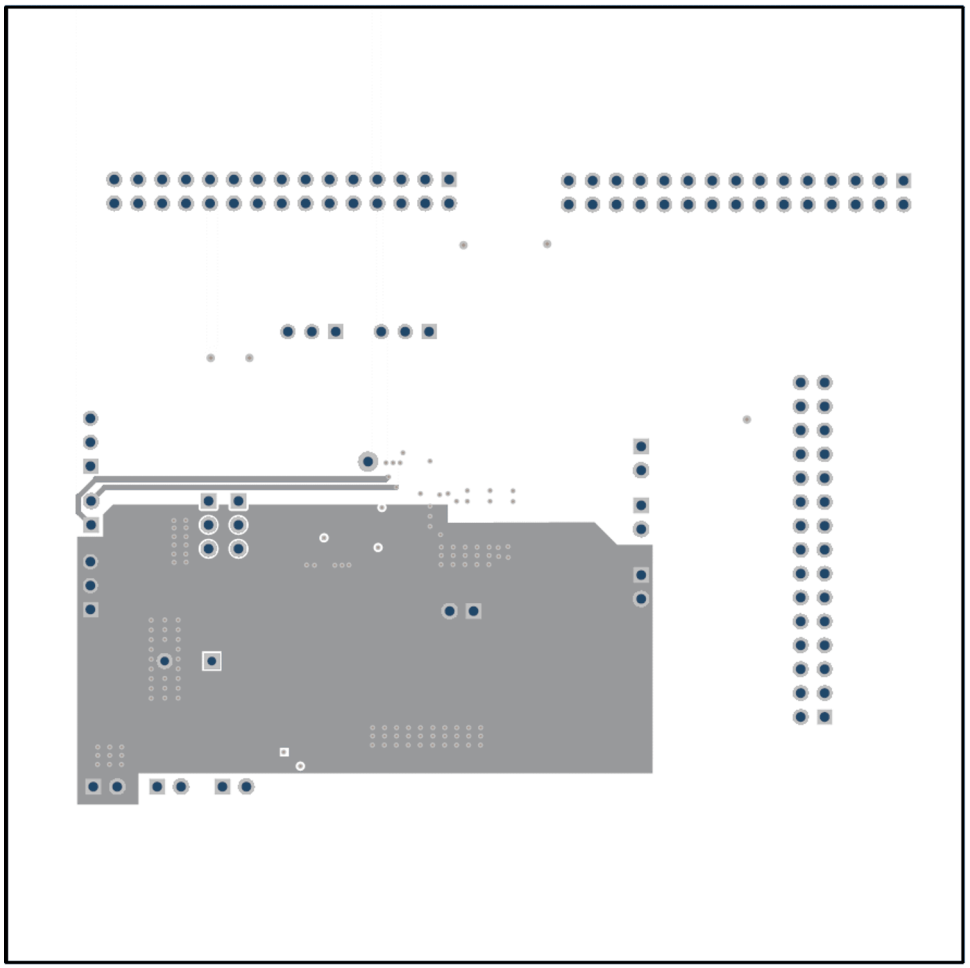

Figure 3-3. TPS61094EVM-066 Inner Layer1 Layout

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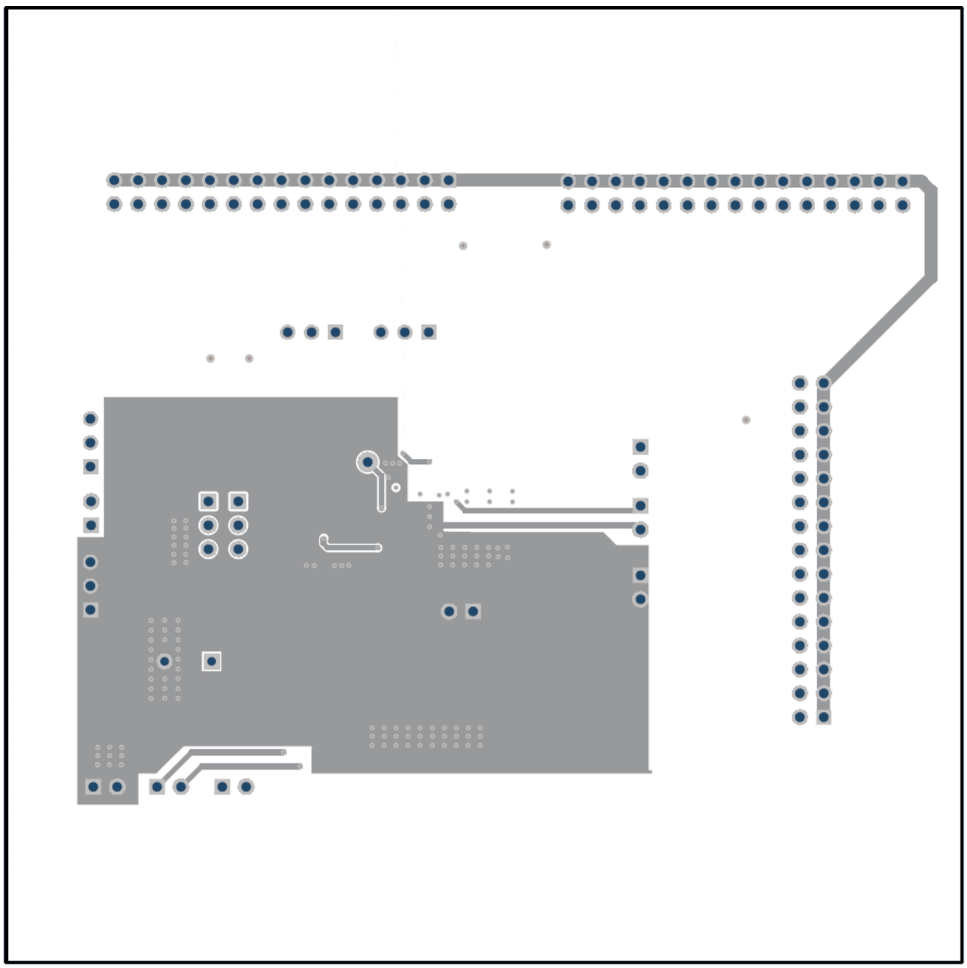

Figure 3-4. TPS61094EVM-066 Inner Layer2 Layout

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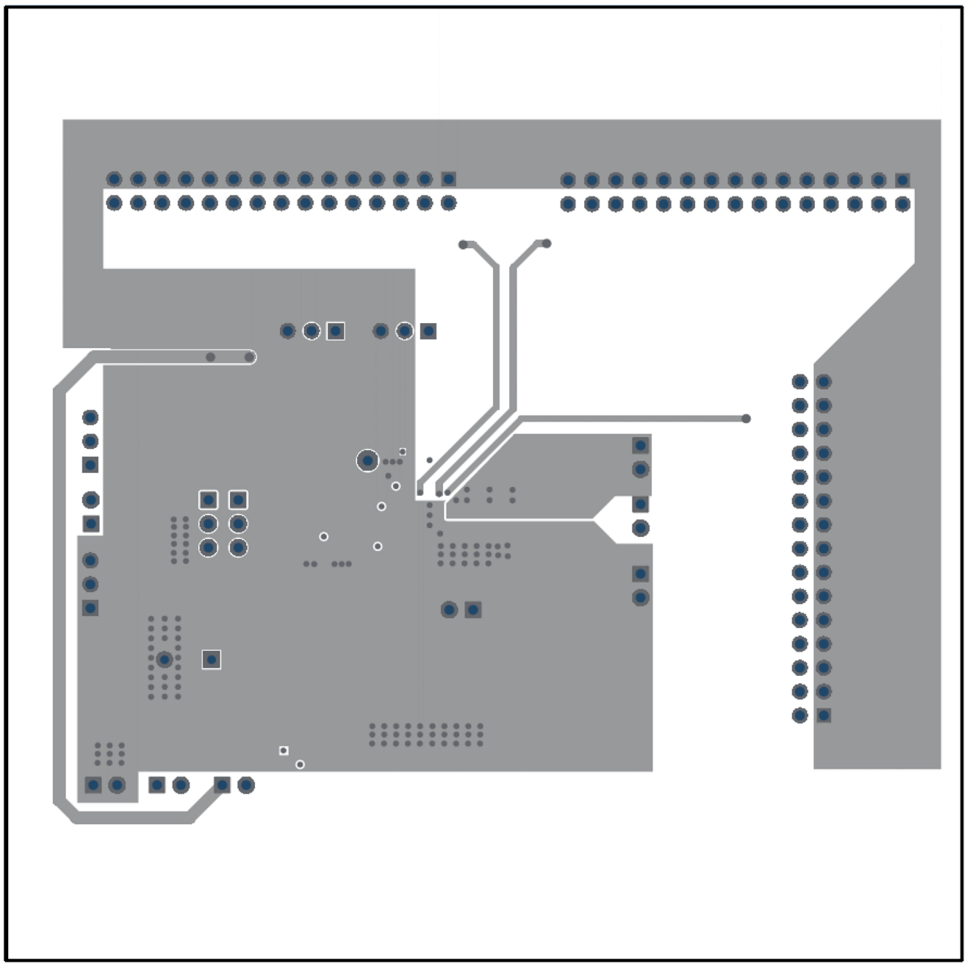

Figure 3-5. TPS61094EVM-066 Bottom Side Layout

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