EVM User's Guide: ADC34RF72

ADC3xRF72 Evaluation Module

Description

The ADC3xRF72EVM is an evaluation module (EVM) designed to evaluate the ADC34RF7x family of highspeed ADCs. The ADC3xRF72EVM is populated with an ADC3xRF72. The ADC3xRF72 is a 16-bit ADC, quad channel ADC with an JESD interface, and can operate at samples rates up to 1.5 GSPS. The ADC3xRF72EVM allows for evaluation of all device speed grades, and number of channels.

Get Started

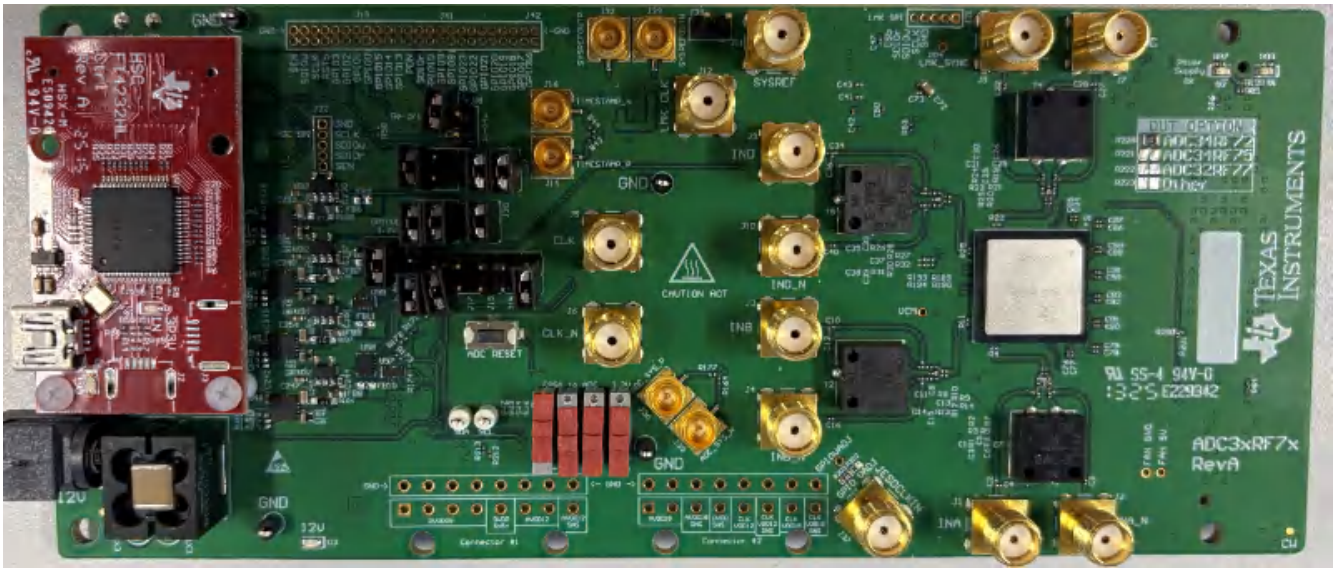
1. Order the EVM from ti.com (ADC3xRF72EVM).
2. Download the latest revision of the data sheet (SBASAL0).
3. Download the latest software.
4. Download the comprehensive reference design files from the tools page of the EVM (ADC3xRF72).

Features

- Noise spectral density: -164.2 dBFS/Hz
- Full power input bandwidth (-3dB): 1.8GHz
- Power consumption: 0.95 W/channel (1.5GSPS)
- Eight digital down-converters, can be configured in single band, dual band and octal band configurations. Supporting real and complex decimation with factors starting at /2,/3,/5 up to 32768.
- 48-bit NCO phase coherent frequency hopping
- Serial JESD interface supporting lane rate up to 24.75Gbps
- Multiple integrated DSP features such as 96-tap/ch PFIR equalizer an fractional delay filter

Applications

- Phase array radar
- Wafer inspection
- Spectrum analyzers
- Software defined radio (SDR)
- Electronic warfare
- High-speed digitizer
- Cable infrastructure
- Communications infrastructure



ADC3xRF72EVM

1 Evaluation Module Overview

1.1 Introduction

The ADC3xRF72EVM allows for evaluation of the ADC3xRF72 high speed ADC. The EVM is configured to receive external single-ended analog inputs as the EVM utilizes on board baluns for single-ended to differential conversion. The ADC sampling clock is sourced externally and is single-ended, the EVM also utilizes an on board balun for single-ended to differntial conversion for the ADC's sample clock. For data capture, the ADC3xRF72EVM is paired with the TSW14J58EVM. The TSW14J58EVM is an FPGA based data capture card which features a AMD Kintex Ultra Scale FPGA. The ADC data, captured by the FPGA, is then transferred to the PC and displayed in the High Speed Data Converter Pro capture software. This user's guide describes the characteristics, operation, and use of the ADC3xRF72 evaluation module (EVM).

1.2 Kit Contents

Item	Description	Quantity
ADC3xRF72EVM	PCB	1
Mini - USB Type X Cable	Cable	1
JTAG-HS2 Programming Dongle	Dongle and cable assembly	1
Power Cable for 12V Jack	Cable	1

1.3 Specification

The specifications for the ADC3xRF72 can be found in the device-specific data sheet *ADC3xRF72 Quad Channel 16-bit 1.5 GSPS RF Sampling Data Converter Data Sheet* (SBASAL0).

1.4 Device Information

The ADC3xRF72 EVM is configured to receive external single-ended analog inputs as the EVM includes baluns for single-ended to differential conversion. The ADC sampling clock is also sourced externally and is single-ended. For more details, the device information for the ADC3xRF72 can be found in the device-specific data sheet *ADC3xRF72 Quad Channel 16-bit 1.5 GSPS RF Sampling Data Converter Data Sheet* (SBASAL0).

2 Hardware and Software Setup

This section describes the necessary hardware for evaluating the full performance of the ADC3xRF72 EVM.

2.1 Board Overview

Figure 2-1 highlights some key features of the board required for evaluation.

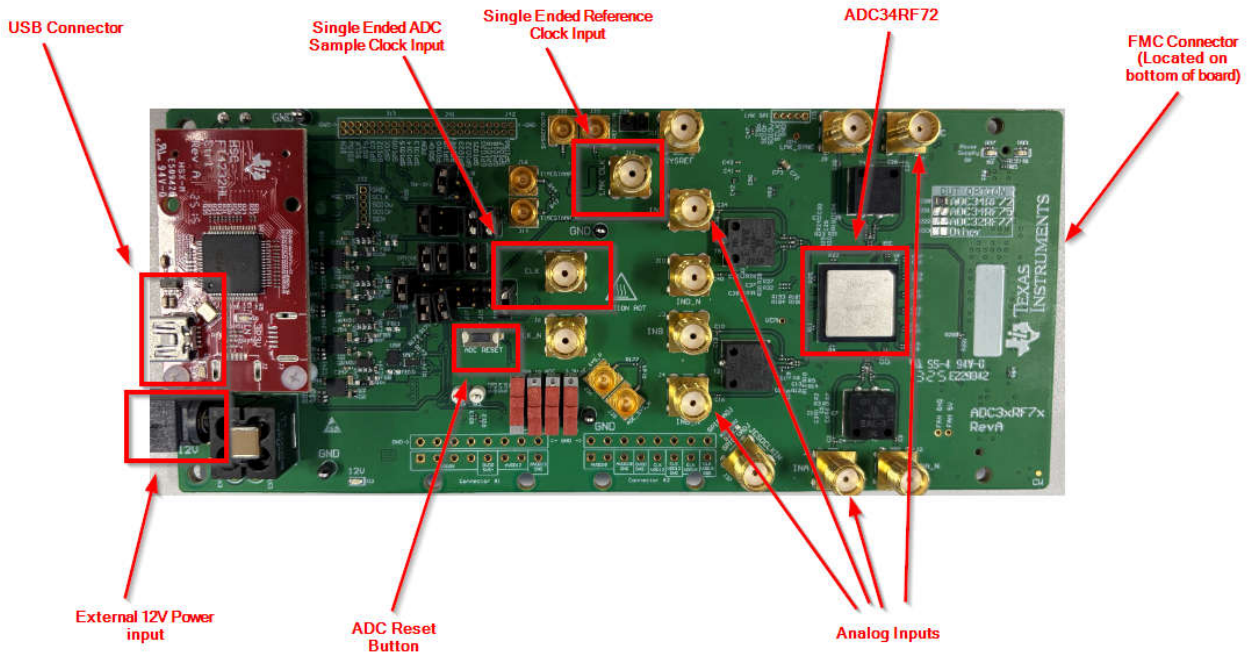


Figure 2-1. ADC3xRF72EVM Features

2.2 Required Equipment

In addition to the provided equipment detailed in section Section 1.2, the following equipment is not included with the EVM kit, but is required for proper evaluation.

- TSW14J58EVM FPGA Capture card for capturing data from the ADC, and everything required for operation according to the TSW14J58EVM User's Guide TSW14J58EVM.
- High-Speed Data Converter Pro Software (HSDC Pro) High Speed Data Converter Pro
- GSPS FPGA SERVER GSPS FPGA SERVER download link
- One 12 Volt power supply capable of supplying 5Amps
- At least two low-noise signal generators to provide the ADC sampling clock and analog inputs to the ADC. TI recommends either of the following signal generators:
  - Rohde and Schwarz SMA100A
  - Rohde and Schwarz SMA100B
- A lower performance signal generator is also required as a reference clock to the ADC:
  - This clock does not affect ADC performance and is only be used for functionality.
- Bandpass filters for the sample clock and analog inputs. It is recommended to use filters with a narrow passband (within 5%-15% of the desired bandwidth), and minimal insertion loss.
- SMA cables to connect the inputs

By default, the EVM is configured for an external reference clock to be provided, there are optional board modifications that can be done to allow for only a single clock be supplied to the ADC EVM. These modifications are noted in Section 5.2

2.3 Required Software Installation

In this section, all of the necessary software installations for the ADC3xRF72 EVM are detailed. To operate the ADC correctly the following software must be installed.

2.4 Required TI Software to Install

- ADC3xRF72 EVM GUI

  This is used for programming the ADC and clocking chips properly into the desired mode of operation for evaluation of the ADC. This can be found on the Ti.com product page for the EVM ADC3xRF7xEVM GUI download
- High Speed Data Converter Pro (HSDC Pro)

  This is used for live plotting and analysis of signals captured by the ADC to allow for simple and quick evaluation of the ADC. Minimum required version is 5.2, if user already has a version installed that meets the requirement this step can be skipped. High Speed Data Conveter Pro Download
- GSPS FPGA SERVER

  This is used for connecting and controlling the TSW14J58EVM capture card with the ADC EVM GUI Software. It is used to program the Capture card into the required mode of operation as well as handle all data collection from the high speed ADC. GSPS FPGA SERVER download link

2.5 3rd Party Software to Install

In addition to software provided by TI there are some additional software packages required to evaluate the ADC.

- Vivado 2019.1 64-bit Hardware Server for Windows:
  - This is required for communication with the FPGA to allow for configuration of FPGA capture software.
  - Can be installed from AMD Xilinx website. The SW is license free but an AMD Xilinx Account is required for install.
  - Version 2019.1 is recommend since it is the smallest install size that satisfies the requirements.
  - If the users PC already has a version of Vivado, Vivado Lab tools or equivalent then this step can be skipped.
  - It is necessary to also add Xilinx hardware server to your system path which can be done by following the steps in section Section 2.6.
- FT_Prog FTDI Software:
  - This is an optional piece of software but is useful for checking USB handle name is correct and serial number is valid
  - Can be installed from the FTDI website

2.6 Software Environment Setup

Vivado Lab bin must be added to your PATH system environment variable. Depending on where you installed Vivado Lab and what version you installed, the path to the bin folder typically looks something like this: C:\Xilinx\Vivado_Lab\2023.1.1\bin

Figure 2-2 is showing the process to add vivado lab tools to your environment variables path.

To verify that this is successfully done, type the command "xsdb" into a command prompt and a message indicating that the "Xilinx System Debugger" has been launched.

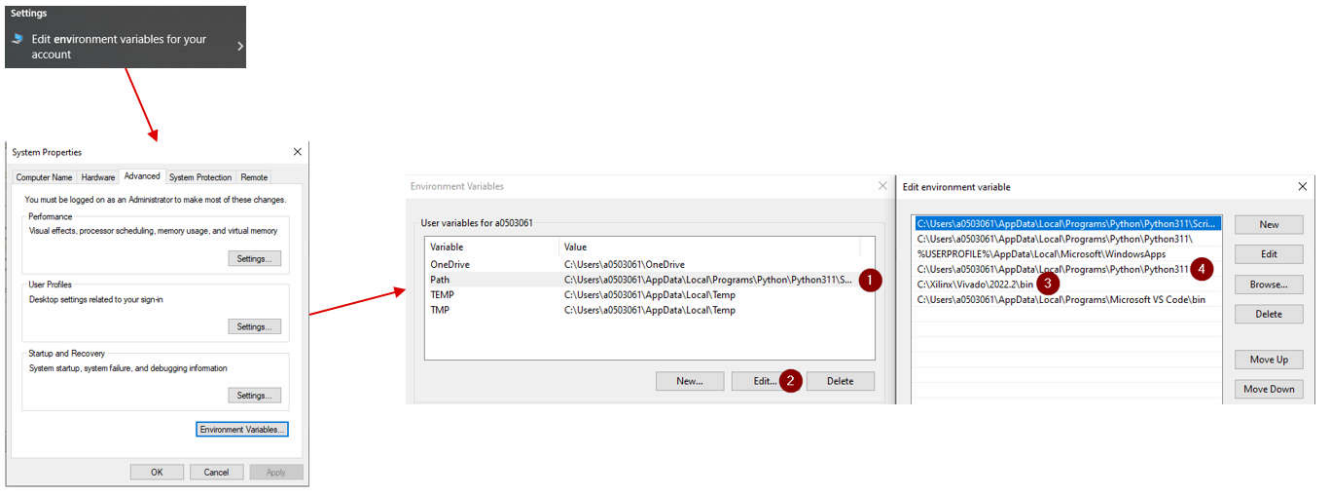


Figure 2-2. Environment Path Example

2.7 Hardware Setup and Connections

This section describes all necessary hardware and connections.

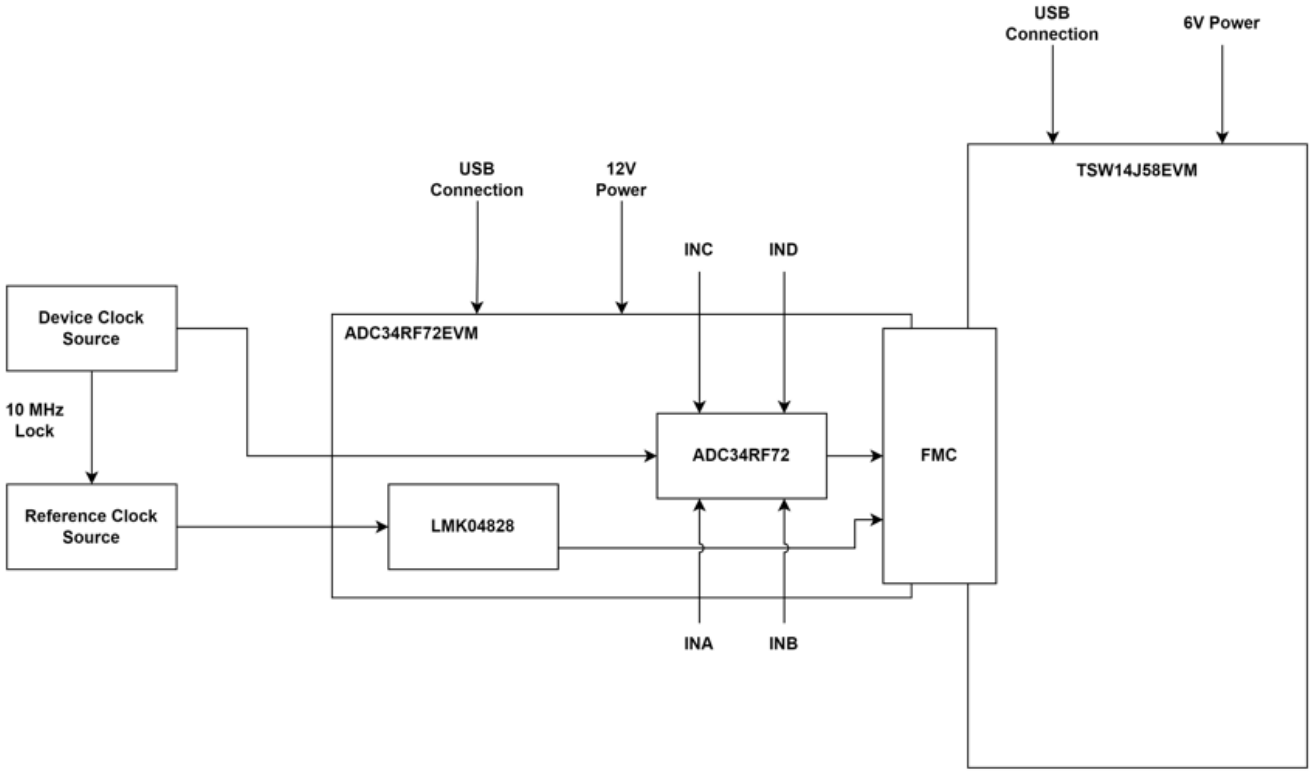


Figure 2-3. Hardware Connection Block Diagram

2.8 ADC3xRF72 EVM Connections

This section describes all of the necessary connections on the ADC3xRF72 EVM in order. At this time, all power supplies and signal generators must be powered off.

1. Connect USB mini connector to FTDI Daughter Card.
   a. On connection LED D1 on daughter card lights up green, if not the daughter card can be broken and needs to be inspected.
2. Connect low-noise signal generator to SMA connector J5 (labeled CLK on EVM), this serves as the high-speed sampling clock to the ADC.
   a. Set Signal generator to desired sampling rate of ADC and output power to 9dBm.
   b. On connection, the signal generator must be in the off state.
3. Connect low-noise signal generator to SMA connector J12 (labeled LMK CLK on EVM), this serves as the reference clock source to the ADC EVM.
   a. Set Signal generator to match the sampling rate of the device and the output power to 9dBm.
   b. On connection the signal generator must be in the off state.
4. Connect low-noise signal generator to SMA connector J1 (labeled INA on EVM), this serves as the analog input signal to channel A of the ADC.
5. Connect 12V 5A to barrel connector J31.
6. Power on all signal generators to EVM.
7. Verify that all signal generators are also phase locked to each other.

For best performance TI recommends the use of Bandpass filter for the ADC clock input signals and ADC Analog input signals, this is to help limit the addition of external noise to the ADC.

There are a number of jumper and switches on the EVM for advanced control and extended features. For more information, Section 2.11. For default operation of the EVM, the switches and jumpers they must be in the following configuration:

- J19 installed: to power DVDDMEM09 ADC power rail from on board DVDD09 rail
- J20 installed on second option: Installed to set GPIOVDD level to 1.8V
- J24 installed: Installed to set ADC and LMK SPI control to come from USB via FTDI chip
- J25 uninstalled: Sets GPIO0, GPIO1 and PDN_ADC to come from FPGA via FMC connector
- J26 installed: Set range of GPIO to come from USB
- J27 installed: Set range of GPIO to come from USB
- J30 installed: Controls Level Shifting direction
- J34 installed: Selects FPGA Transceiver reference clock to be supplied by the on board LMK04828 device
- J38 uninstalled: Selects the source of the ADC's SYSREF signal to come from LMK04828 device
- J40 installed: Selects the JESDCLKIN input of the ADC to come from the onboard LMK04828 device
- J45 installed: Selects the HW reset signal for the ADC to be triggered via the USB
- SW2 UP
- SW3,4,6 DOWN

2.9 TSW14J58 Data Capture Card Connections

This section describes all the hardware connections for the TSW14J58 capture card.

1. Connect power supply at 6V 4A to barrel connector J2 (labeled PWRIN on capture card).
2. Verify that the power switch is in the “ON” position.
3. Connect JTAG debug dongle to pin header labeled JTAG.
4. Connect ADC EVM to FMC connector.

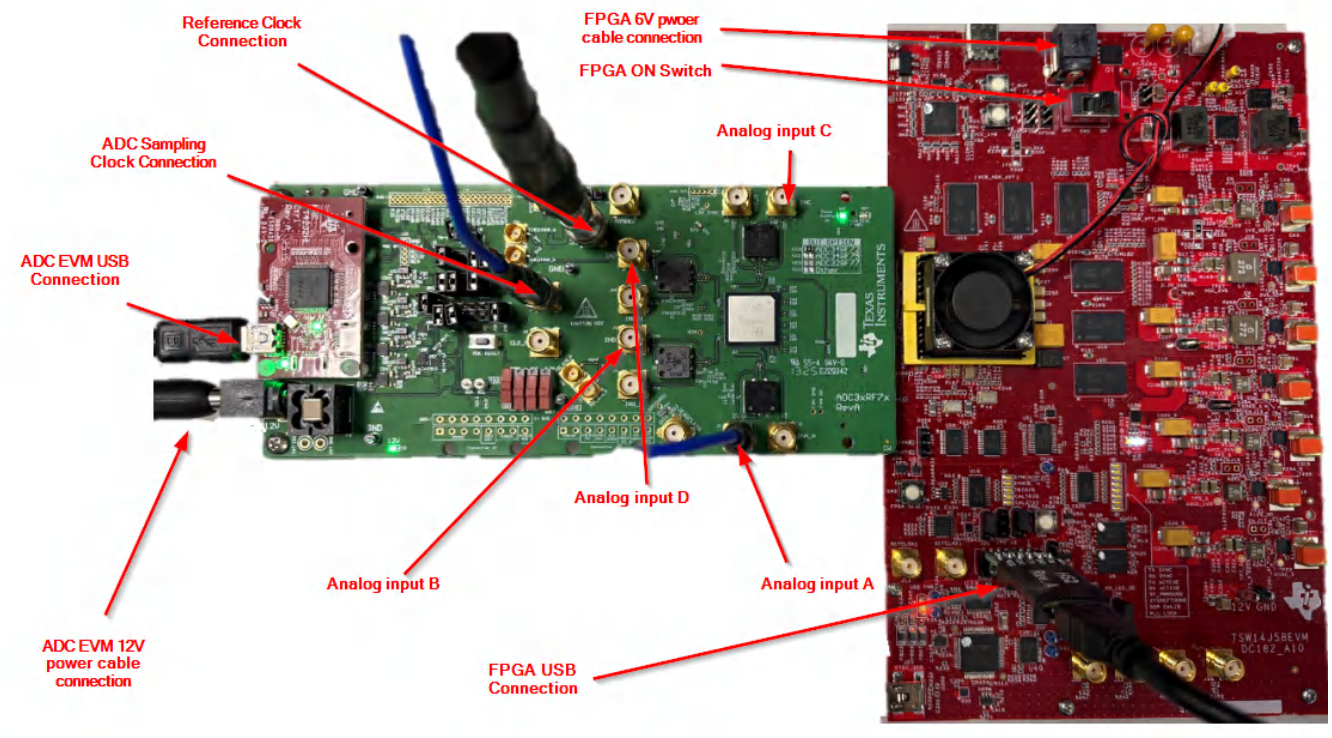


Figure 2-4. Example HW Setup

2.10 Debug LEDs

This section details all the debug LEDs on the EVM to verify that the hardware is functioning properly.

LED Number	Description
D2	All power rails on EVM good
D3	12V power on EVM

2.11 EVM Jumpers and Switches

Table 2-1 details all the jumpers and switches on the EVM and their functions.

Table 2-1. Jumpers and Switches and Their Functions

Jumper Name	Function
J19	DVDDMEM09 Source. Installed inherit from DVDD09 rail, uninstall externally powered.
J20	Swizzle between GPIOVDD level, 1.8V or 1.2V
J24	Controls Switching ADC and LMK comms from USB or FPGA. Installed USB SPI, uninstalled FPGA SPI
J25	Controls switching signals GPIO0, GPIO1 and PDN_ADC to come from USB or from FMC. Installed USB, Uninstalled FMC
J26+J27	Work together to select which GPIOs go to ADC. See truth table in schematic.
J30	USB GPIO Direction, controls level shifter for USB -> ADC Level shifting. Affects signals RSTb_ADC_FT, PDN_ADC_FT, GPIO_MUX0_FT, GPIO_MUX1_FT. Installed ADC to USB, Uninstalled USB to ADC.

Table 2-1. Jumpers and Switches and Their Functions (continued)

Jumper Name	Function
J34	MGTREFCLK0 Sel MUX, Mux to select where FPGA JESD xcvr ref clock comes from, installed lmk, uninstalled ADC
J38	ADC SYSREF Input Mux, installed sysref comes from external smp connectors, uninstalled sysref comes from on board lmk04828
J40	JESDCLKIN Mux, installed JESDCLKIN comes from LMK, uninstalled comes from external sma connector
J45	ADC HW Reset Input Mux, installed HW reset from USB, uninstalled HW reset from FMC
SW2	Controls level shift direction for GPIO0, GPIO1, GPIO14 and GPIO15 of the ADC
SW3	Controls level shift direction for GPIO20, GPIO21, GPIO22 and GPIO23 of the ADC
SW4	Controls level shift direction for GPIO16, GPIO17, GPIO18 and GPIO19 of the ADC
SW6	Controls level shift direction for I2C lines

Figure 2-5 shows all of the positions of the different jumpers and switches on the EVM. For a full list of functionality, see List of EVM jumpers and switches.

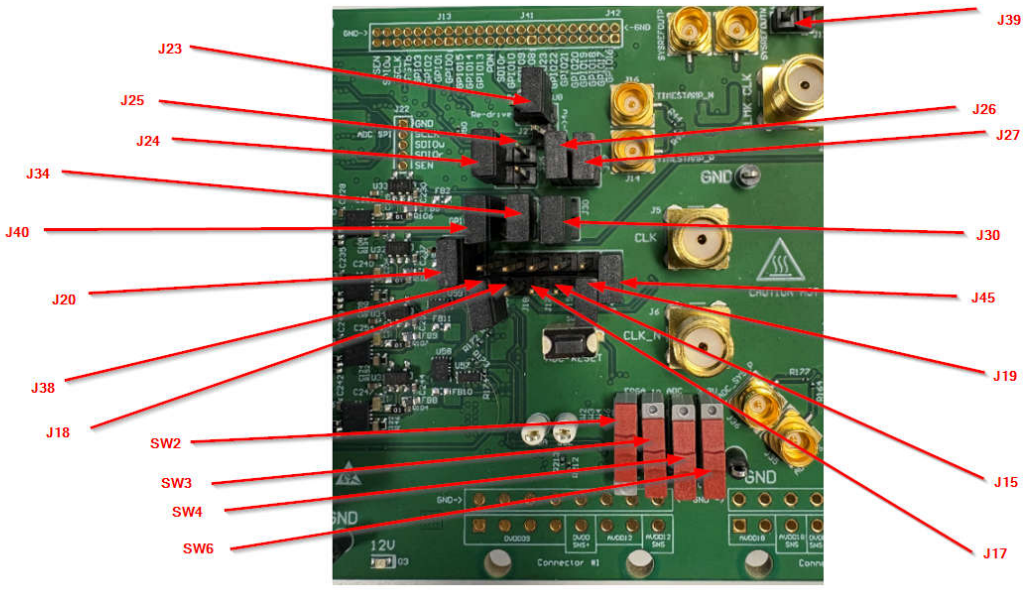


Figure 2-5. ADC3xRF72 EMV Jumper and Switch Positions

3 ADC3xRF72 EVM Configuration and Programming

This section details the bringup and programming of the ADC3xRF72 EVM into the desired mode of operation.

3.1 ADC EVM Quick Start

The first test with the ADC EVM serves as an initial “quick start” to verify there are no hardware issues and everything is functioning as expected. This section walks through step by step the setup, programming and finally capturing and analysis of signals. This section assumes steps in section Section 2 have been followed and all necessary hardware connections are made but power supplies and signal generators are turned off.

3.2 Power on all Boards and Signal Generators

1. Turn on 12V @ 5A power supply for ADC3xRF72 EVM. To verify that all of the power rails of the ADC EVM have successfully powered up, LED D2 can be checked. If this is lit up, then all power supplies have successfully powered on.
2. Power on 6V @ 5A Power supply for TSW14J58 capture card and verify that the power switch is in the “ON” position.
3. Set the ADC clock signal generator to 1.5GHz at 9dBm power. Turn this signal generator on.
4. Set the LMK clock signal generator to 1.5GHz at 9dBm power. Turn this signal generator on.
5. Set the ADC input signal generator to desired frequency (for the example an input of 125MHz is used) with power set to 0dBm.

3.3 Launch GSPS FPGA Server

Before beginning to program the ADC EVM, you must first launch the GSPS FPGA SERVER to allow for programming and data capture. This can be done by launching the application by searching for GSPS_FPGA_Server in windows search bar and launching. Once this is done a console window with the following message seen in Figure 3-1. If this message is not seen, see Section 4 for assistance.

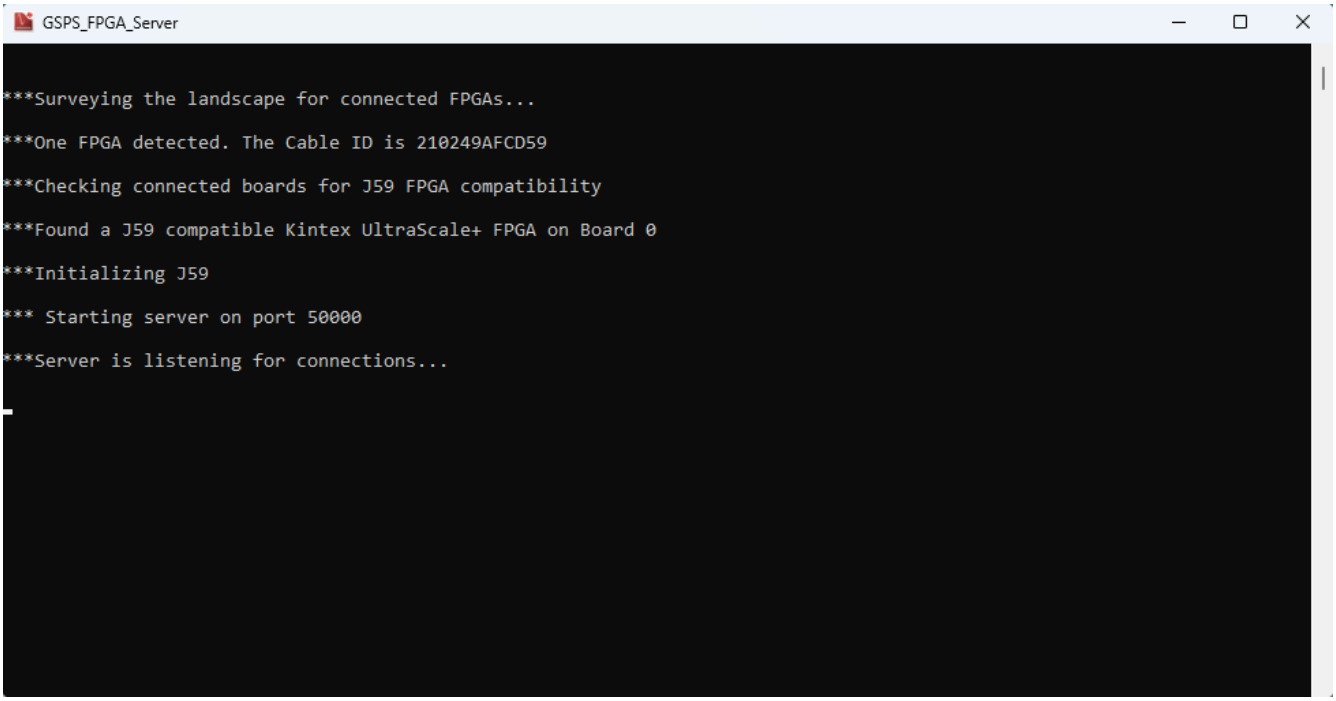


Figure 3-1. Server Listening for Connections

Once the server is launched, it does not have to be interacted with directly. All necessary communication happens via the ADC GUI.

3.4 Launch High-Speed Data Converter Professional (HSDC Pro) SW

For signal plotting and analysis High speed Data convert pro is used. To launch, locate the application and click "OK". The blank plotting screen shows, as shown in Figure 3-2. Similar to the server, this can be left on in the background and the ADC GUI can handle all of the necessary communication.

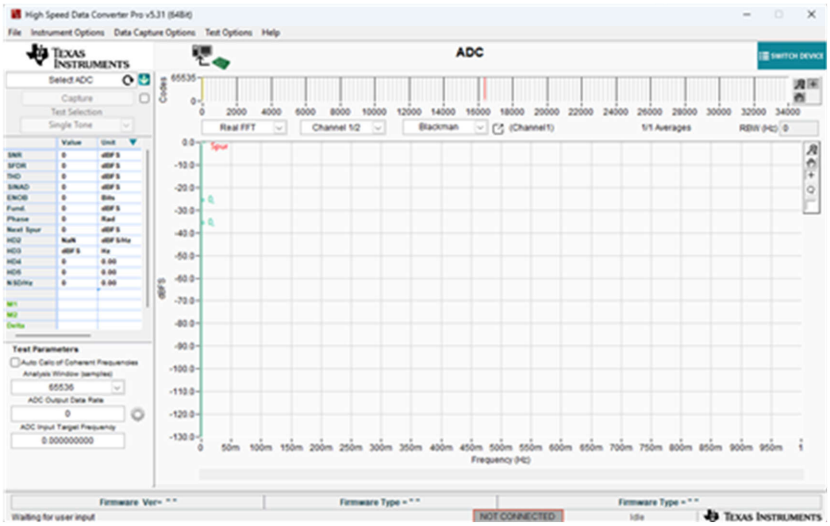


Figure 3-2. HSDC Pro

3.5 Programming the ADC

For programming, the ADC3xRF72 comes with a GUI that allows the user to configure the EVM into their desired mode of operation. The GUI can be found at the product page for the EVM on ti.com. Launch the GUI.

Note

The ADC3xRF72 EVM GUI does not support a simulation mode and must have a physical EVM connected to function correctly. If it is launched without an EVM connected, the following error message appears (as shown in Figure 3-3). This message also appears if the usb handle for the EVM does not match what is expected for the EVM. For more details and information regarding debugging this issue,see Section 4.

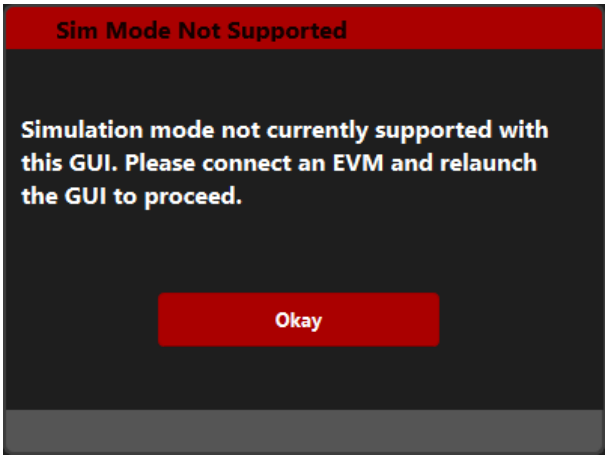


Figure 3-3. Sim Mode Not Supported

If the ADC EVM successfully connects to the GUI, it looks like Figure 3-4. The GUI comes preset to a default configuration of Sampling frequency = 1.5GHz and all internal digital signal processing bypassed. If the hardware is configured as mentioned in Section 5, then the user can simply click "program ADC" and the GUI programs the ADC, the FPGA and tries to initialize the FPGA link so that data can start to be captured.

Progress can be monitored in the below message console. If the ADC successfully programs the message, “ADC programming Success!” prints out in the console. Now the GUI starts to program the FPGA, debug messages can be seen in the message console as well but progress can also be monitored in the FPGA tab of the GUI. If the FPGA is successfully programmed and the link is successfully initialized then the following status shows in the FPGA tab. If not, then refer to Section 4 for further support.

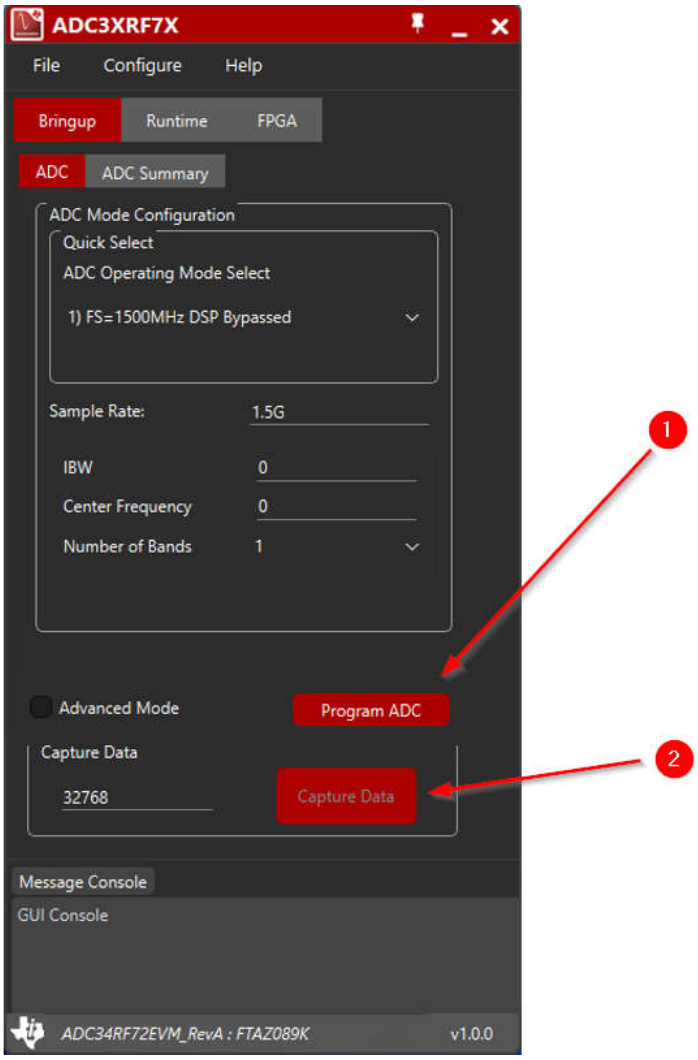


Figure 3-4. EVM GUI Program ADC

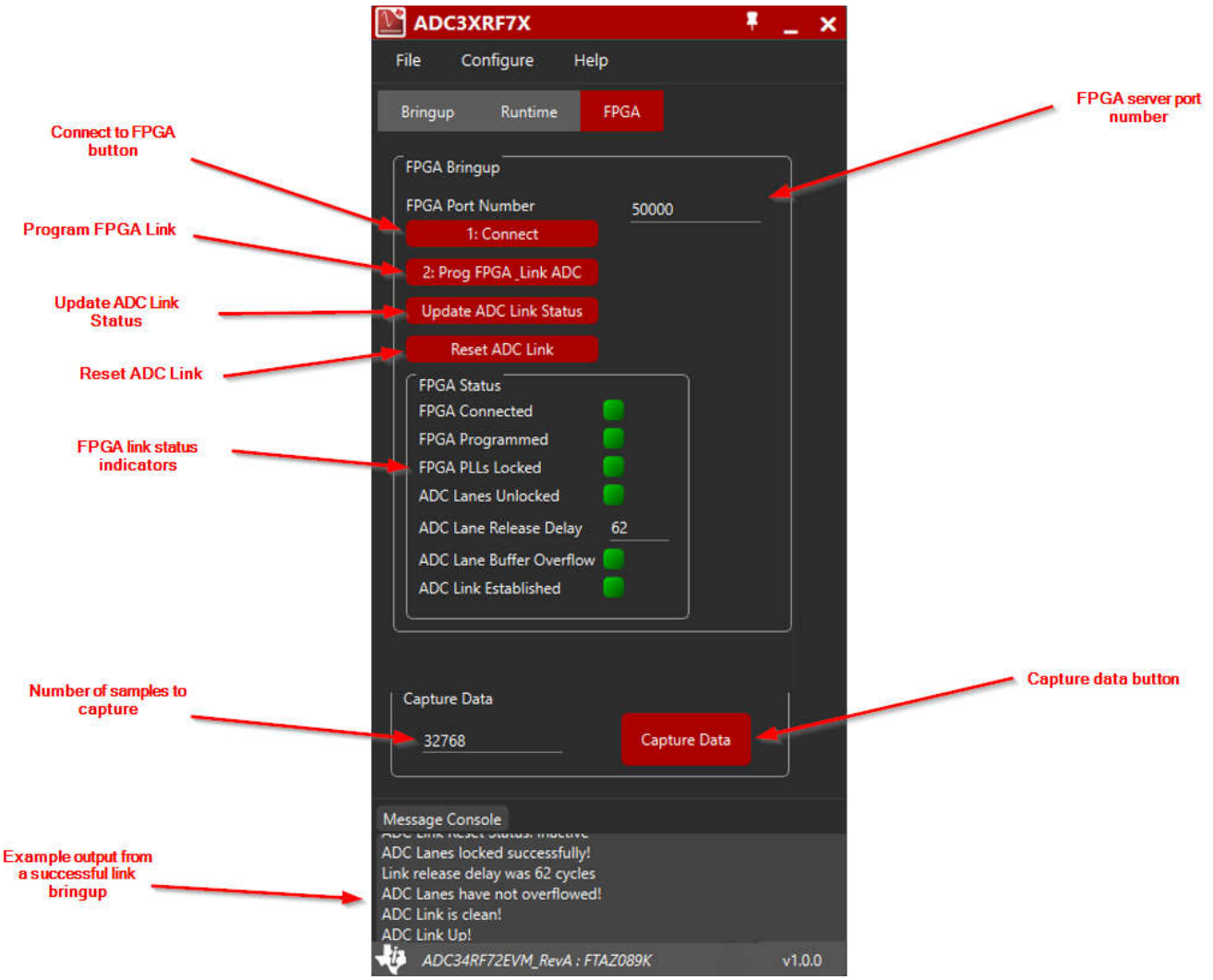


Figure 3-5. ADC GUI FPGA

If the status matches what is shown in the figure, then the data can be captured and plotted in HSDC Pro. To do this press the “Capture Data” button in the ADC GUI. The resulting data can be seen in HSDC Pro as shown in Figure 3-6.

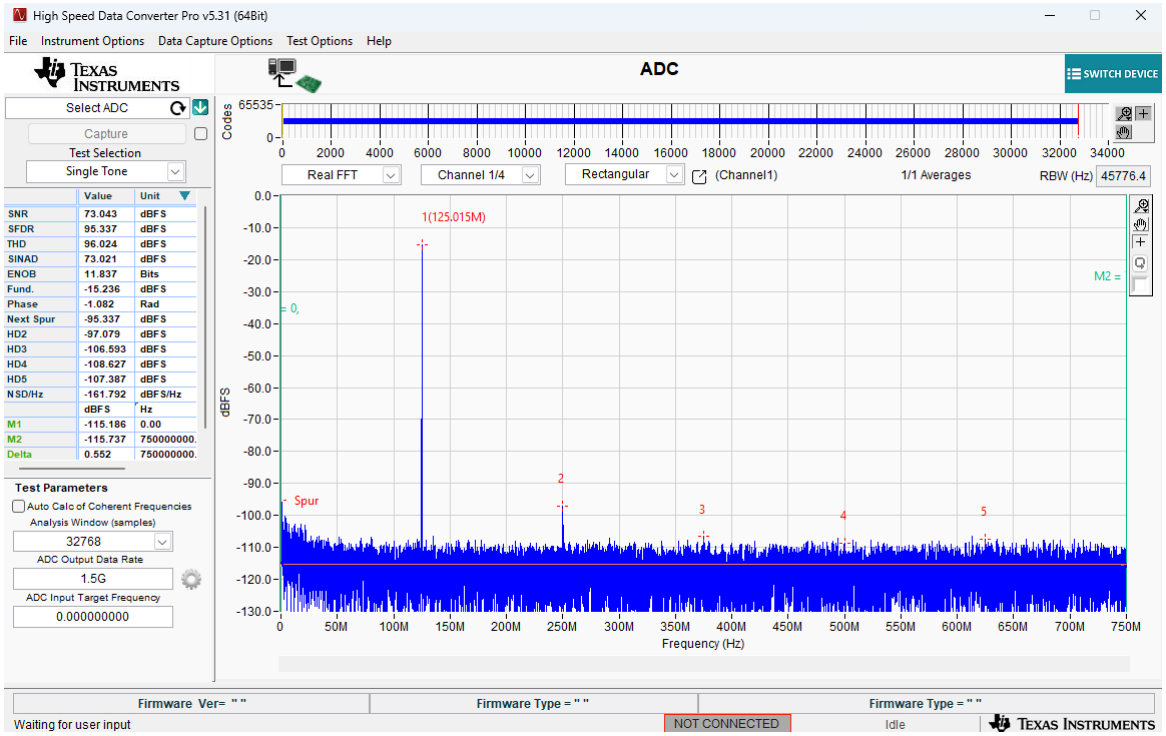


Figure 3-6. Example FFT Output Spectrum

3.6 Quick Start Mode

In addition to the default mode described above, the “FS=1500MHz DSP Bypassed” the GUI also comes with a number of pre-built configurations for users to choose from. These can be selected in the Quick Start selection drop down. Once selected the program ADC button can be clicked and the ADC and FPGA is programmed to that mode. If successful, then data can be captured and plotted to HSDC Pro.

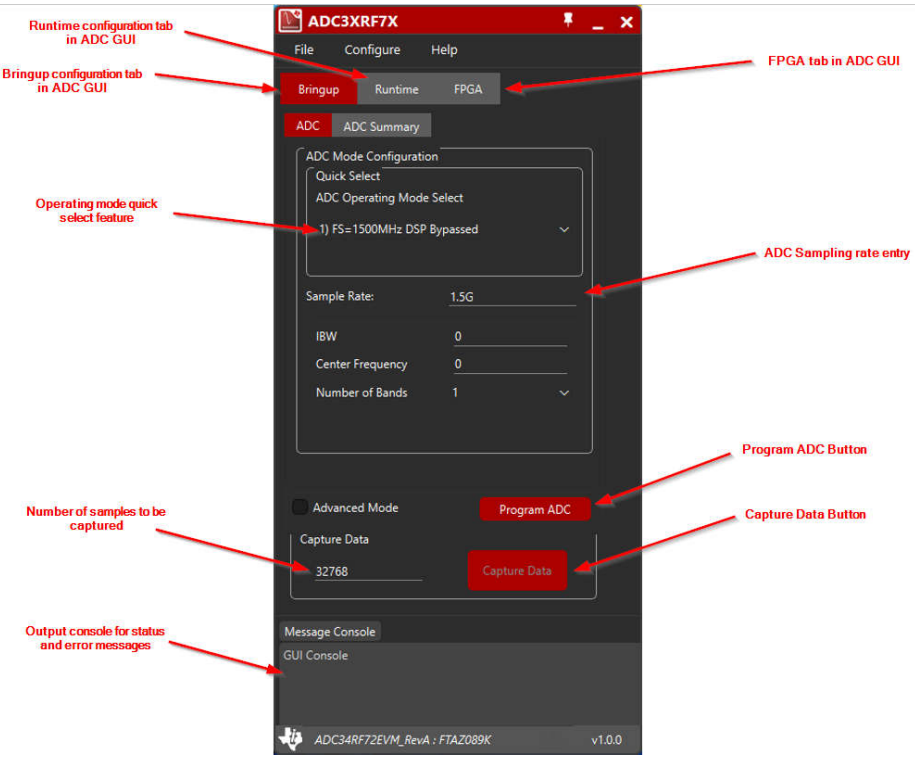


Figure 3-7. EVM GUI: Bringup ADC

3.7 System Level Configuration Mode

To allow for rapid evaluation of the ADC, the GUI supports a “System Level Configuration” mode where the user can input close to their exact system level parameters and the ADC finds the optimal mode for meeting those goals. By default, the GUI shows this mode as well as the Quick Start mode described above. The following entry’s is shown “Sample Rate”, “IBW” or instantaneous bandwidth, “Center Frequency” and “Number of Bands.” Each option is described in detail below.

- Sample Rate
  - This set the operating frequency of the ADC, this must be configured first as it sets the limit on all other selections.
- Instantaneous Bandwidth (IBW)
  - The amount of useable information bandwidth. This is determined by Nyquist's theorem (Fs/2) as well as any necessary decimation settings required. For instance, If IBW of 800 is entered the GUI updates the value to 750MHz as this is the maximum IBW that can be obtained by the part. If less IBW is required then the GUI determines the closest configuration to meet that IBW requirement for example with an Fs = 1.5GHz and a desired IBW of 225MHz the GUI finds a value of 300MHz as that is the closest value given the parts DSP options to meet that requirement.

- Center Frequency
  - IBW == Fs/2
    - Center frequency is not available as a programmable option as the ADC's internal Digital Down Converters are bypassed to preserve the full rate produced by the ADC.
    - IBW < Fs/2
      - This sets the default center frequency for the band of interest. For example, if the user signal is located at 600MHz then the center frequency of the ADC can be set to 600MHz
  - Number of Bands
    - IBW == Fs/2
      - Then number of bands is disabled and the ADC outputs four distinct bands corresponding to each ADC input
    - IBW < Fs/2
      - Number of bands == 1
        - This option outputs one complex band per ADC input (Single Band)
      - Number of bands == 2
        - This option outputs two complex bands per ADC input (Dual Band)
      - Number of bands == 4
        - This option outputs four complex bands for channels A and C of the ADC. Channels B and D are ignored in this mode of operation (Quad Band)
      - Number of bands == 8
        - This option outputs eight complex bands for just channel A (Octal Band) the other analog inputs are ignored in this mode of operation

After configuring the system level settings, the user can click the program ADC button and after the GUI is finished, begin to capture data and analyze in HSDC Pro.

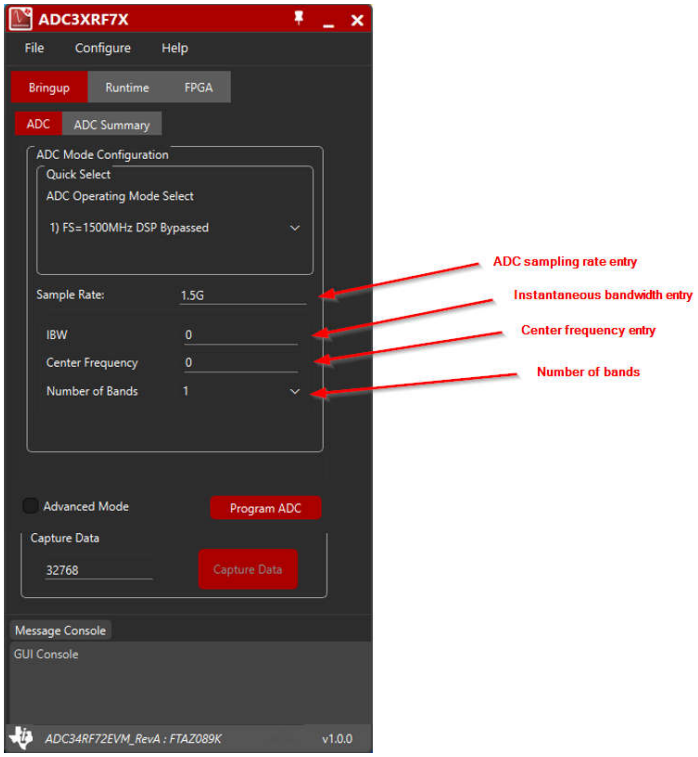


Figure 3-8. ADC GUI System Mode Labeled Image

3.8 Advanced Mode

For enhanced control, the GUI also supports an “Advanced mode” that allows the user to more closely control how the ADC is configured. This mode can be enabled by checking the “Advanced Mode” checkbox after enabling the GUI updates to look like Figure 3-9. This allows access to the “JESD” control tab where the number of lanes can be edited. The number of channel, frame octets and samplers per frame variables are inferred based on other settings of the ADC. The user can also edit the encoding scheme used by the JESD link by default “8b10b” JESD204B is chosen, but the ADC also supports 64b66b JESD204C. This tab also calculates the exact SERDES rate of the JESD link as well as the required FPGA reference clock and SYSREF frequency, which are generated on the EVM from the provided external reference clock input.

If the operating mode is changed to “Enable DSP” on the ADC tab, then this allows access to the “DSP” tab of the ADC GUI. In this tab, the user can configure the ADC to average channels A+B, C+D or A+B+C+D. The Digital Down Converters (DDC) can also be configured on this page. Based on selections on this page, the JESD page updates the number of channels required to output the ADC’s data.

Once the user is satisfied with the configuration of the ADC, they can click program and then, if successful, can capture data and plot to HSDC Pro.

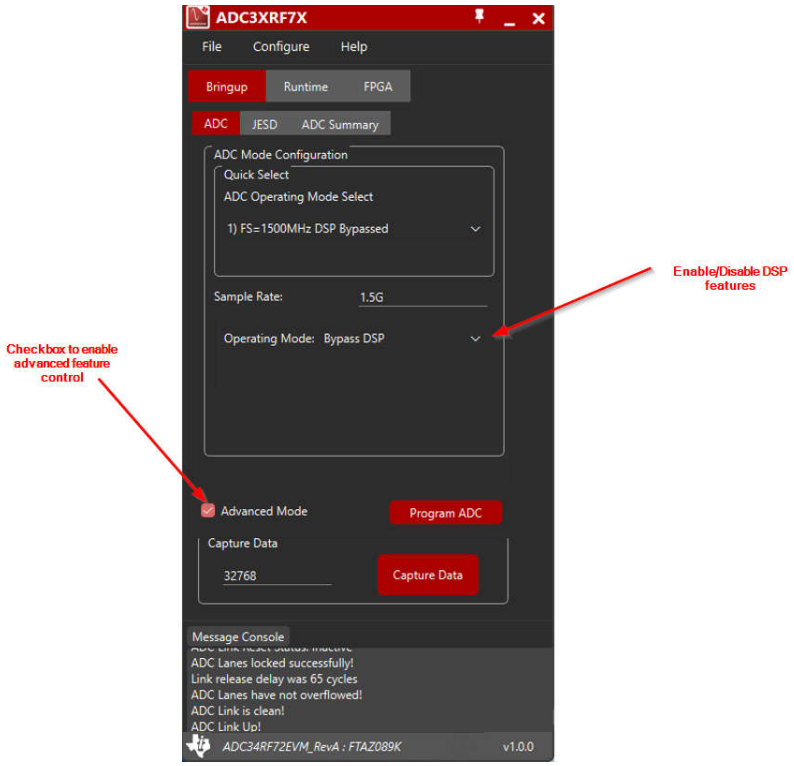


Figure 3-9. EVM GUI: Enable Advanced Control Mode

Figure 3-10 shows all the different dropdowns and entry available to the user in the DSP tab of the GUI.

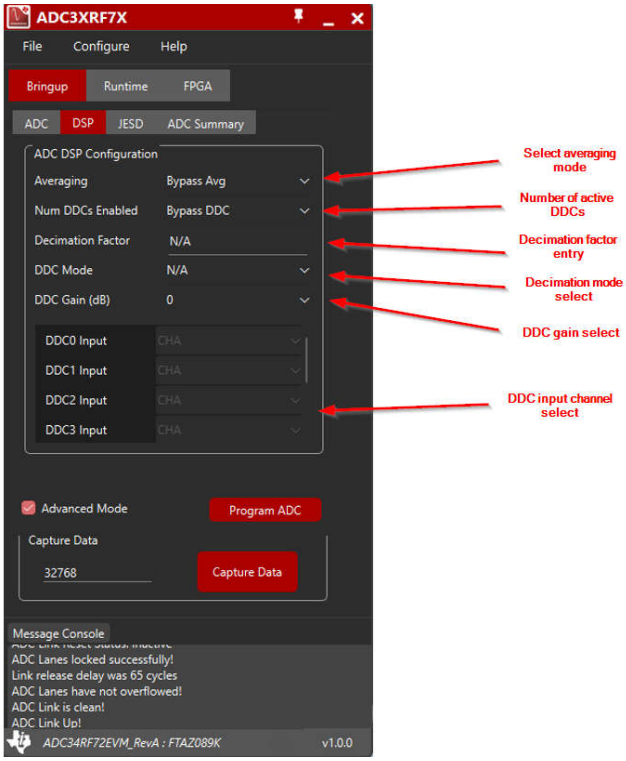


Figure 3-10. EVM GUI: DSP Tab Labeled

Figure 3-11 shows all the different dropdowns and entry available to the user in the JESD tab of the GUI.

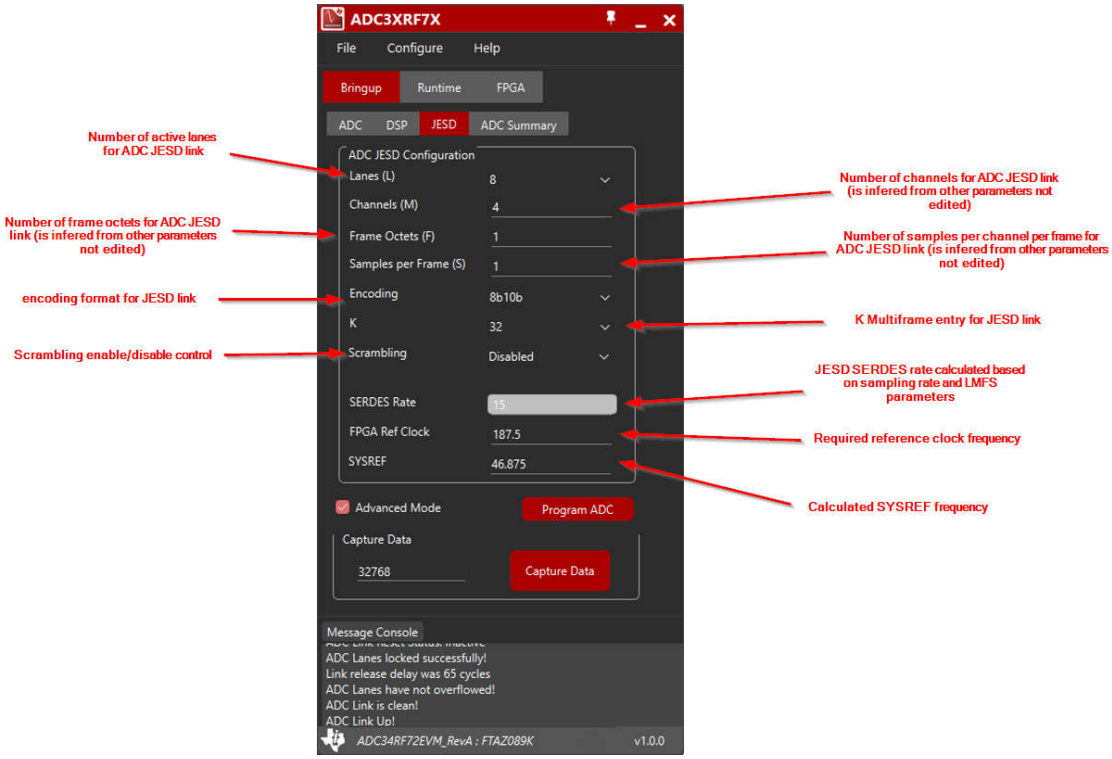


Figure 3-11. EVM GUI: JESD Tab Labeled

3.9 Runtime Configuration

The GUI also supports a number of runtime configurations and monitoring. These include editing NCO values, real time power monitoring of ADC power rails, SYSREF features.

- NCO – In this tab, the NCO frequency can be edited and adjusted real time.
- ADC power – In this tab, the real-time voltage and current can be read back for each individual power rail of the ADC so the exact power can be calculated. The ADC EVM also supports to option to margin each ADC rail to its nominal value using a feedback network of Digital potentiometers to dial in the exact feedback circuit for the power supply.
- SYSREF - In this tab the ADC SYSREF can be re armed to allow for re-synchronization.

3.10 Exporting ADC3xRF72 Configuration and Python API usage

To transfer the ADC's desired configuration from the GUI to a users application there is a feature that allows for exporting a configuration file for the ADC's desired mode of operation. To export the configuration, navigate to the "ADC Summary tab" of the GUI. Once here there is a button labeled "Export ADC System Parameters" click this button and select a valid location to save this file. Once this is done you can access the Python API files which are included in the install of the ADC3xRF72EVM GUI. Using these files, you are able to replicate the exact programming sequence performed by the GUI. For additional help with the API ,see the documentation included in the API release folder. In GUI install path ***Documents\Texas Instruments\ADC3xRF7xEVM\{GUI Version}\adc3xrf7x_customer_handoff\docs***.

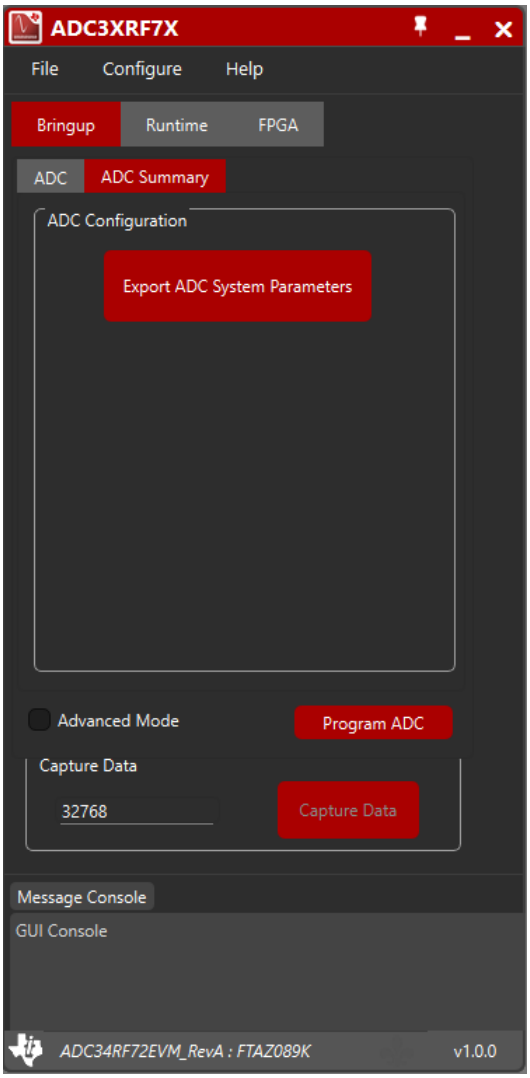


Figure 3-12. Include Picture of EVM GUI Showing Export Process

3.11 Further GUI Help

For more in depth details on the GUI operation, see the additional documentation included with the GUI install. Search the GUI install path, by default it is ***Documents\Texas Instruments\ADC3xRF7xEVM\{GUI Version}\Docs***.

4 Troubleshooting and FAQ

Table 4-1. Troubleshooting and FAQ

Issue	Troubleshooting Step
General Issues	• Verify test setup shown in section Section 2 and repeat “ADC EVM quick start” section to verify basic functionality. • Check power supply to ADC EVM and TI Capture Card. If Power good LEDs on ADC EVM are not lit up then there is likely a power supply issue. • Check signal and clock connections • Make sure that the FMC connector is tightly secured
TI Capture Card cannot connect in GSPS FPGA Server Application	• Make sure that all steps to setup 3**rd** party software are followed in section Section 2.6 • Make sure that the diligent JTAG dongle is properly connected. • Using FT_Prog search for connected USB devices and make sure that the ‘Diligent USB Device’ is found correctly. If it initially is not found, disconnect dongle from board and replug in the micro USB cable then search. • If the issue still persists, launch a command prompt and type command ‘xsdb’ to launch the Xilinx debug server. If command prompt returns the error ‘xsdb’ is not recognized as an internal or external command operable program or batch file, then it is likely the environment variables have not been setup correctly. • If xsdb launches correctly type commands “connect” and then “targets” upon successful completion of these commands the command prompt shows xcku5p as one of the targets. • If connection of board in GSPS FPGA server is still unsuccessfu, uninstall and reinstall the application
ADC EVM cannot connect in GUI	• Verify that the USB cable and daughter card are making solid connection. • Using FT_Prog verify that the ADC FTDI handle is found and matches the following “ADC3xRF72EVM_RevA”
ADC EVM fails programming	• Make sure that device clock to ADC has enough power to the EVM (9dBm) and the frequency matches what is programmed in the GUI. • Make sure that all jumpers are in the default position. Particular care that jumper J24 is installed as this controls if the SPI programming signals for the ADC come from the PC via USB or from the FPGA via JTAG. • Check that the resetb signal is held low. Using the multimeter probe RSTb signal located on the GPIO header. This signal reads approximately 1.8V indicating the ADC is not being held in reset. If this is not the case the EVM can be damaged or broken.
ADC Link fails to come up	• In FPGA tab of the ADC EVM GUI there are a number of LEDs to indicate the FPGAs status. Refer to this and the corresponding table entries below.
FPGA Connect LED not lit up	See above table Entry "TI Capture Card cannot connect in GSPS FPGA Server Application"
FPGA Programmed LED not lit up	• Verify that power supply meets the criteria of 6V, 5A. Programming the FPGA is one of the highest current draws on the FPGA. Check that during this time the power supply is not hitting its current compliance.

Table 4-1. Troubleshooting and FAQ (continued)

Issue	Troubleshooting Step
FPGA PLLs Unlocked	• Verify that EVM hardware is setup as shown in Section 2.7and reference clock to the EVM is at least 9dBm and the frequency matches what is selected in the GUI for the ADC sample frequency. • Verify that ADC Clock and reference clock are phase locked to each other. • Using Oscilloscope probe on resistor R62 and make sure that frequency matches what is shown in the ADC EVM GUI in the Bringup>JESD tab in the “FPGA Ref Clock” box.
ADC Lanes Unlocked	• Verify that programmed JESD params in the GSPS FPGA Server match what is shown in the ADC EVM GUI in the Bringup>JESD tab. • Probe resistor R204 and make sure that ADC SYSREF signal is present and matches the frequency shown in the Bringup>JESD tab in the “SYSREF” box. • Make sure that that jumper J38 is un installed, this verifies that the SYSREF signal is coming from the onboard LMK and not the smp connectors.
ADC Lanes Lock but release delay is stuck at zero	• Probe resistor R204 and make sure that ADC SYSREF signal is present and matches the frequency shown in the Bringup>JESD tab in the “SYSREF” box. • Make sure that jumper J38 is un installed, this makes sure that the SYSREF signal is coming from the onboard LMK and not the smp connectors. • Make sure that jumper J27 and J26 are installed, Jumper J25 is uninstalled and SW2 is in the “UP” position.
ADC Lane Buffer Overflow	• Probe resistor R204 and make sure that ADC SYSREF signal is present and matches the frequency shown in the Bringup>JESD tab in the “SYSREF” box. • Make sure that jumper J38 is uninstalled. This verifies that the SYSREF signal is coming from the onboard LMK and not the smp connectors. • Verify that ADC Clock and reference clock are phase locked to each other.
Sub Optimal Performance	• Verify signal quality of both clock and ADC inputs as these directly limit the ADCs performance. • Make sure that the bandpass filters are used for both ADC clock and any inputs.

5 Important Signal Routing

This section details all important signal routing on the EVM.

Table 5-1. JESD FMC Data Routing

ADC JESD Output (p,n)	FMC Pin Number (p,n)	Physical Routing P/N Inversion	Schematic Net Name (p,n)
STXOUT0	(A18,A19)	N	DOUT0_FMC
STXOUT1	(B16,B17)	N	DOUT1_FMC
STXOUT2	(A14,A15)	N	DOUT2_FMC
STXOUT3	(B12,B13)	N	DOUT3_FMC
STXOUT4	(A2,A3)	Y	DOUT4_FMC
STXOUT5	(C6,C7)	Y	DOUT5_FMC
STXOUT6	(A6,A7)	Y	DOUT6_FMC
STXOUT7	(A10,A11)	Y	DOUT_7_FMC

Table 5-2. Additional JESD FMC Signal Routing

Signal Description	FMC Pin Number	Schematic Net Name
Transceiver Reference Clock 0 (P,N)	D4,D5	MGTREFCLK0_FMC_P/N
Transceiver Reference Clock 1 (P,N)	D4,D5	MGTREFCLK1_FMC_P/N
JESD Application Layer Clock	G6,G7	LMK_CORECLK_P/N
SYSREF	G9,G10	FPGA_SYSREF_P/N
Hardware Sync	H31	GPIO_MUX_0_FPGA

Table 5-3. Other FMC Signals

Signal Description	FMC Pin Number	Schematic Net Name
Carrier card IO voltage level adjust	E39,F40,G39,H40	VADJ
SCLK from carrier card at carrier voltage IO level	G12	SCLK_FMC_VADJ
SDI write from carrier card at carrier voltage IO level. Is SDI line for both ADC3xRF72 and LMK04828	G13	SDI_FMC_VADJ
SDO read from carrier card at carrier voltage IO level. Is SDO line for both ADC3xRF72 and LMK04828	G15	SDO_FMC_VADJ
SPI chip select for LMK04828	G16	CSb_LMK_FMC_VADJ
SPI chip select for ADC3xRF72 SPI from carrier card at carrier voltage IO level	C18	SEN_ADC_FMC_VADJ
Active low ADC3xRF72 hardware reset	H13	RSTb_ADC_FMC_VADJ
ADC3xRF72 power down	H14	PDN_ADC_FMC_VADJ
I2C clock	C30	SCL_FMC
I2C Data	C31	SDA_FMC

5.1 ADC Device Clock Routing

Figure 5-1 shows the clocking system for the EVM. In addition, optional clocking modifications are listed below and highlighted in red in the block diagram. A schematic snippet is also included for clarity.

- Differential Clock input to ADC (Bypass on board balun).
  - By default the EVM is configured to accept a single ended clock for convenience but the board can be modified so an external differential signal can be provided. This modification can be done by making the following modification.
  - Remove C20, C19, C22
  - Install C17, C18, C23 as 0.1uF 0201 capacitors.
- LMK04828 source clock shared from device clock input.
  - By default the board is configured so the device clock and LMK04828 reference clock come from two separate sources. There is an option to split the device clock input so it can be used as the reference clock to the LMK04828 as well. Note, this requires a higher power clock signal input to the EVM to account for the extra loss introduced by the splitting of the signal. This modification can be done by making the following modification.
  - Remove R15, R16 and R33.
  - Install R15, R16, R18 as 16 0201 resistors.
  - Install C55 as 0.1uF capacitor.

Figure 5-1 shows the clocking sub system for the EVM board. The red lines indicate the various optional clocking modifications.

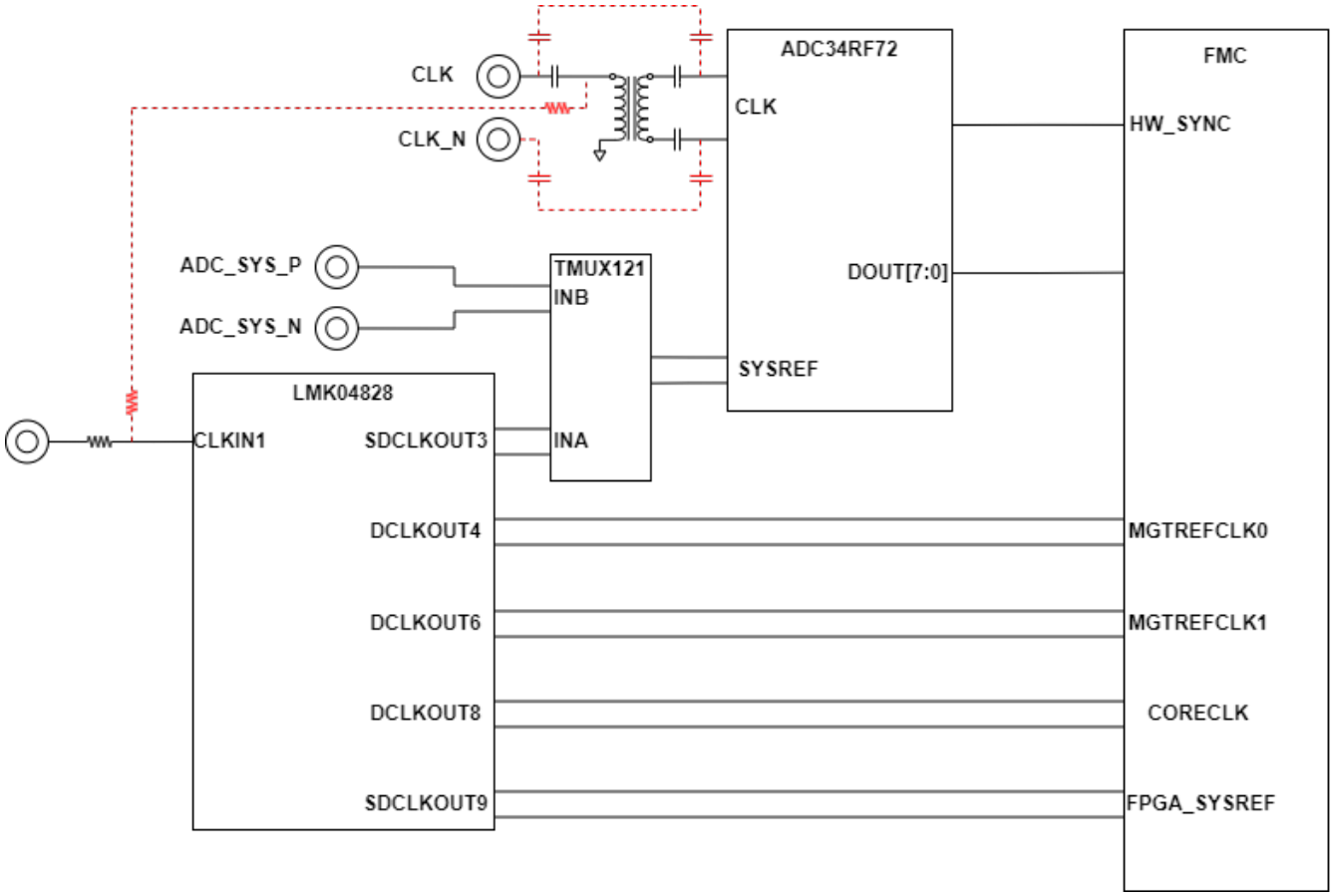


Figure 5-1. ADC3xRF72 Clock Routing

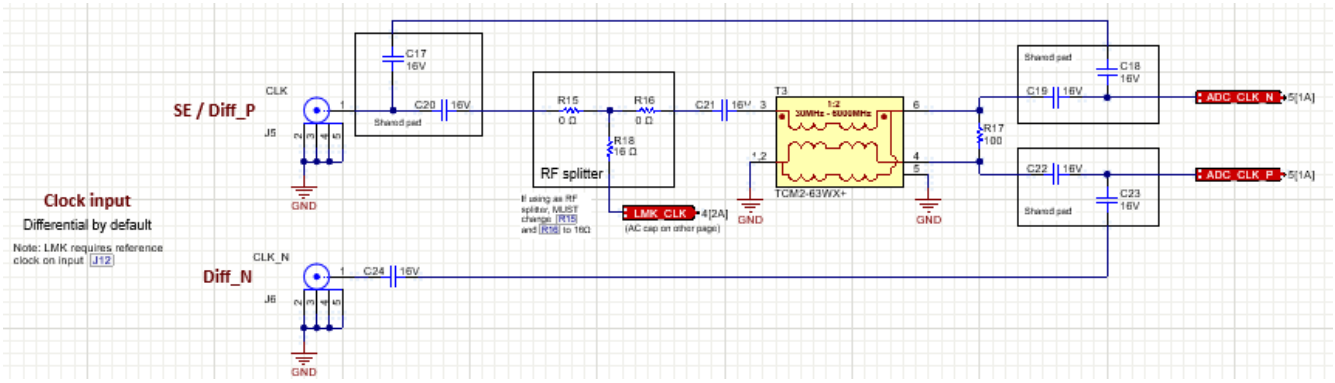


Figure 5-2. ADC3xRF72 EVM Clock Input Schematic Snippet

5.2 Board Modifications

5.2.1 ADC3xRF72 Analog Inputs

The ADC3xRF72 has four analog inputs and the EVM routes all four as length matched signals. The default comes configured as single ended inputs that are AC couple and then SE-DIFF converted using the on board balun. There is also space on the EVM for a matching network to experiment with different matching networks depending on the application requirements.

The EVM can also be configured to accept an external differential signal with the following modifications. For components to bypass on board baluns, see Figure 5-3 through Figure 5-6.

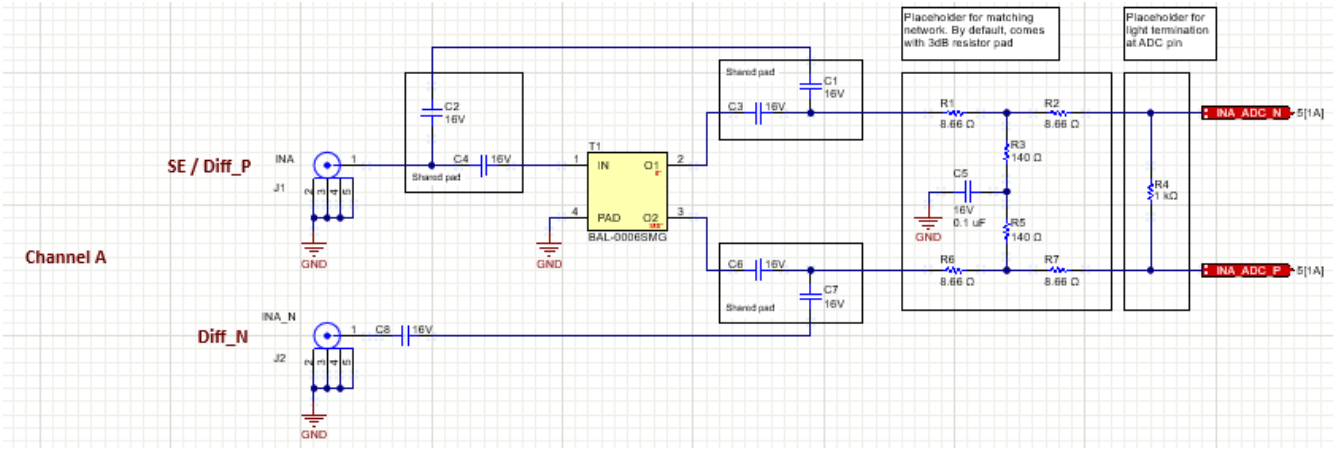


Figure 5-3. ADC3xRF72 EVM Input A Analog Input Schematic Snippet

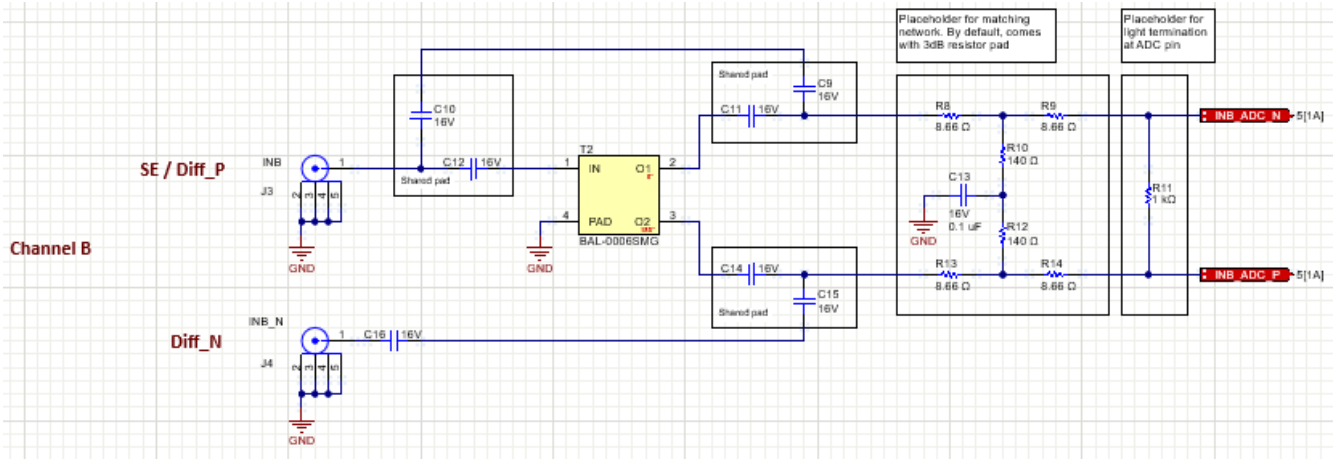


Figure 5-4. ADC3xRF72 EVM Input B Analog Input Schematic Snippet

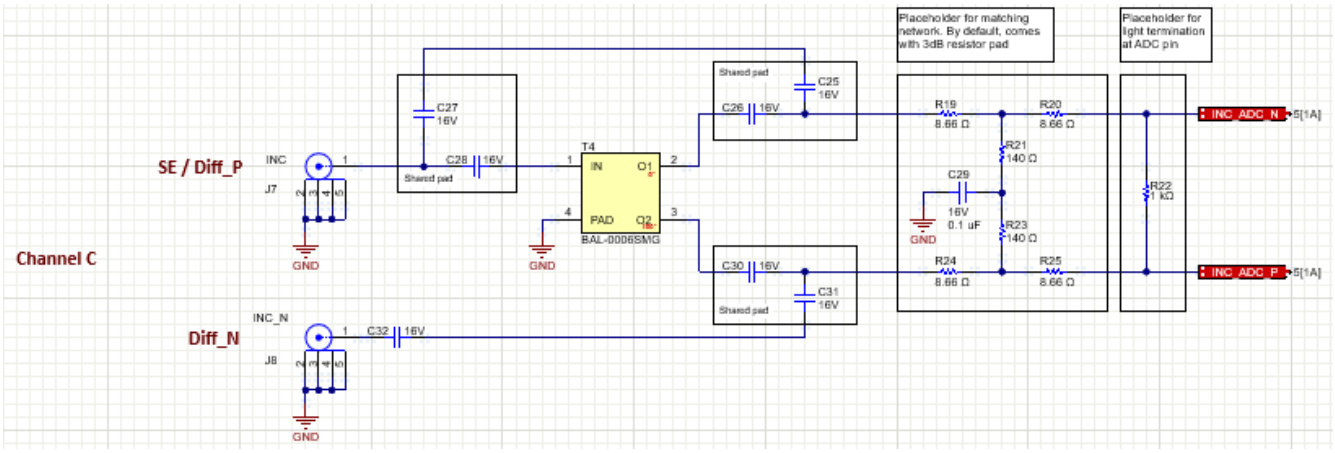


Figure 5-5. ADC3xRF72 EVM Input C Analog input Schematic Snippet

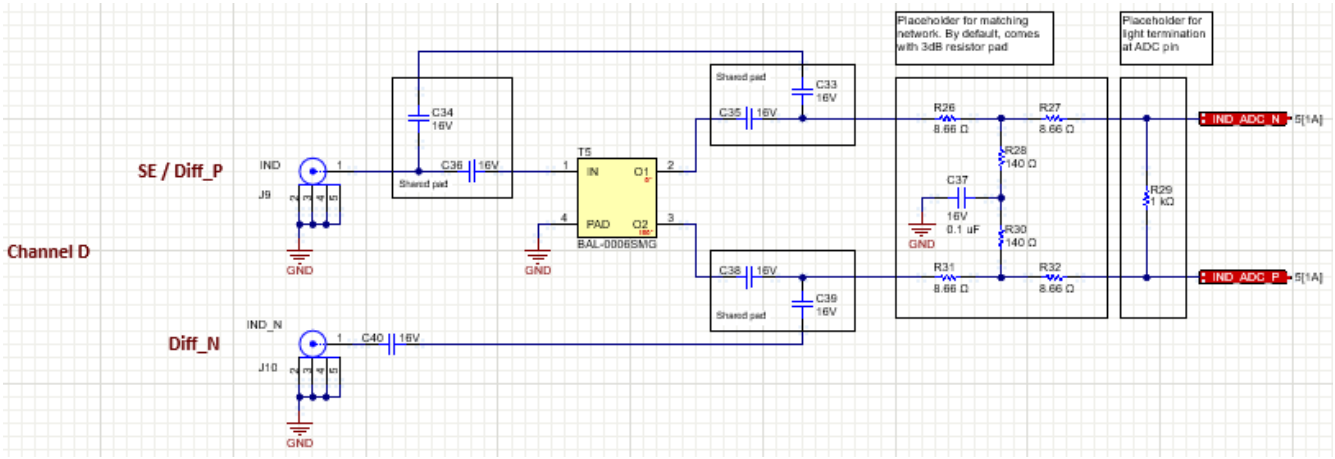


Figure 5-6. ADC3xRF72 EVM Input D Analog Input Schematic Snippet

6 Hardware Design Files

6.1 Schematics

The schematics are available on the product page: (ADC34RF72EVM web page).

6.2 PCB Layouts

The PCB layout is available on the product page: (ADC34RF72EVM web page).

6.3 Bill of Materials (BOM)

The bill of materials is available on the product page: (ADC34RF72EVM web page).

7 Additional Information

7.1 Trademarks

All trademarks are the property of their respective owners.

8 References

- *ADC3xRF72 Quad Channel 14-bit 1.3 GSPS RF Sampling Data Converter Data Sheet* (SBASAL0)

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   2.3 TI's sole liability shall be at its option to repair or replace EVMs that fail to conform to the warranty set forth above, or credit User's account for such EVM. TI's liability under this warranty shall be limited to EVMs that are returned during the warranty period to the address designated by TI and that are determined by TI not to conform to such warranty. If TI elects to repair or replace such EVM, TI shall have a reasonable time to repair such EVM or provide replacements. Repaired EVMs shall be warranted for the remainder of the original warranty period. Replaced EVMs shall be warranted for a new full ninety (90) day warranty period.

WARNING

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NOTE:

EXPOSURE TO ELECTROSTATIC DISCHARGE (ESD) MAY CAUSE DEGREDATION OR FAILURE OF THE EVALUATION KIT; TI RECOMMENDS STORAGE OF THE EVALUATION KIT IN A PROTECTIVE ESD BAG.

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3.1.1 *Notice applicable to EVMs not FCC-Approved:*

FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247*

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

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Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

3.3 *Japan*

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。

https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-delivered-in-japan.html

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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3.4.1 *For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive)*:

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

4 *EVM Use Restrictions and Warnings:*

4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.

4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3 *Safety-Related Warnings and Restrictions:*

4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.

5. *Accuracy of Information:* To the extent TI provides information on the availability and function of EVMs, TI attempts to be as accurate as possible. However, TI does not warrant the accuracy of EVM descriptions, EVM availability or other information on its websites as accurate, complete, reliable, current, or error-free.

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