EVM User's Guide: UCC35341-Q1, UCC34141EVM-116

UCC35341-Q1 2W Bias Evaluation Module

Description

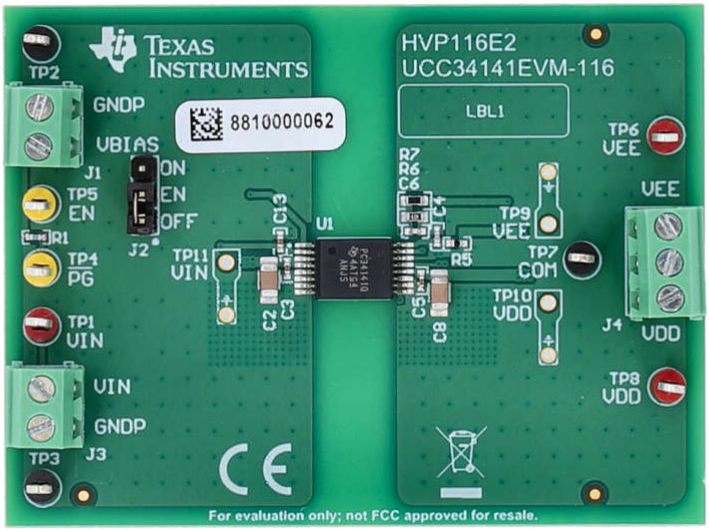
This evaluation module (EVM) accepts the UCC35341-Q1 as a drop-in, pin-to-pin compatible, 2W variant of the UCC34141-Q1, 1.5W bias module. The UCC34141EVM-116 EVM operates from 5.5VIN to 20VIN and is configured for dual outputs of VDD=18V and VEE= -5V.

Features

- Pin-to-pin compatible with UCC34141-Q1
- High power density
- >5kV$_{RMS}$ isolation
- Open drain /power good (PG) signal
- Integrated protections: Undervoltage Lockout (UVLO), Overvoltage Lockout (OVLO), short-circuit, Overvoltage Protection (OVP), Under Voltage Protection (UVP), and thermal shutdown.
- ENA pin for logic enable, ON/OFF control
- AEC-Q100 qualified for automotive applications: -40°C≤T$_A$≤125°C

Applications

- Hybrid, electric and power train systems (EV/HEV)
  - HEV/EV inverter and motor control
  - HEV/EV OBC and DC/DC converter
  - DC/DC converters
- Energy infrastructure
  - DC fast charging power module
  - DC fast charging station
  - String inverter
- Industrial automation
  - Off-highway vehicle electric drive
- Power delivery
  - Rack and server power



1 Evaluation Module Overview

1.1 Introduction

This user's guide provides a description as well as directions for use of the UCC34141EVM-116, EVM variant 002, to evaluate the UCC35341-Q1, high frequency, integrated transformer, DC-DC converter module from Texas Instruments. This EVM allows designers to quickly and efficiently evaluate the UCC35341-Q1 for use in automotive or industrial applications requiring gate driver IC bias power as high as 2W, meeting up to $5kV_{RMS}$ isolation.

The UCC35341-Q1 is pin-to-pin compatible with UCC34141-Q1 and can be evaluated by ordering the UCC34141EVM-116 EVM and contacting your dedicated TI Technical Sales Representative or Field Applications Engineer to request IC samples of UCC35341-Q1. Remove the UCC34141-Q1 IC and replace it with UCC35341-Q1.

The UCC35341-Q1 is a high efficiency, low-emissions, $5kV_{RMS}$ Isolated DC-DC Converter capable of delivering 2-W of power. Since the UCC35341-Q1 provides isolated power in an integrated package, this allows systems to reduce cost and size by removing the need for separate isolated power supplies. The UCC35341-Q1 delivers class-leading power density and highest efficiency while removing the need for bulky external transformers or power modules commonly used in existing designs. This integration allows for minimal printed circuit board (PCB) area as well as decreased height profile.

1.2 Replace U1: Solder reflow

The UCC34141-Q1 is the default IC used in the UCC34141EVM-116, but any of the alternate versions listed in Table 1-1 can be used for evaluation. Each of the component versions listed in Table 1-1 are pin-to-pin compatible.

Table 1-1. U1 Component Selection

General Part Number	Orderable Part Number	Power Good Active Polarity	Fault Response
UCC34141-Q1	UCC34141QDHARQ1	LOW	Latch-OFF
UCC34141-Q1	PUCC34141QDHARQ1		
UCC34141D-Q1	UCC34141DQDHARQ1	HIGH	Auto-Restart
UCC34141D-Q1	PUCC34141DQDHARQ1		
UCC35341-Q1	UCC35341QDHARQ1	LOW	Latch-OFF
UCC35341-Q1	PUCC35341QDHARQ1		

When performing solder rework by hand, the recommended solder profile used in manufacturing is often not easily followed on the lab bench. Please exercise appropriate ESD material handling precautions and use caution when soldering, especially with forced air solder equipment. For IC removal, use only just enough hot air focused at the pins while gently lifting upward on the IC package body so that as soon as the solder begins to reflow, the IC is lifted off the PCB. Recommend to set the hot air temperature to no more the 250°C with minimal forced air. For IC install by hand, recommend to hand solder with solder iron if possible, otherwise, follow similar guidance if hot air must be used.

1.3 Replace R1:

Replace R1 according to Table 4. EVM Component Changes to Evaluate UCC35341-Q1.

1.4 Kit Contents

- 1 - PCB1/HVP116E2 - UCC34141EVM-116

1.5 Specification

V_{IN}=12V, V_{DD}-COM=18V, V_{EE}-COM=-5V, T_A=25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS						
V_{IN}	Input voltage range	$P_{VDD-COM}$=2W	10	12	17	V
		$P_{VDD-COM}$=1.5W	9	12	20	V
V_{IN_ON}	Input voltage on		7		8	V
V_{IN_OFF}	Input voltage off		6.3		7.3	V
OUTPUT CHARACTERISTICS						
V_{DD}-COM	DC full load set-point	10V<V_{IN}<17V, I_{VDD}=112mA		18		V
I_{VDD}	V_{DD} load current range	10V<V_{IN}<17V	0		112	mA
P_{MAX}	Maximum output power	10V<V_{IN}<17V, I_{VDD}=112mA			2	W
V_{EE}-COM	DC full load set-point			-5		V

1.6 Device Information

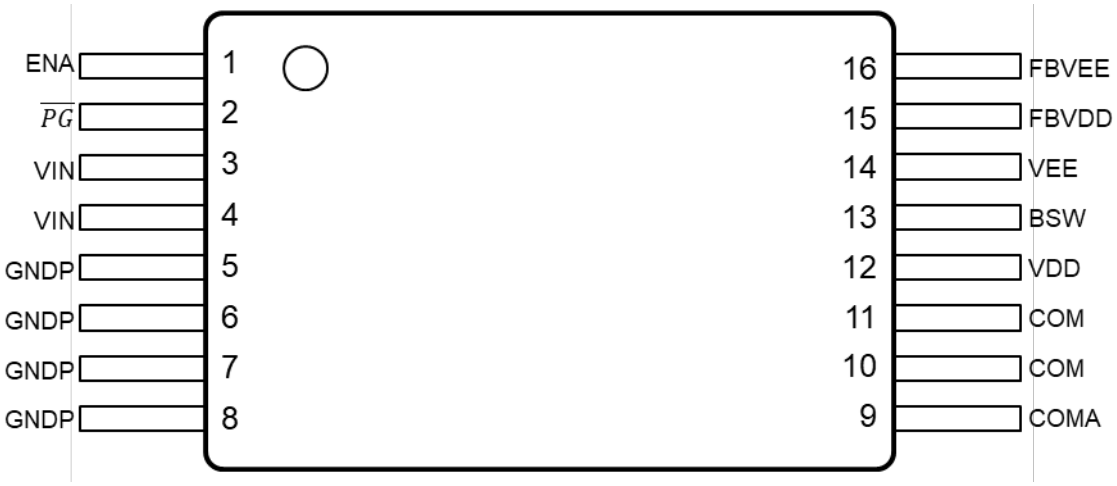


Figure 1-1. UCC35341-Q1 Package Top View

Table 1-2. UCC35341-Q1 Pin Description

Pin		Type [1]	Description
Name	**No.**		
ENA	1	I	Enable pin. Forcing ENA LOW disables the device. Pull HIGH to enable normal device functionality. 5.5V recommended maximum. Can be used to program input UVLO with a resistor divider from VIN.
/PG	2	O	Active low power-good open-drain output pin. PG remains low when: VVIN_UVLOP ≤ VVIN ≤ VVIN_UVLOP; VVDD_UVP ≤ VFBVDD ≤ VVDD_OVP; VVEE_UVP ≤ VFBVEE ≤ VVEE_OVP; TJ_Primary ≤ TSHUT_P_R and TJ_secondary ≤ TSHUT_S_R.
VIN	3,4	P	Primary input voltage. Connect a 10µF and a parallel 0.1µF ceramic capacitor from VIN to GNDP. The 0.1µF ceramic capacitor is for by-passing the high frequency noise and must be next to the VIN and GNDP pins
GNDP	5, 6, 7, 8	G	Primary-side ground connection for VIN. Place several vias to copper pours for thermal relief. See PCB Layout Example section for more details.

Table 1-2. UCC35341-Q1 Pin Description (continued)

Pin		Type [1]	Description
Name	No.		
COMA	9	G	Secondary-side analog sense reference connection for the noise sensitive analog feedback input FBVDD, and FBVEE. Connect the low-side FBVDD feedback resistor and high frequency decoupling filter capacitors close to the COMA pin and respective feedback pin FBVDD. Connect to secondary-side gate drive voltage reference, COM. Use a single point connection and place the high frequency decoupling ceramic capacitor close to the COMA pin.
COM	10, 11	G	Secondary ground. Connect to Source of power switch.
VDD	12	P	Secondary-side isolated output voltage from transformer. Connect a 10µF and a parallel 0.1µF ceramic capacitor from VDD to COM. The 0.1µF ceramic capacitor is for bypassing high frequency noise and must be next to the VDD and COM pins.
BSW	13	P	Internal buck-boost converter switch pin. Connect an inductor from this point to COM. Recommend a 3.3µH to 10µH chip inductor.
VEE	14	P	Secondary-side isolated output voltage for negative rail. Connect a 2.2µF ceramic capacitor from VEE to COM for bypassing high frequency noise.
FBVDD	15	I	Feedback (VDD – COM) output voltage sense pin and to adjust the output (VDD – COM) voltage. Connect a resistor divider from VDD to COM so that the midpoint is connected to FBVDD. The equivalent FBVDD voltage is regulated at 2.5V with the internal hysteresis control across isolation. Adding a 220pF ceramic capacitor for high frequency decoupling in parallel with the low-side feedback resistor is needed. The 220pF ceramic capacitor for high frequency bypass must be next to the FBVDD and COMA pins on top layer or back layer connected with vias.
FBVEE	16	I	Feedback (COM – VEE) output voltage sense pin used to adjust the output (COM – VEE) voltage. Connect one feedback resistor, 40kΩ to 160kΩ, to VEE to program the (COM – VEE) voltage from 2V and 8V. The equivalent FBVEE voltage is regulated close to 0V with the internal hysteresis control. Connect a 10pF ceramic capacitor from FBVEE to COMA for bypassing high frequency noise. The 10pF ceramic capacitor must be next to the FBVEE pin on top layer or back layer connected with vias.

1. TYPE: P=Power, PG=Primary Ground, SG=Secondary Return, SGA=Secondary Return Analog, I=Input, O=Output

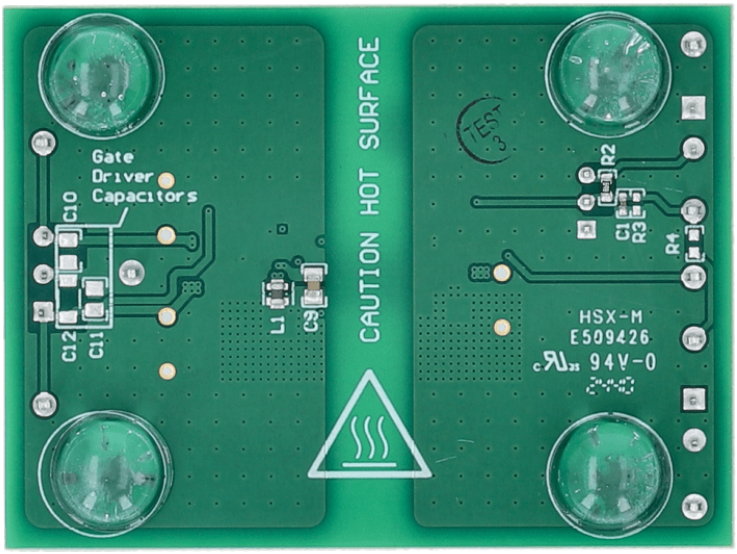
2 Hardware

WARNING

- **Caution Hot Surface. Contact may cause burns. U1 package surface can reach temperatures of 45°C above ambient. Do not touch!**
- **If you are not trained in proper safety, handling and testing power electronics, please do not test this EVM**

2.1 Additional Images

The UCC34141EVM-116 is intended to allow designers to evaluate the performance characteristics and capabilities of the UCC35341-Q1 quickly and easily for use in automotive, isolated, gate driver bias applications as well as a variety of isolated industrial bias power applications. The EVM allows users to test functions of the UCC35341-Q1 such as: Enable/Disable (EN) of the device as well as configure the isolated output voltage for 15V<VDD<20V, and -8V<VEE<0V and easily apply variable loads to the outputs. This EVM allows the user to measure efficiency across the input voltage range and varying output loads according to system requirements. Another feature of the EVM is the ease of probing during test. Test points, are strategically placed and described according to Table 3.



UCC34141EVM-116, HVP116E2, Bottom View

2.2 Power Requirements

2.3 Recommended Test Equipment

1. V_{BIAS}: DC power supply1: 5V, 10mA
2. V_{IN}: DC power supply2: 20V, 500mA
3. I_{VDD}: Electronic load (set to constant resistance) or fixed resistor: 18V, 112mA
4. I_{VEE}: Electronic load (set to constant resistance) or fixed resistor: 5V, 65mA
5. (3) DVMs measuring DC voltage <30V
6. (3) DVMs measuring DC current <200mA on I_{VDD}, I_{VEE}, <500mA on I_{VIN}
7. Oscilloscope: 4-channel, 500MHz or better, voltage probes, current probes
8. Minimum wire gauge 20 AWG to 22 AWG or better
9. Thermal camera (optional) or thermocouple to measure U1 case temperature

2.4 Setup

2.5 External Connections for Easy Evaluation

The UCC34141EVM-116 utilizes screw terminals for quickly connecting to V_{IN}, VDD and VEE. Connecting the appropriate ammeters and voltmeters, as shown in Figure 2-1, allows accurate EVM efficiency measurements to be made.

Connecting test equipment:

1. Move shunt jumper, SH-J1 into the J2, 1-2, EN OFF position. This assures the EVM cannot start while test equipment is being connected.
2. Connect a +5V DC bias power supply J1:1-2 (+3.3V to +5V). Set the power supply to 0V. The +5V supply at J1 will serve as the pullup bias for /PG and ENA. Turn off/disable the +5V DC Bias power supply.
3. Connect the V_{IN} DC power supply capable of 5V<V_{IN}<20V, 500mA at J3:1-2 (V_{IN}). Adjust the power supply to 12V, and set the current limit to 1A. Turn off/disable the V_{IN} power supply.
4. Connect a variable load between J4:1 (VDD) and J4:2 (COM). If using an electronic load, set to constant resistance (CR), 650Ω (~500mW). Leave the load disabled until the EVM is powered.

5. Connect a second load between J4:2 (COM) and J4:3 (VEE). If using an electronic load, set to constant resistance (CR), 250Ω (~10mW). Leave the load disabled until the EVM is powered. Since the required load is small, a through-hole, 500mW, load resistor can be connected between J4:2-3.
6. Some electronic loads may not be able to regulate/stabilize CC when setting in the low mA range. Monitor the input current and load currents by inserting ammeters as shown in Figure 2-1. A current probe can be used with the oscilloscope to verify the stability of the DC current being regulated by an electronic load.

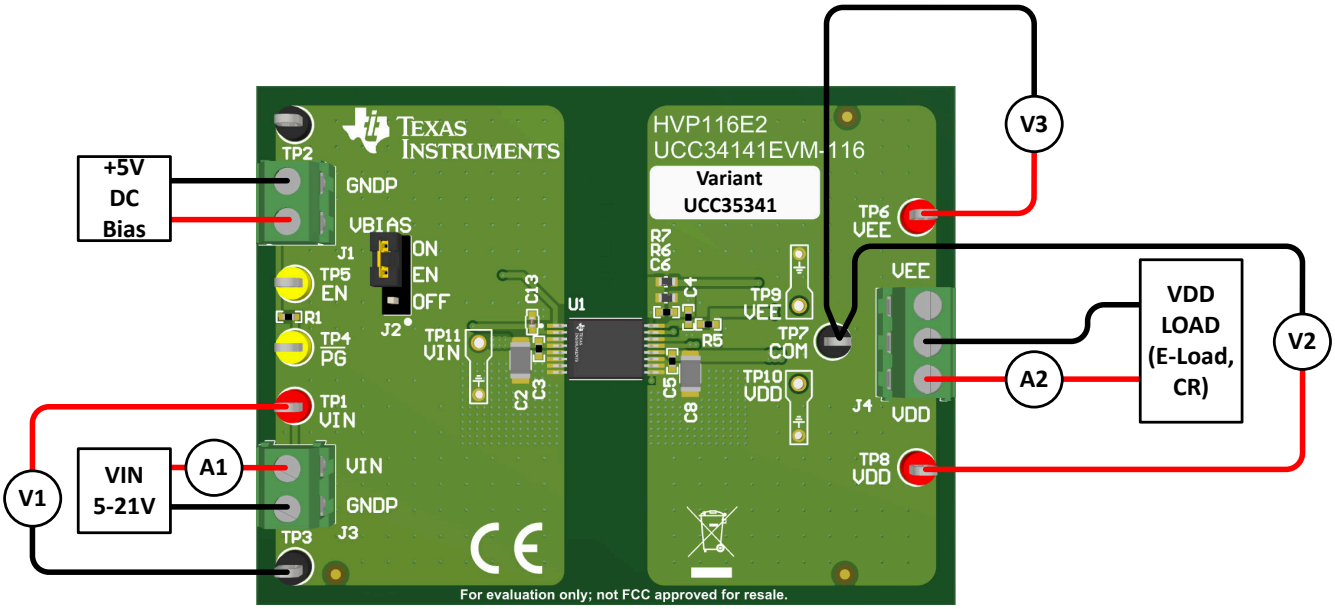


Figure 2-1. Typical Efficiency Measurement Setup

Power on for start-up:

1. Verify V_{IN} and +5V DC Bias power supplies are off/disabled and no voltage is applied to the UUT
2. Move shorting jumper, SH-J1, into the J2:2-3, EN ON position. NOTE: removing the shorting jumper, SH-J1 also results in EN ON.
3. Turn on the V_{IN} DC power supply. Verify 12V is present at TP1-to-TP3
4. Verify the loads on VDD and VEE are disabled
5. Turn on the +5V DC bias power supply. EVM is now enabled with VDD and VEE in regulation under no load condition.
6. Verify +18V present on VDD-COM, and -5V present on VEE-COM
7. Enable the load on VDD, enable the load on VEE
8. The UCC35341-Q1 is now regulating VDD and VEE and processing ~0.5W of isolated output power
9. Vary V_{IN} between 5V<V_{IN}<20V, vary I_{VDD} between 0mA<I_{VDD}<112mA, Vary I_{VEE} between 0mA<I_{VEE}<6mA.
10. Insert oscilloscope probes into TP9, TP10 and TP11 for measuring VEE, VDD and V_{IN} startup, steady state and AC ripple voltage

Power off for shutdown:

1. Move shorting jumper SH-J1 into the J2:1-2, EN OFF position
2. Turn off +5V, DC bias power supply
3. Disable I_{VDD} load
4. Disable I_{VEE} load
5. Turn off V_{IN} power supply

2.6 Test Points

Table 2-1 describes the various EVM test points, allowing easy access for connecting oscilloscope probes, DVM test leads and wire connections to lab test equipment as outlined in Recommended test equipment. Pay attention to maintain separation between the primary side, GNDP and secondary side, COM. Primary-side test points are not to be referenced to COM through improper test equipment insertion. Likewise, secondary-side test points are not to be referenced to GNDP through improper test equipment insertion.

Table 2-1. Input, Output, Test Point (I/O/TP) Description

PIN	I/O/TP	COLOR	DESCRIPTION	MIN	TYP	MAX	UNIT
J1	I	Green	V_{BIAS}, EN and /PG bias	3	V_{BIAS}	5	V
SH-J1	I	Black	J2 shorting jumper		0		V
J2:1-2	I	Black	EN, off		0		V
J2:2-3	I	Black	EN, on (SH-J1 removed is EN, on)		V_{BIAS}		V
J3	I	Green	V_{IN}, primary input voltage	5	12	20	V
J4:1-2	O	Green	Secondary VDD-to-COM	0		18	V
J4:2-3	O	Green	Secondary VEE-to-COM	-5		0	V
TP1	TP	Red	V_{IN}, positive probe point	5	12	20	V
TP2	TP	Black	GNDP, shared primary GND test point		0		V
TP3	TP	Black	GNDP, shared primary GND test point		0		V
TP4	TP	Yellow	/PG, power good test point		V_{BIAS}		V
TP5	TP	Yellow	EN, enable test point		V_{BIAS}		V
TP6	TP	Red	VEE, secondary VEE test point	-5		0	V
TP7	TP	Black	COM, secondary side reference		0		V
TP8	TP	Red	VDD, secondary VDD test point	0		18	V
TP9	TP	PCB	VEE-to-COM, secondary VDD scope probe point	-5		0	V
TP10	TP	PCB	VDD-to-COM, secondary VDD scope probe point	0		18	V
TP11	TP	PCB	V_{IN}-to-GNDP scope probe point	5	12	20	V

2.7 Oscilloscope Probes: Probing the EVM

Using TP9-11 oscilloscope probe PCB test points: The UCC35341-Q1 is a high frequency DC-DC module that requires careful measurement for accurately capturing transient events and measuring high frequency, AC ripple voltage. Remove the "witch hat" probe tip cover and ground lead from the scope probe. If scope probe ground springs are not available, wrap a piece of 22 AWG bare wire around the scope probe ground ring or use a fitted ground spring and insert the probe tip and ground into the EVM as shown in Figure 2-2.

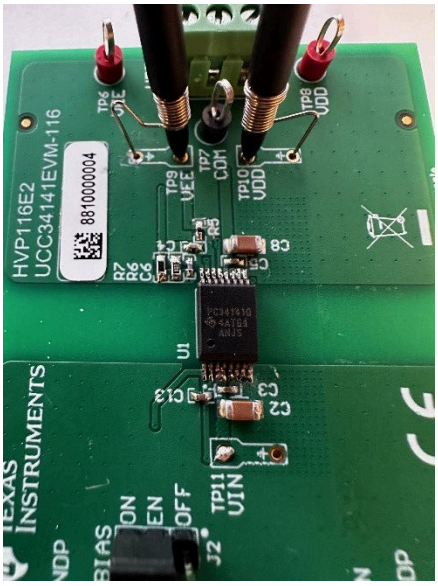


Figure 2-2. PCB Scope Probe Test Points

The EVM output nomenclature (VDD, VEE, COM) corresponds to what is commonly used when referring to isolated gate driver ICs. As shown in Figure 3-1, TP4 (COM) is the midpoint reference intended to connect to the COM pin of the isolated gate driver IC. When the UCC35341-Q1 is used to bias a gate driver IC, VDD (VDD-COM) and VEE (VEE-COM) are referred to with respect to COM.

3 Hardware Design Files

3.1 Schematics

Figure 3-1 shows the EVM electrical schematic. Upon receiving the EVM, U1 must be removed and replaced with UCC35341-Q1 and R1 must be removed and replaced with 4.99kΩ. The necessary component changes are summarized in Table 4 using recommended orderable part numbers shown in Table 5. R3-4 and C10-12 are intentionally unpopulated as indicated by a red X, placed directly over the component.

Table 3-1. EVM Component Changes to Evaluate UCC35341-Q1

Ref Des	Was	Now
U1	UCC34141-Q1	UCC35341-Q1
R1	10kΩ, 1%, 0402	4.99kΩ, 1%, 0402

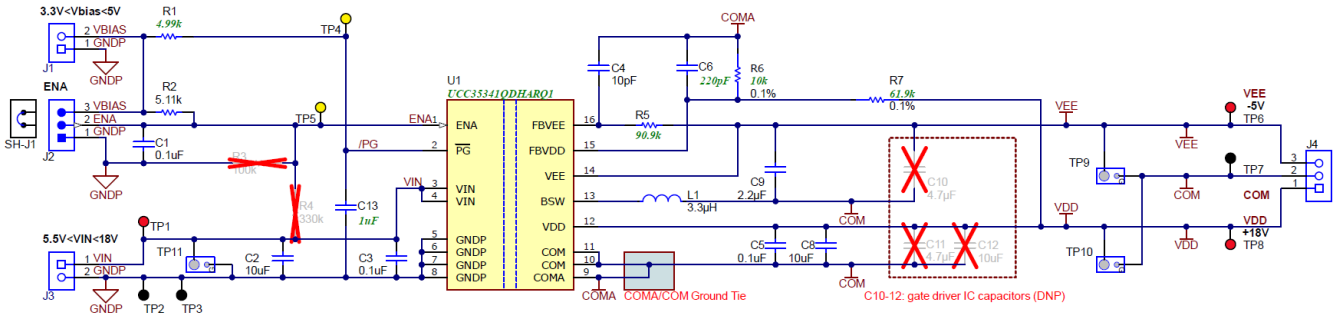


Figure 3-1. Schematic (UCC35341 Variant)

3.2 PCB Layouts

The UCC34141EVM-116 is designed using a four-layer, FR4, PCB, fabricated with 2-ounce copper on all four layers. The EVM, PCB demonstrates the important use of ground planes and tented stitching vias for shielding and improving EMI performance. For higher density PCBs such as automotive traction inverters, the PCB can include several additional signal layers but similar design methodology can be applied as best as possible.

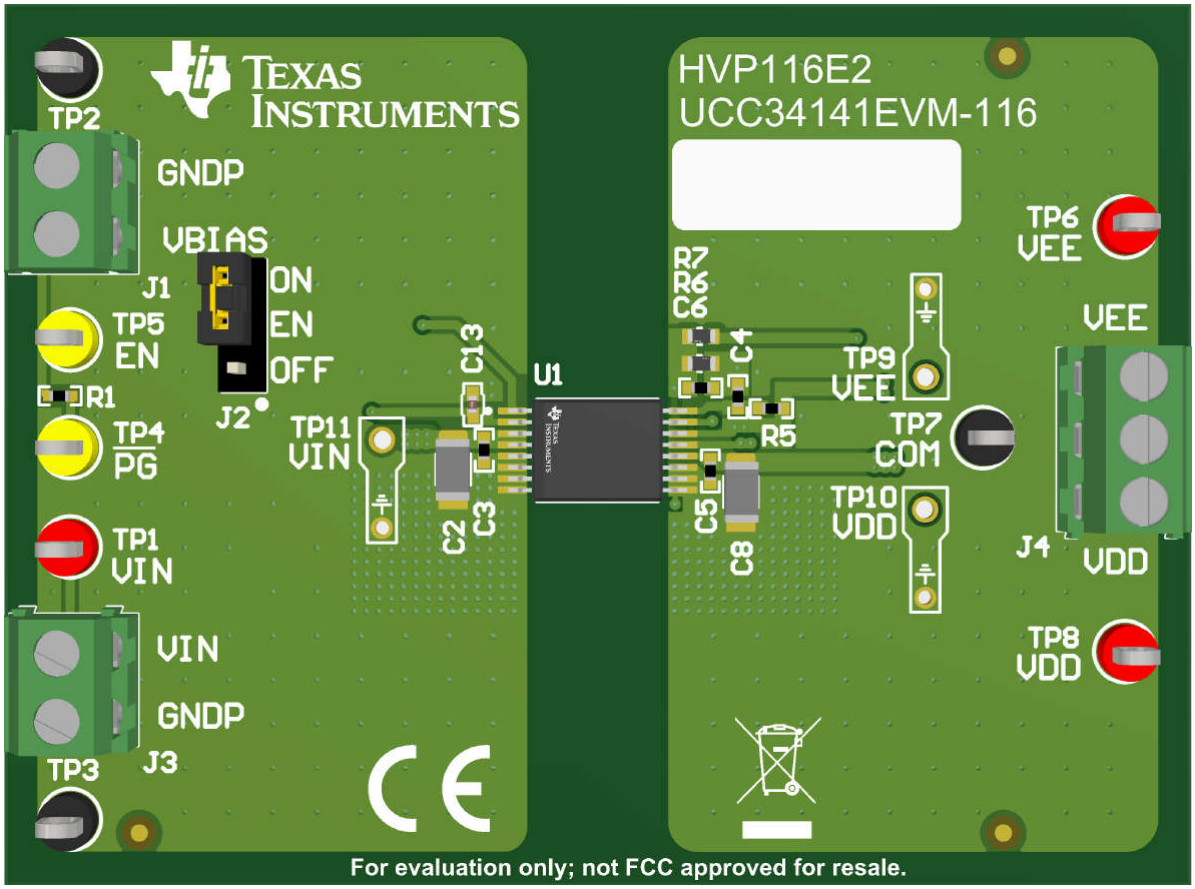


Figure 3-2. Fully Assembled 3D Top View

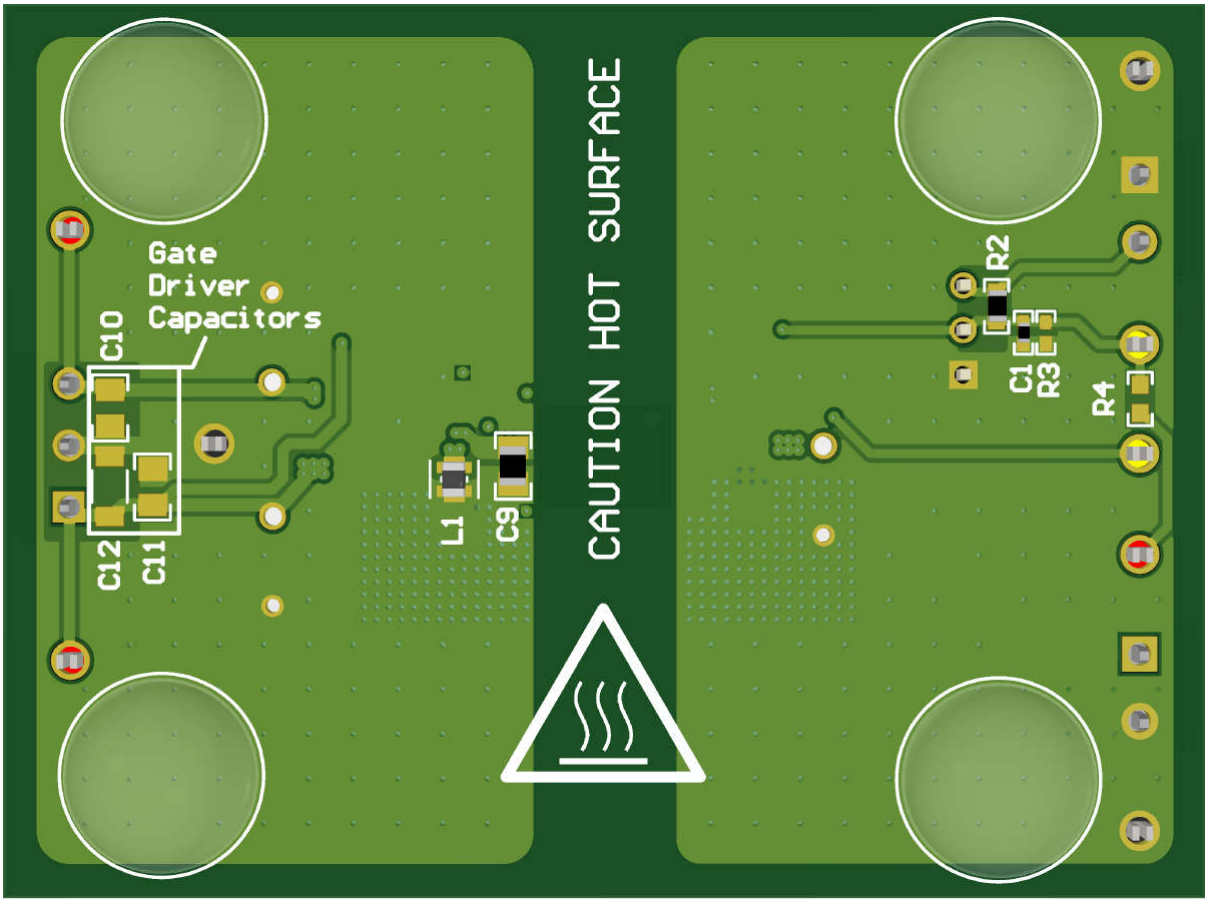


Figure 3-3. Fully Assembled 3D Bottom View

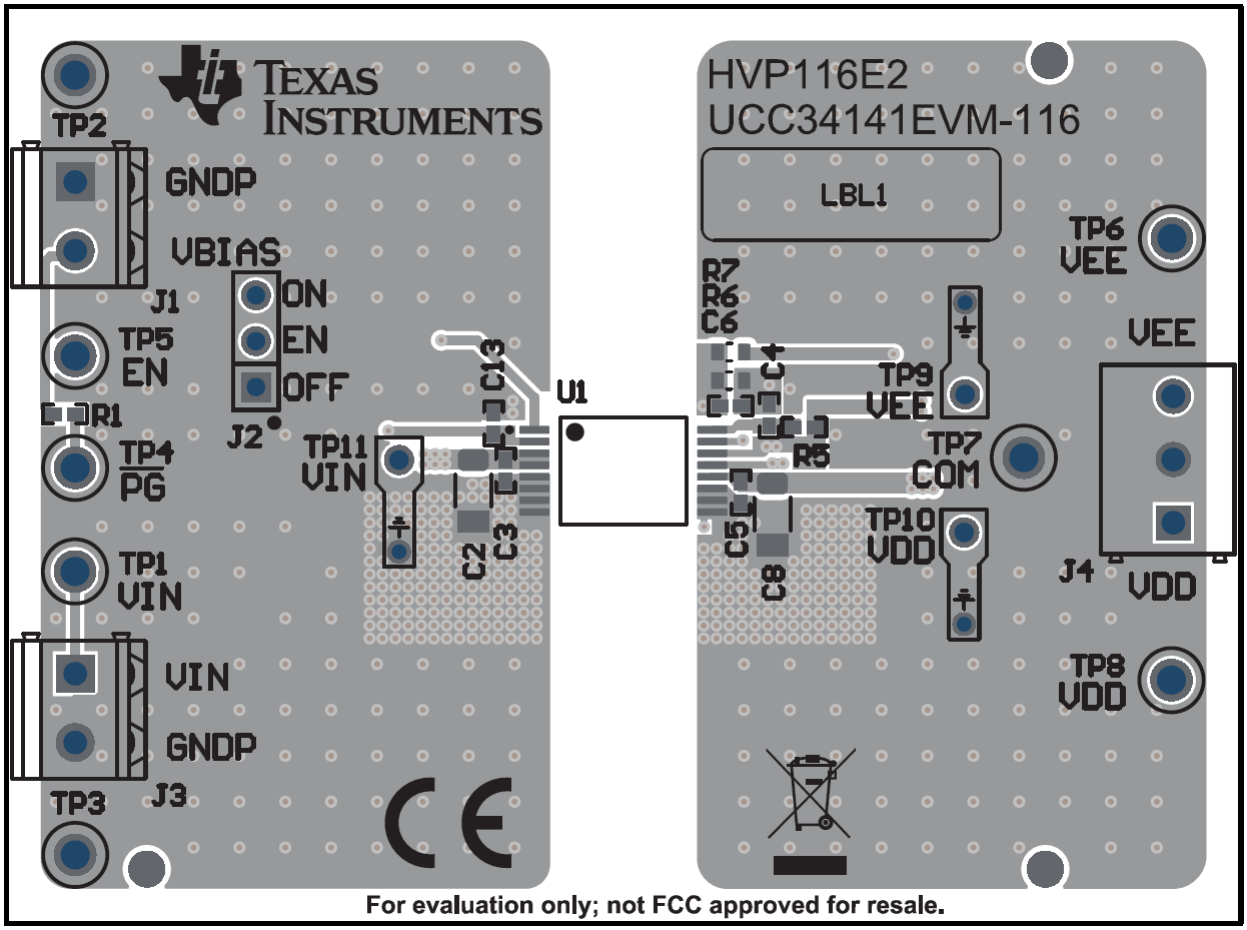


Figure 3-4. PCB Top Layer, Assembly

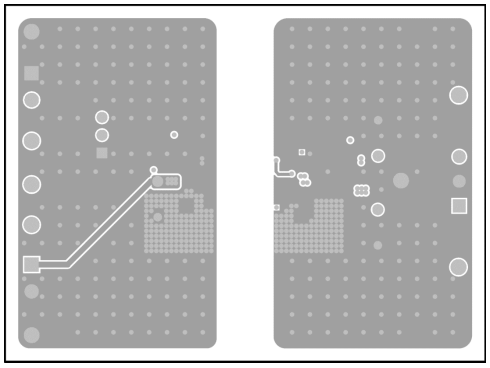


Figure 3-5. Ground Layer 2

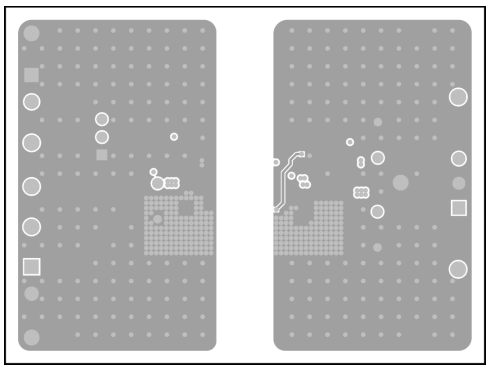


Figure 3-6. Ground Layer 3

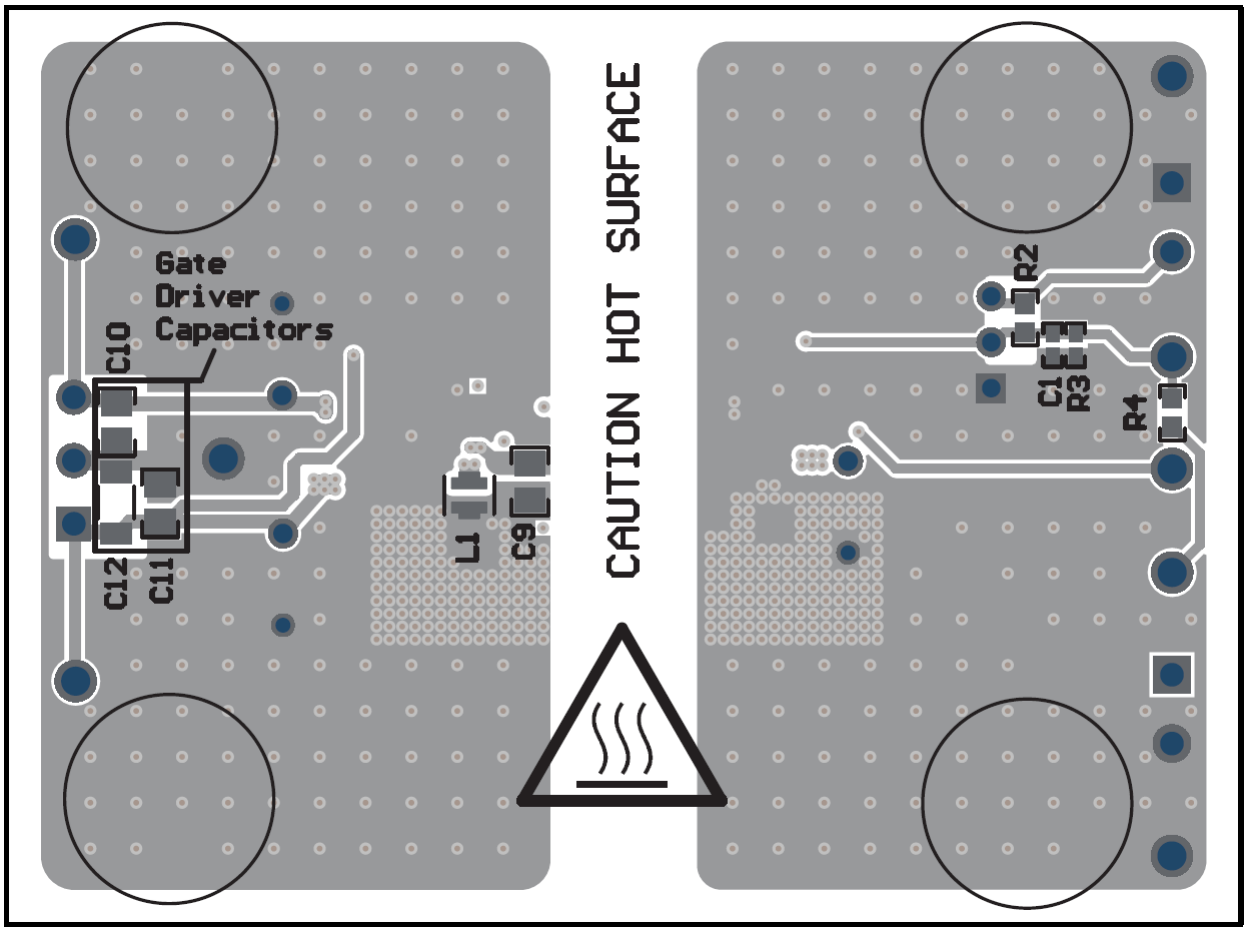


Figure 3-7. PCB Bottom Layer, Assembly (mirrored view)

3.3 PCB Layout Guidelines

The UCC35341-Q1 integrated isolated power solution simplifies system design and reduces board area usage. Follow these guidelines for proper PCB layout to achieve optimum performance. A minimum of 4-layer PCB layer stack using 2-ounce copper on external layers is recommended to accomplish a good thermal PCB design. It is not recommended to route signal tracks or place components directly beneath the UCC34141-Q1.

1. Input capacitors between VIN pin and GNDP pin:
   a. Place the 0.1µF high frequency bypass capacitor (C3) as close as possible to pins 3, 4 (VIN) and pins 5–8 (GNDP) and on the same side of the PCB as the IC. 0402 ceramic SMD or smaller is a desired size for optimal placement. The self-resonant frequency in a range between 10MHz to 30MHz is most ideal to offer low impedance decoupling for the switching frequency noise of the internal isolated convertor.

Do not place any vias between the bypass capacitor and the IC pins so as to force the high frequency current through the capacitor.

b. Place the bulk VIN capacitor(s) (C2) as close as possible and parallel to the 0.1µF high frequency bypass capacitor (C3) and on the same side of the PCB as the IC as shown in Figure 3-8.

2. /PG decoupling capacitor: The /PG decoupling capacitor should be placed close to pin 2 (/PG) and on the same side of the PCB as the UCC34141-Q1. Refer to C13 placement shown in Figure 3-8.
3. Output capacitors between VDD pin and COM pin:
   a. Place the 0.1µF high frequency bypass capacitor (C5) as close as possible to pin 12 (VDD) and pins 10, 11 (COM) and on the same side of the PCB as the IC. 0402 ceramic SMD or smaller is a desired size for optimal placement. The self-resonant frequency in a range between 10MHz to 30MHz is most ideal to offer low impedance decoupling for the switching frequency noise of the internal isolated convertor. Do not place any vias between the bypass capacitor and the IC pins so as to force the high frequency current through the capacitor.
   b. Place the bulk VDD-COM capacitor (C8) as close as possible and parallel to the 0.1µF high frequency bypass capacitor (C5) and on the same side of the PCB as the IC as shown in Figure 3-8.
4. Output capacitors between VEE pin and COM pin:
   a. Place the 2.2µF high frequency bypass capacitor (C9) as close as possible to VEE and COM pins. The self-resonant frequency in 3MHz to 4MHz is most ideal to offer low impedance decoupling for the switching frequency noise of the buck-boost converter with the 3.3uH inductor (L1) selection. It is possible to put the capacitor on the different side of PCB and use vias to connect, in order to reduce the switching loop between the capacitor and the internal low-side MOSFET of the VEE buck-boost converter. In addition, putting the capacitor on different side will also simplify the decoupling capacitor placement of VDD pin and COM pin. An example of bottom side PCB placement of C9 and L1 is shown in Figure 3-12.
5. Feedback:
   a. COMA should be isolated through all PCB layers, from the COM plane. Use one via to make a direct connection to the low-side resistor and filter capacitor from FBVDD pin, same as the low-side filter capacitor from FBVEE pin.
   b. Place the RFBVDD feedback resistors (R6 and R7) and the decoupling ceramic capacitor (C6) close to the IC.
   c. The top-side feedback resistor should be placed next to the low-side resistor with a short, direct connection between both resistors and single connection to FBVDD pin. The top connection to sense the regulated rail (VDD-COM) should be routed and connected at the VDD bias capacitor remote location near the gate driver pins for best accuracy and best transient response.
   d. The VEE feedback resistor (R5) should be placed with the decoupling ceramic capacitor (C4) next to FBVEE (pin 15); while the connection to sense the regulated rail (COM-VEE) should be routed and connected at the COM bias capacitor remote location near the gate driver pins for best accuracy and best transient response.
   e. When using the dual output mode, the buck-boost inductor (L1) and a 2.2uF decoupling ceramic capacitor (C9) must be populated. They can be place on the opposite side of the IC or on the same layer as IC.
   f. A layout example is shown in Figure 3-9, where L2 (yellow) is routed on layer 2 and L3 (green) is routed on layer 3.
6. Thermal vias: The UCC35341-Q1 internal transformer makes a direct connection to the lead frame. It is therefore critical to provide adequate space and proper heatsinking designed into the PCB as outlined in the steps below.
   a. TI recommends to connect the VIN, GNDP, VDD, and COM pins to internal ground or power planes through multiple vias. Alternatively, make the polygons connected to these pins as wide as possible.
   b. Use multiple thermal vias connecting PCB top side GNDP copper to bottom side GNDP copper. If possible, it is recommended to use 2-ounce copper on external top and bottom PCB layers.
   c. Use multiple thermal vias connecting PCB top side VEE copper to bottom side VEE copper. If possible, it is recommended to use 2-ounce copper on external top and bottom PCB layers.
   d. Thermal vias connecting top and bottom copper can also connect to internal copper layers for further improved heat extraction.

e. Thermal vias should be similar to pattern shown below but apply as many as the copper area will allow. TI recommends to use thermal via with 30mil diameter, 12mil hole size.
f. A layout example is shown in Figure 3-10. For cases where less copper area is available, use as many thermal vias as the design permits, placed close to pins 5-8 (primary) and 9-11 (secondary).

7. Creepage clearance: To maintain the full creepage, clearance and voltage isolation ratings specified in the data sheet, avoid routing signal traces or placing components directly under the UCC35341-Q1. Maintain the clearance width highlighted in red, throughout the entire defined isolation barrier. Keep-out clearance for basic isolation can be 50% less than the reinforced isolation requirement (8.2mm). Using 8.2mm provides additional margin. A layout example is shown in Figure 3-11.
8. Gate driver output capacitors: CVDD_GD (C11 and C12) and CVEE_GD (C10) are reference designators referred to in the UCC35341-Q1 Excel Calculator Tool. C11 and C12 are the capacitors between VDD-COM and C10 is the capacitor between COM-VEE. C10-12 are capacitors required by the gate driver IC.
   a. CVDD_GD and CVEE_GD should be placed next to the gate driver IC for best decoupling and gate driver switching performance.
   b. For optimal voltage regulation, the feedback trace from VEE (FBVEE) and VDD (FBVDD) should be as direct as possible so that the voltage feedback is being sensed directly at the VDD and VEE capacitors near the gate driver IC.

3.4 PCB Layout Example

The PCB layout example, highlighted in the following figures, is based on the EVM schematic shown in Figure 3-1 and PCB layer images shown in Figure 3-4 to Figure 3-7.

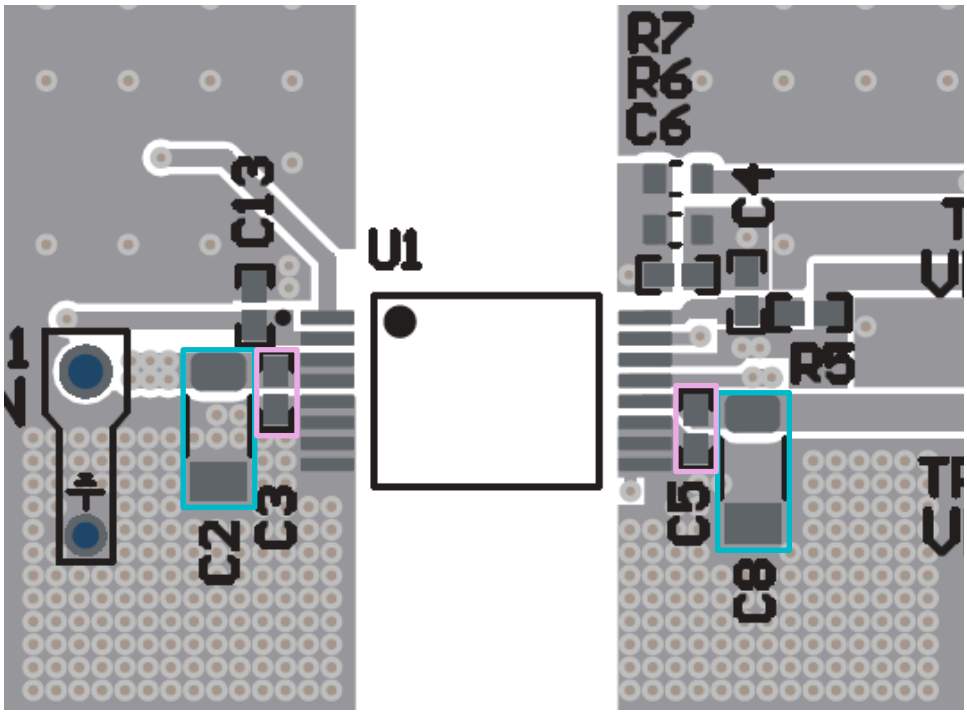


Figure 3-8. VIN (C2, C3) and VDD (C5, C8) Capacitors

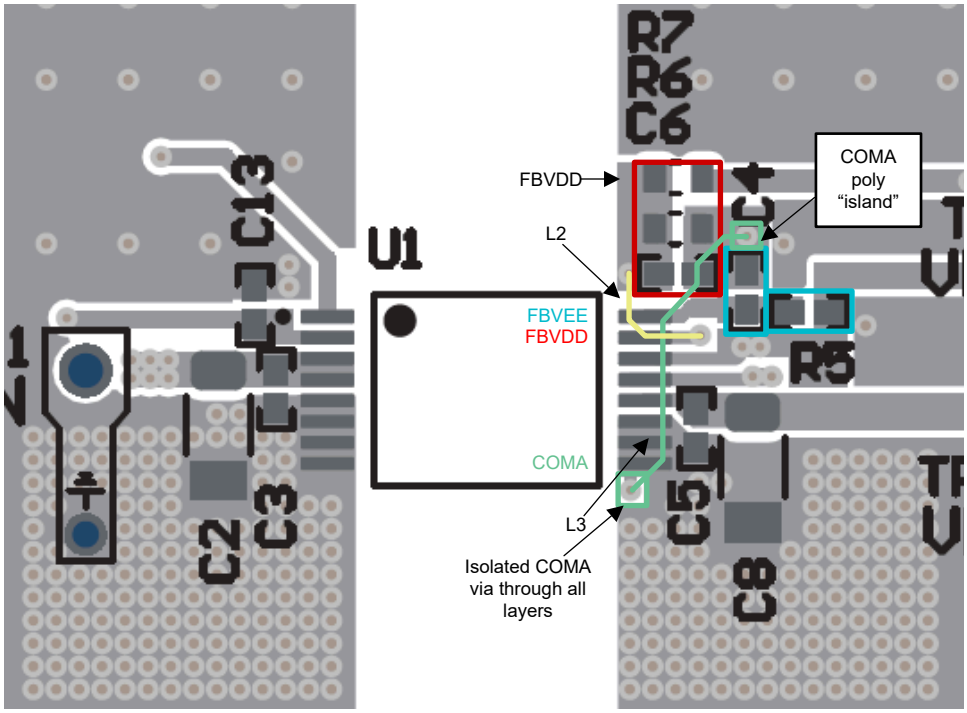


Figure 3-9. FBVDD (R6-7, C6), FBVEE (R5, C4), COMA Routing

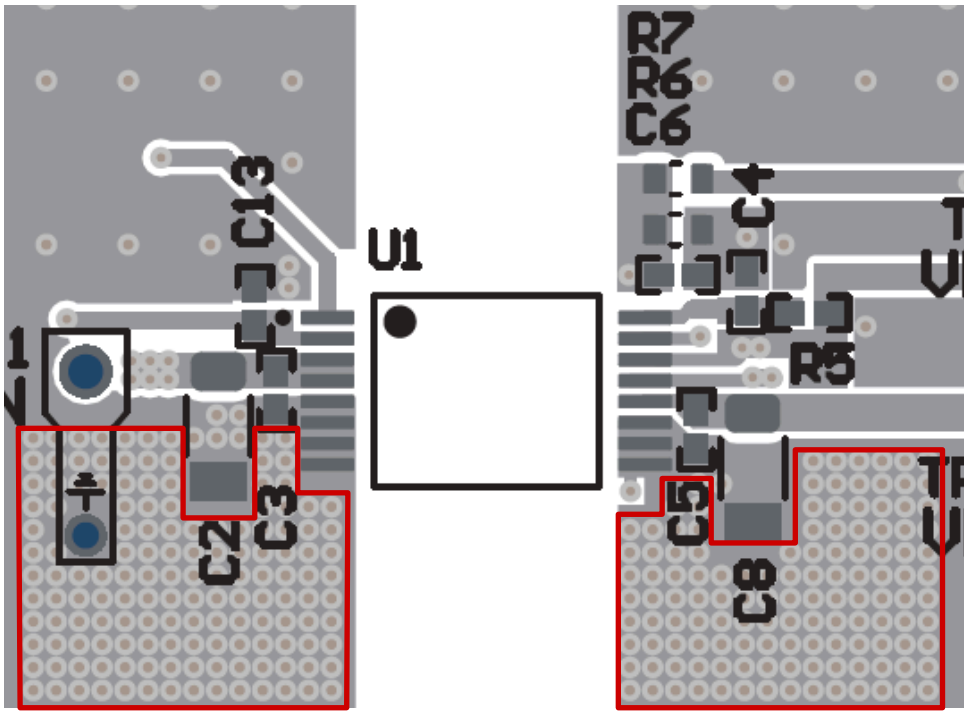


Figure 3-10. Thermal Vias

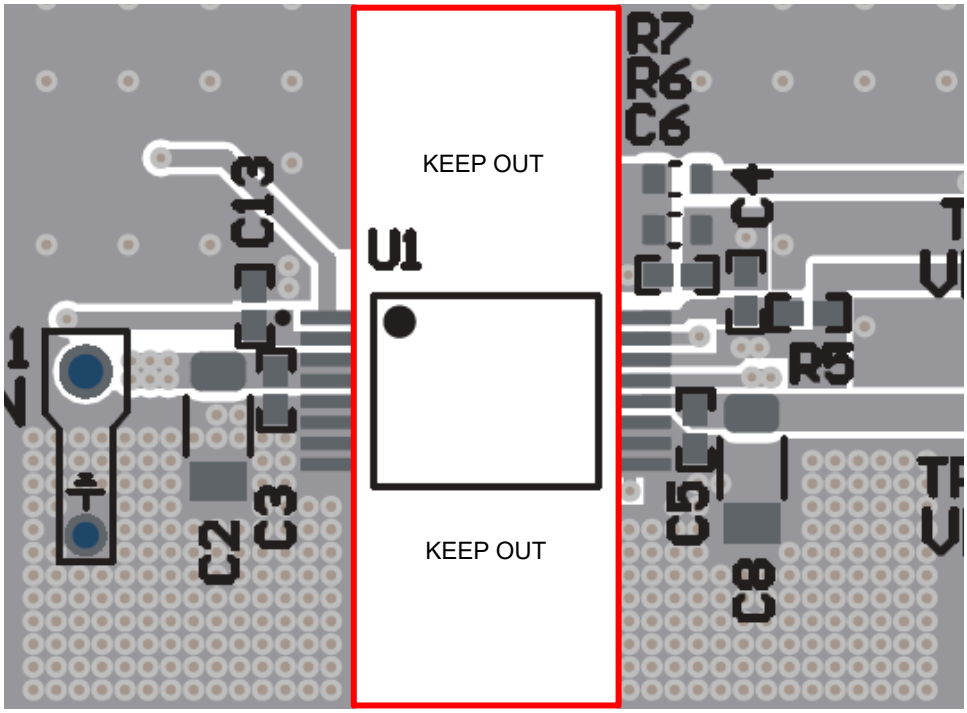


Figure 3-11. Isolation Keep Out Region

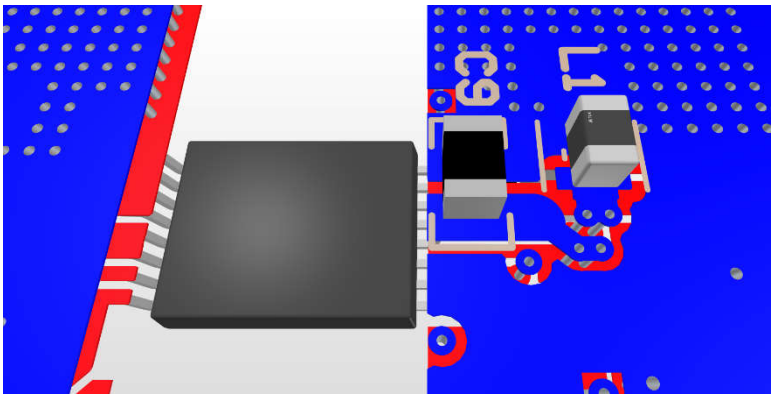


Figure 3-12. Bottom Side, Buck Boost, VEE LC Placement and Routing

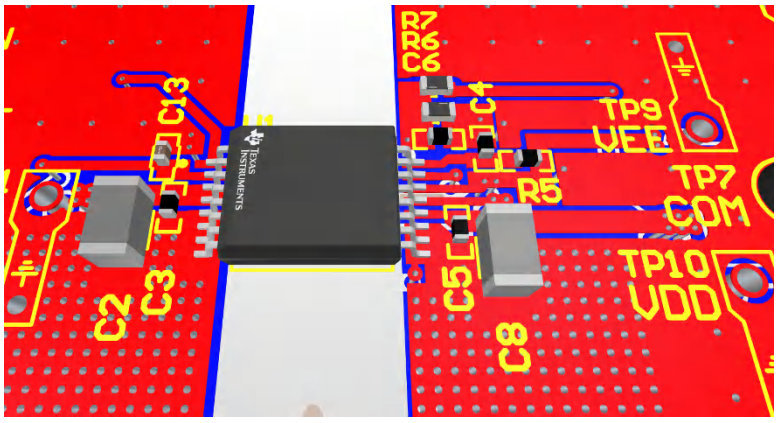


Figure 3-13. Top Side, Component Placement and Routing

3.5 Bill of Materials (BOM)

Table 3-2. Bill of Material (BOM)

Ref Des	Qty	Description	Part Number	Mfr
PCB1	1	Printed Circuit Board	HVP116	Any
C1, C3, C5	3	CAP, CERM, 0.1µF, 50V, ±10%, X7R, AEC-Q200 Grade 1, 0402	GCM155R71H104KE02D	MuRata
C2, C8	2	CAP, CERM, 10µF, 35V, ±10%, X7R, AEC-Q200 Grade 1, 1206_190	CGA5L1X7R1V106K160AC	TDK
C4	1	CAP, CERM, 10pF, 50V, ±5%, C0G/NP0, AEC-Q200 Grade 1, 0402	CGA2B2C0G1H100D050BA	TDK
C6	1	CAP, CERM, 220pF, 50V, ±5%, C0G/NP0, AEC-Q200 Grade 1, 0402	CGA2B2C0G1H221J050BA	TDK
C9	1	CAP, CERM, 2.2µF, 16V, ±10%, X7R, 0805	C2012X7R1C225K125AB	TDK
C13	1	1µF ±20% 10V Ceramic Capacitor X7R 0402 (1005 Metric)	KAM05CR71A105MH	KYOCERA AVX
H1, H2, H3, H4	4	Bumpon, Hemisphere, 0.44 X 0.20, Clear	SJ-5303 (CLEAR)	3M
J1, J3	2	Terminal Block, 2x1, 3.81mm, 24-16 AWG, 10A, 300VAC, TH	691214310002	Wurth Elektronik
J2	1	Header, 100mil, 3x1, Tin, TH	PEC03SAAN	Sullins
J4	1	Terminal Block, 3.5mm, 3x1, Tin, TH	691214110003	Wurth Elektronik
L1	1	Shielded Inductor 3.3µH ±20% 500mA 260mΩ AEC-Q200 SMD 0805	MLZ2012M3R3HTD25	TDK
R1	1	RES, 4.99k, 1%, 0.1W, AEC-Q200 Grade 0, 0402	ERJ-2RKF4991X	Panasonic
R2	1	RES, 5.11kΩ, 1%, 0.1W, AEC-Q200 Grade 0, 0603	CRCW06035K11FKEA	Vishay-Dale
R5	1	RES, 90.9kΩ, 1%, 0.063W, AEC-Q200 Grade 0, 0402	CRCW040290K9FKED	Vishay-Dale
R6	1	10kΩ. ±0.1% 0.1W, Chip Resistor 0603 Automotive AEC-Q200 Thin Film	ERA-3AEB103V	Panasonic
R7	1	61.9kΩ, ±0.1% 0.1W, Chip Resistor 0603 Automotive AEC-Q200 Thin Film	ERA-3AEB6192V	Panasonic
SH-J1	1	Shunt, 100mil, Gold plated, Black	SNT-100-BK-G	Samtec
TP1, TP6, TP8	3	Test Point, Multipurpose, Red, TH	5010	Keystone Electronics
TP2, TP3, TP7	3	Test Point, Multipurpose, Black, TH	5011	Keystone Electronics
TP4, TP5	2	Test Point, Multipurpose, Yellow, TH	5014	Keystone Electronics
U1	1	Automotive 2W, 12V-Vin, 25V-Vout, High Efficiency, High-Density, >5kV$_{RMS}$, Isolated DC-DC Module	UCC35341QDHARQ1	Texas Instruments
U1 - ALT	0	Automotive 1.5W, 12V-Vin, 25V-Vout, High Efficiency, High-Density, >5kV$_{RMS}$, Isolated DC-DC Module	UCC34141QDHARQ1	Texas Instruments
C10, C11	0	CAP, CERM, 4.7µF, 35V, ±10%, X7R, AEC-Q200 Grade 1, 0805	CGA4J1X7R1V475K125AC	TDK
C12	0	CAP, CERM, 10µF, 35V, ±10%, X7R, AEC-Q200 Grade 1, 1206_190	CGA5L1X7R1V106K160AC	TDK
R3	0	RES, 100kΩ, 5%, 0.1 W, AEC-Q200 Grade 0, 0402	ERJ-2GEJ104X	Panasonic
R4	0	RES, 330kΩ, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	ERJ-3EKF3303V	Panasonic

4 Additional Information

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NOTE:

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3 *Regulatory Notices:*

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3.1.1 *Notice applicable to EVMs not FCC-Approved:*

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3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

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- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247*

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

3.3 *Japan*

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https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-delivered-in-japan.html

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If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

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2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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