EVM User's Guide: ISO64XX-WB-EVM

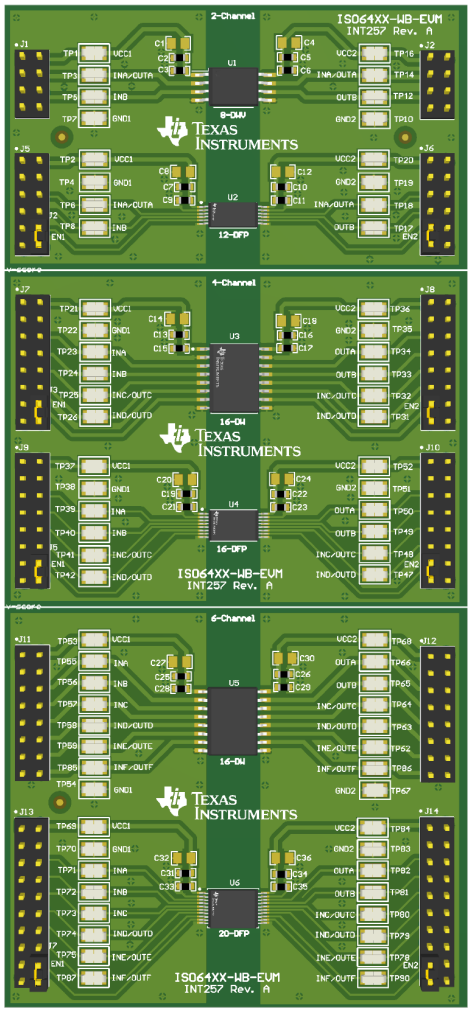
ISO64XX Wide-body Digital Isolator Evaluation Module

Description

The ISO64xx wide-body package evaluation module (EVM) allows designers to evaluate device performance for fast development and analysis of isolated systems. The EVM supports evaluation of any of the ISO64XX single-channel, dual-channel, quad-channel, or six-channels digital isolator devices in various wide-body packages: 8-pin WB SOIC (DWV), 12-pin WB SOIC (DFP), 16-pin WB SOIC (DW), 16-pin WB SOIC (DFP), and 20-pin WB SOIC (DFP).

Features

- Platform for complete evaluation of ISO64XX device family.
- Break-away design allows for easy separation of board footprints
- Test points and jumper options
- Passives and footprints for basic modifications included
- Robust isolation barrier



ISO64XX-WB-EVM

1 Introduction

This user's guide describes the ISO64XX Wide-body Package Evaluation Module (EVM). This EVM lets designers evaluate device performance for fast development and analysis of isolated systems. The EVM supports evaluation of any of the ISO64XX single-channel, dual-channel, quad-channel, or six-channels digital isolator devices in various wide-body packages: 8-pin WB SOIC (DWV), 12-pin WB SOIC (DFP), 16-pin WB SOIC (DW), 16-pin WB SOIC (DFP), and 20-pin WB SOIC (DFP). This guide also describes the standard pin configurations of devices for each package, bill of materials, EVM schematic, PCB layout, and typical laboratory test setup. A typical input and output waveform is also presented.

2 Pin Configurations of Digital Isolators in Different Packages

The ISO64XX-WB-EVM has provision for multiple device footprints that are unoccupied to allow for testing of various ISO64XX devices. Figure 2-1 through Figure 2-15 show all possible device pin configurations of digital isolators with different channel options in different packages that can be tested on this EVM. The figures also provide reference to device footprint designators (like U1) of the EVM where a given digital isolator for a given channel option in a given package can be tested on the EVM. Table 2-1 can be used as a quick reference table to identify the device footprint designator where a digital isolator can be tested for a given channel and package options.

Table 2-1. Digital Isolator Channel and Package Options and The Respective Footprint Locations

Number of Channels	Digital Isolator Part Numbers That can be Tested	Example Part Number	Package	Testing Location
2	ISO642x	ISO6421	DWV-8	U1
			DFP-12	U2
4	ISO644x	ISO6441	DW-16	U3
			DFP-16	U4
6	ISO646x	ISO6462	DW-16	U5
			DFP-20	U6

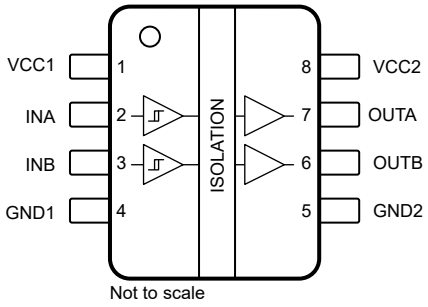


Figure 2-1. Dual-Channel (ISO6420) Digital Isolator Pin Configuration for DWV-8 Package on U1

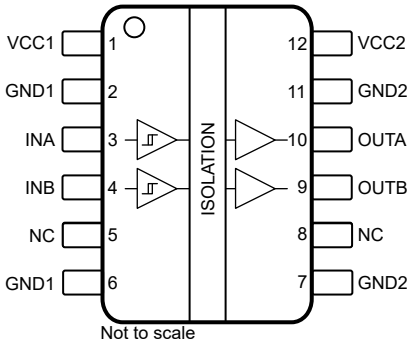


Figure 2-2. Dual-Channel (ISO6420) Digital Isolator Pin Configuration for DFP-12 Package on U2

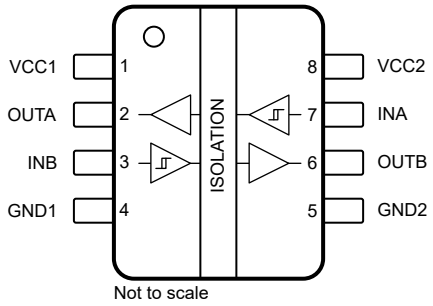


Figure 2-3. Dual-Channel (ISO6421) Digital Isolator Pin Configuration for DWV-8 Package on U1

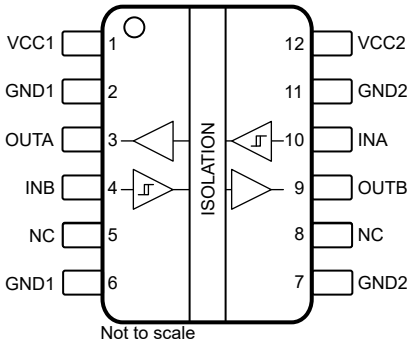


Figure 2-4. Dual-Channel (ISO6421) Digital Isolator Pin Configuration for DFP-12 Package on U2

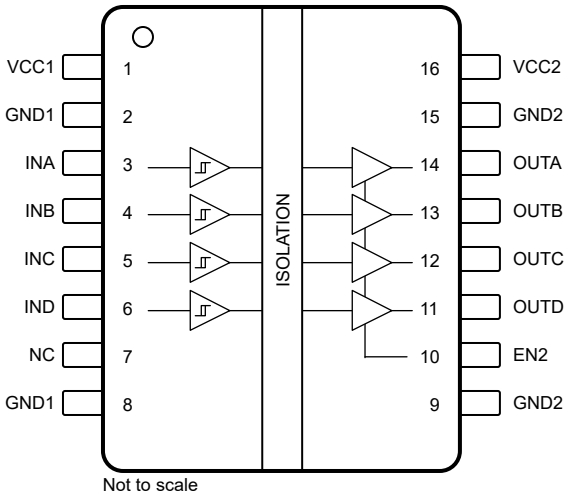


Figure 2-5. Quad-Channel (ISO6440) Digital Isolator Pin Configuration for DW-16 Package on U3 and DFP-16 Package on U4

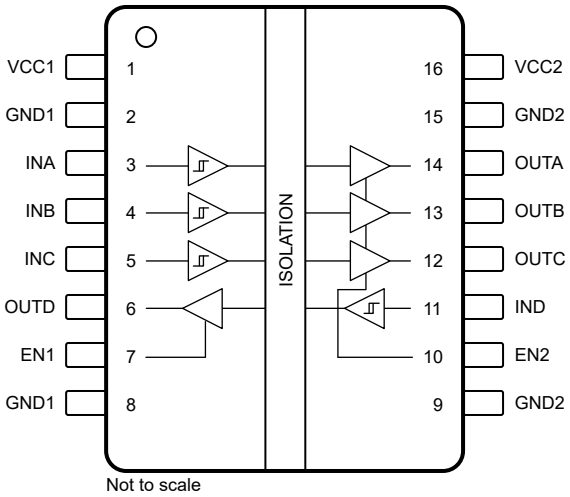


Figure 2-6. Quad-Channel (ISO6441) Digital Isolator Pin Configuration for DW-16 Package on U3 and DFP-16 Package on U4

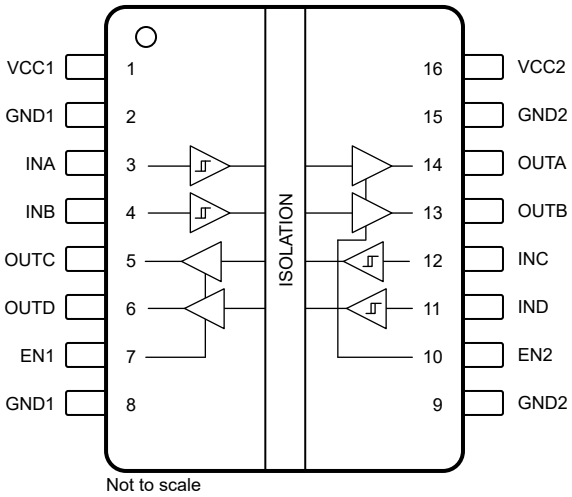


Figure 2-7. Quad-Channel (ISO6442) Digital Isolator Pin Configuration for DW-16 Package on U3 and DFP-16 Package on U4

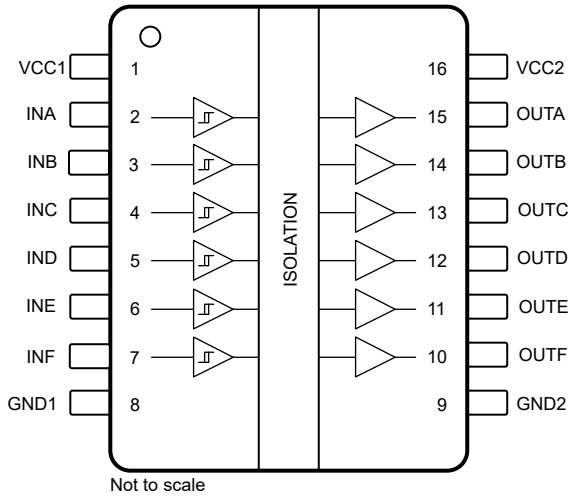


Figure 2-8. Six-Channel (ISO6460) Digital Isolator Pin Configuration for DW-16 Package on U5

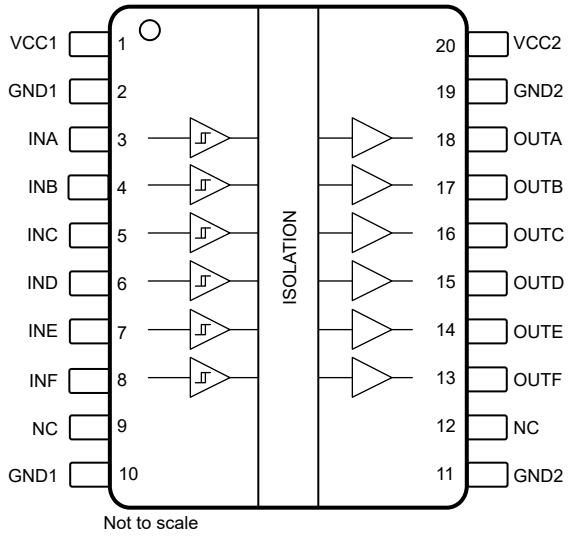


Figure 2-9. Six-Channel (ISO6460) Digital Isolator Pin Configuration for DFP-20 Package on U6

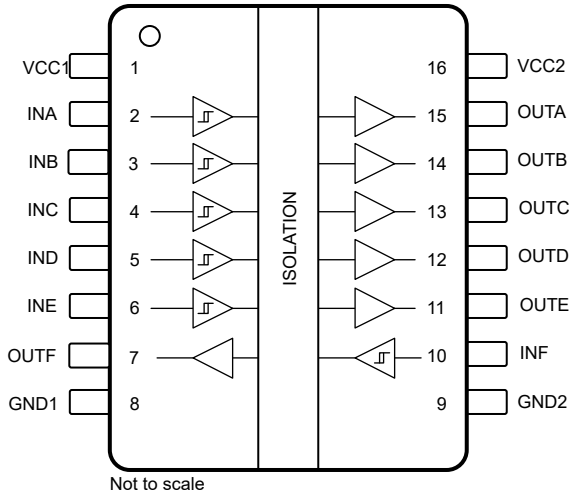


Figure 2-10. Six-Channel (ISO6461) Digital Isolator Pin Configuration for DW-16 Package on U5

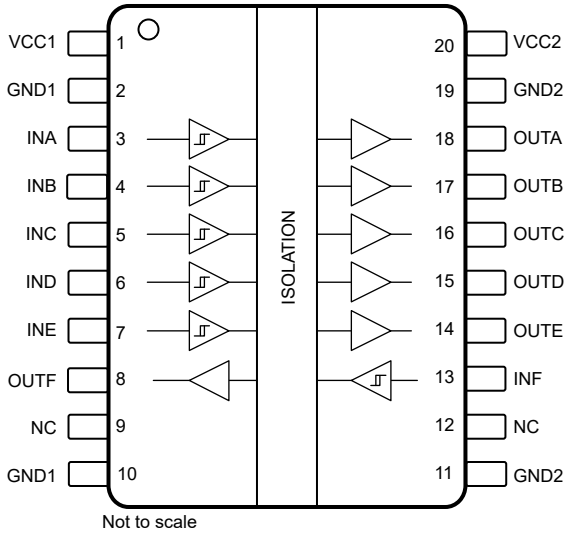


Figure 2-11. Six-Channel (ISO6461) Digital Isolator Pin Configuration for DFP-20 Package on U6

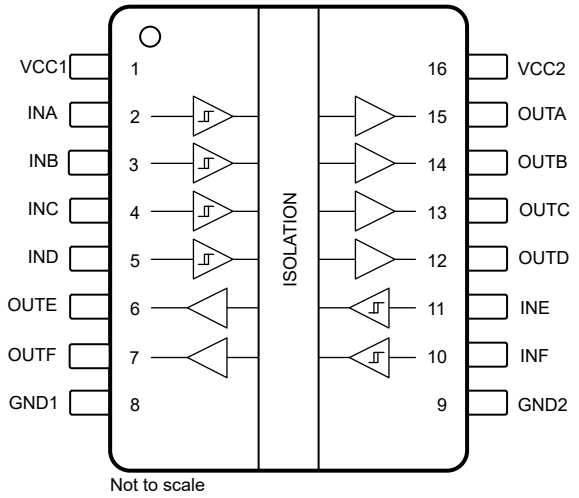


Figure 2-12. Six-Channel (ISO6462) Digital Isolator Pin Configuration for DW-16 Package on U5

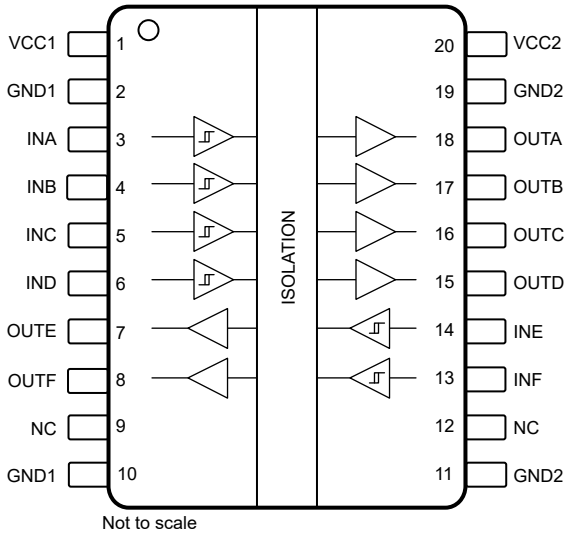


Figure 2-13. Six-Channel (ISO6462) Digital Isolator Pin Configuration for DFP-20 Package on U5

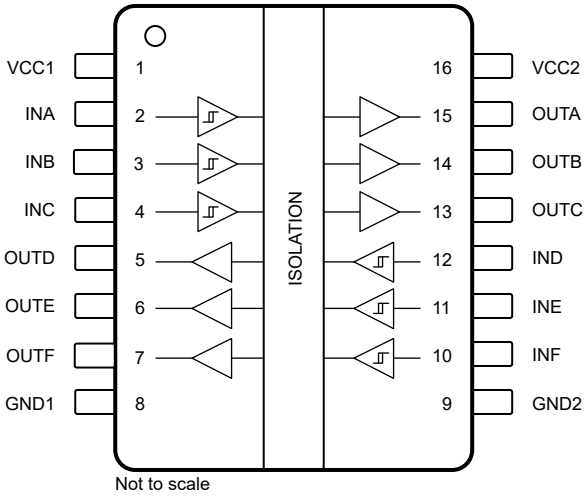


Figure 2-14. Six-Channel (ISO6463) Digital Isolator Pin Configuration for DW-16 Package on U5

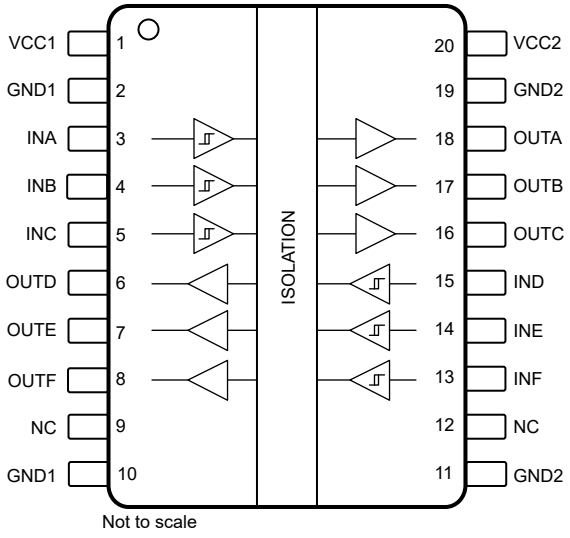


Figure 2-15. Six-Channel (ISO6463) Digital Isolator Pin Configuration for DFP-20 Package on U6

3 EVM Setup and Operation

This section describes the setup and operation of the EVM for parameter performance evaluation. Figure 3-1 shows the configuration for operating the ISO64XX-WB-EVM for one device footprint using two power supplies.

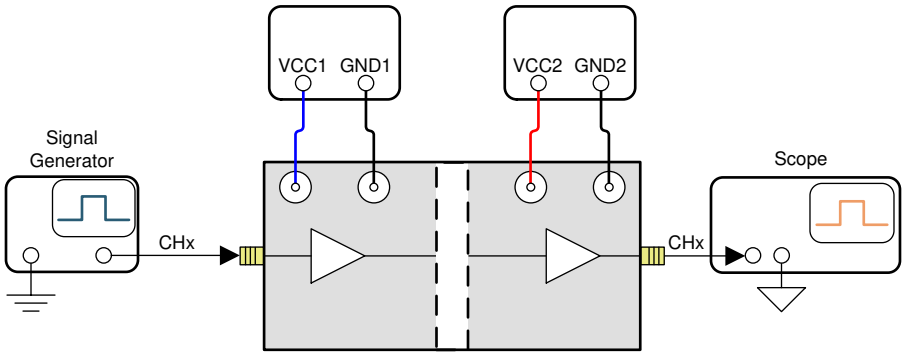


Figure 3-1. Basic EVM Operation

Figure 3-2 shows typical input and output waveforms of the EVM for a 1MHz clock. The input is shown as channel 1, and the output is shown as channel 2.

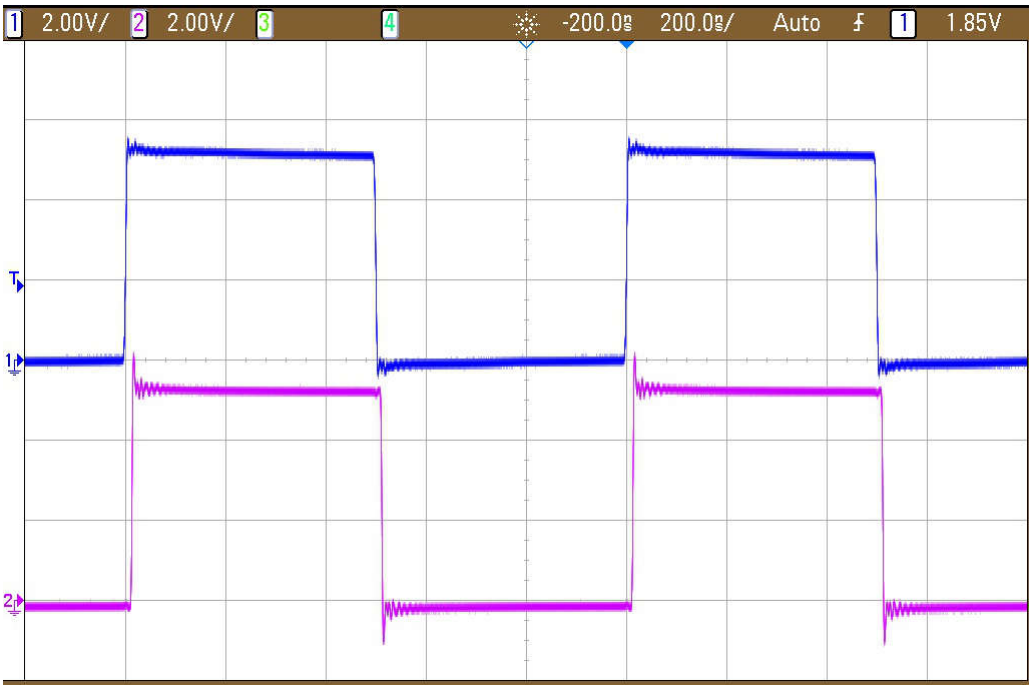
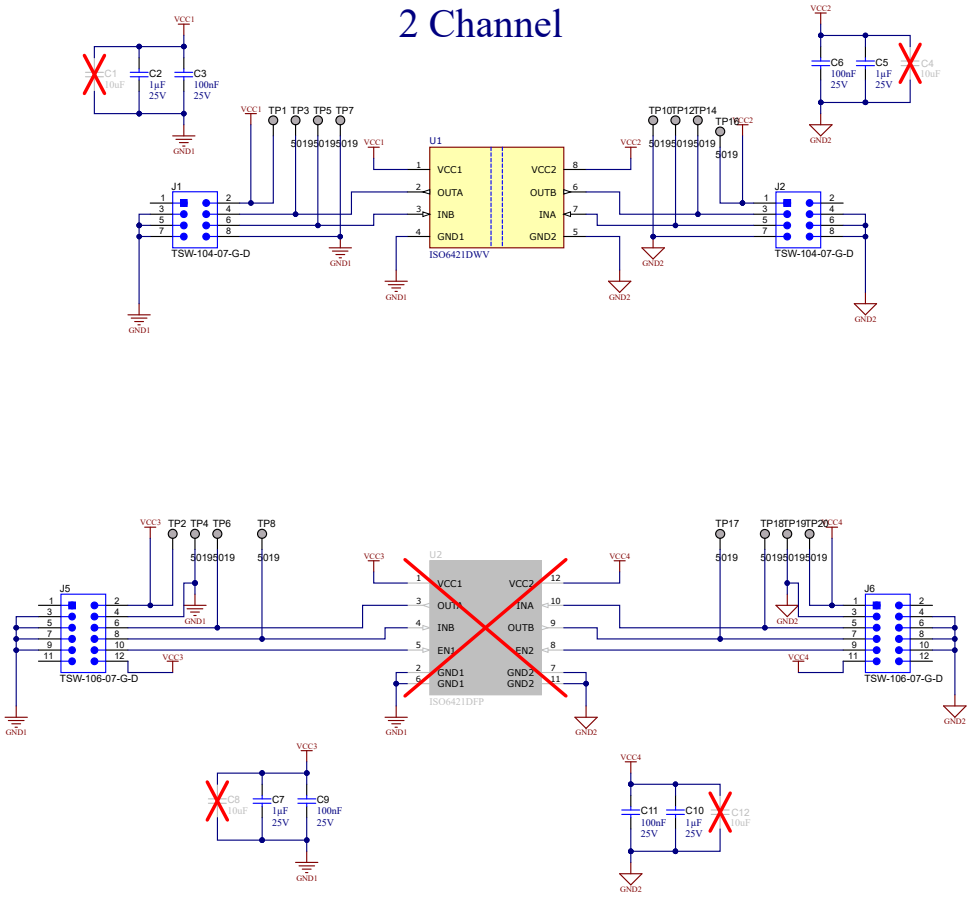


Figure 3-2. Typical Input and Output Waveform

4 EVM Schematic and PCB Layout

The ISO64XX widebody EVM is designed to accommodate various ISO64XX digital isolators with different channel options and packages. To evaluate any of the digital isolator devices in a given package, populate the device of interest on the ISO64XX-WB-EVM PCB according to the footprint positions suggested in section 2. No other component requires any modification on the EVM. Figure 4-1 shows the ISO64XX-WB-EVM schematic. Figure 4-2 and Figure 4-3 show the printed-circuit board (PCB) layout of the EVM.



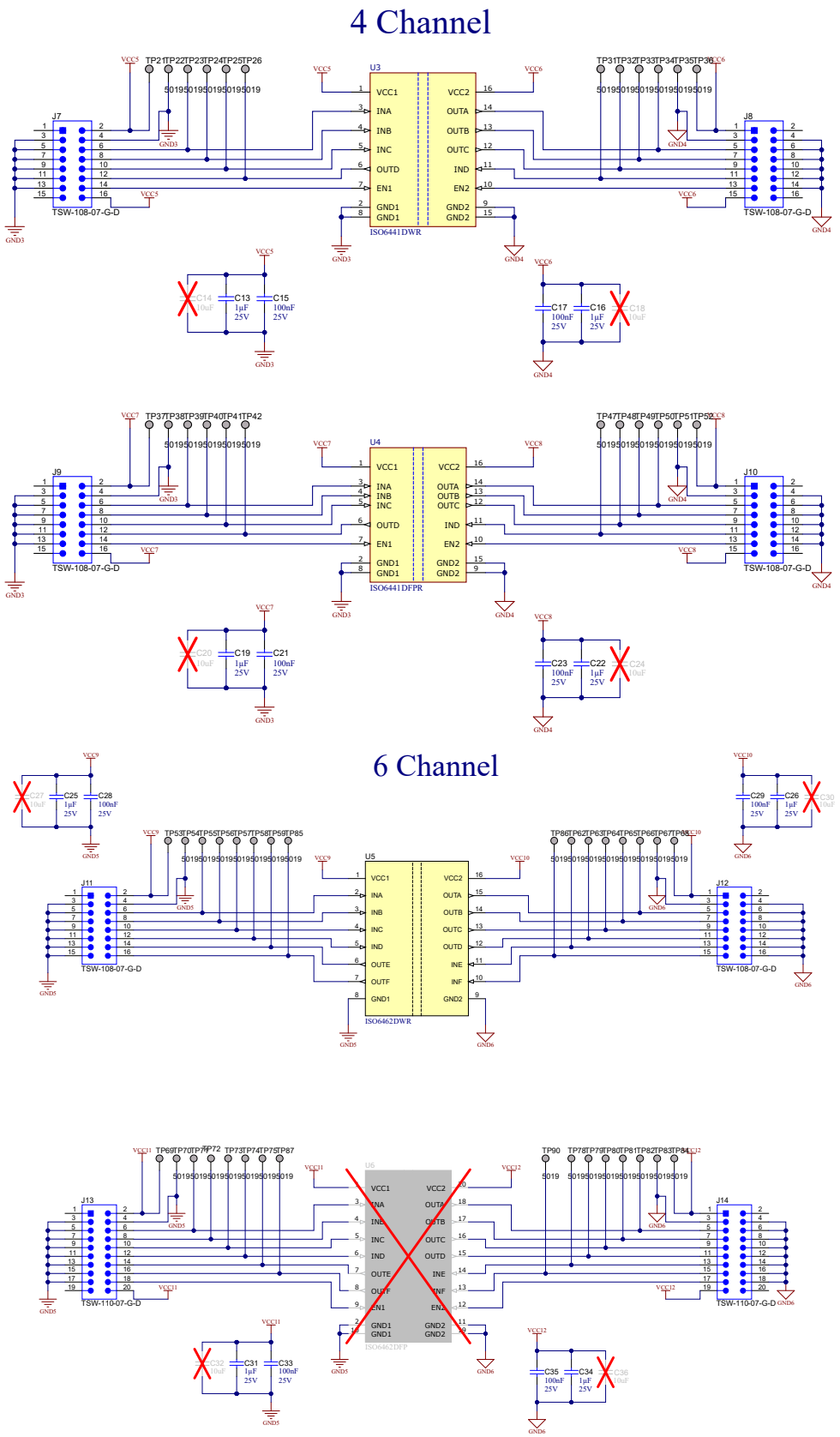


Figure 4-1. ISO64XX-WB-EVM Schematic

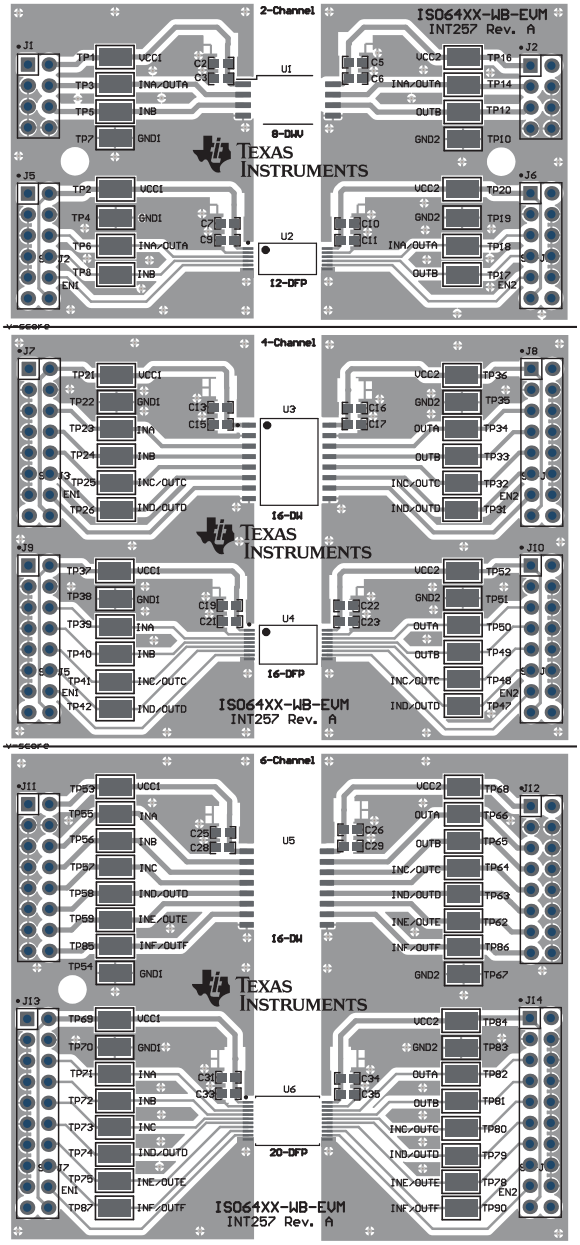


Figure 4-2. ISO64XX-WB-EVM PCB Layout - Top Layer

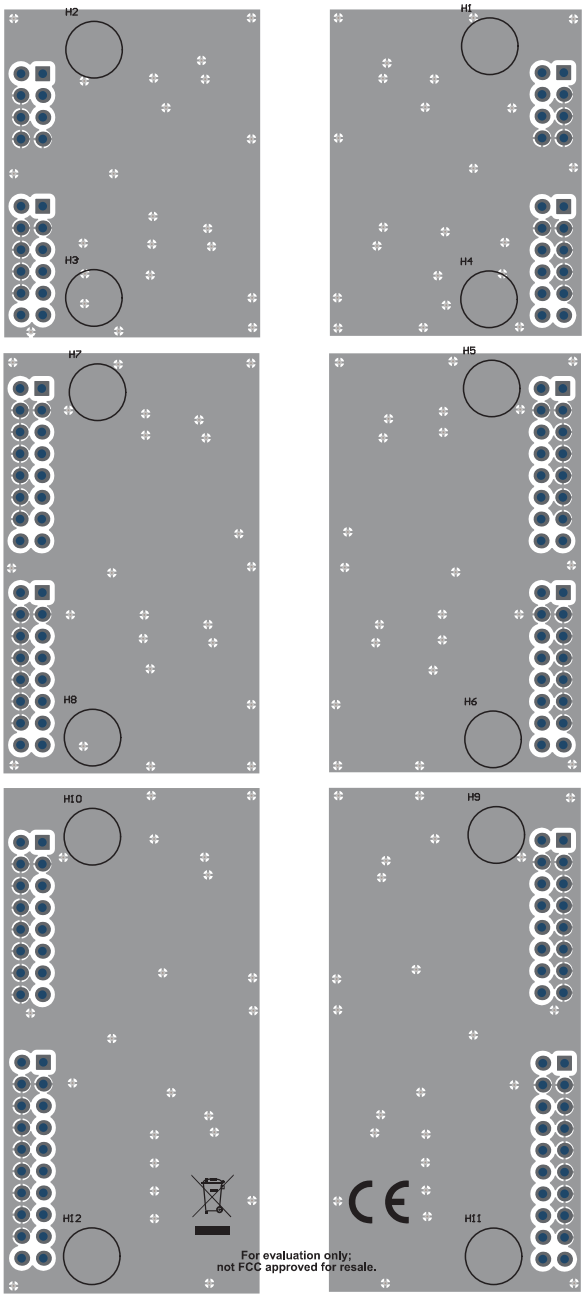


Figure 4-3. ISO64XX-WB-EVM PCB Layout - Bottom Layer

5 ISO64XX-WB-EVM Image

Figure 5-1 shows the 3D diagram of the EVM.

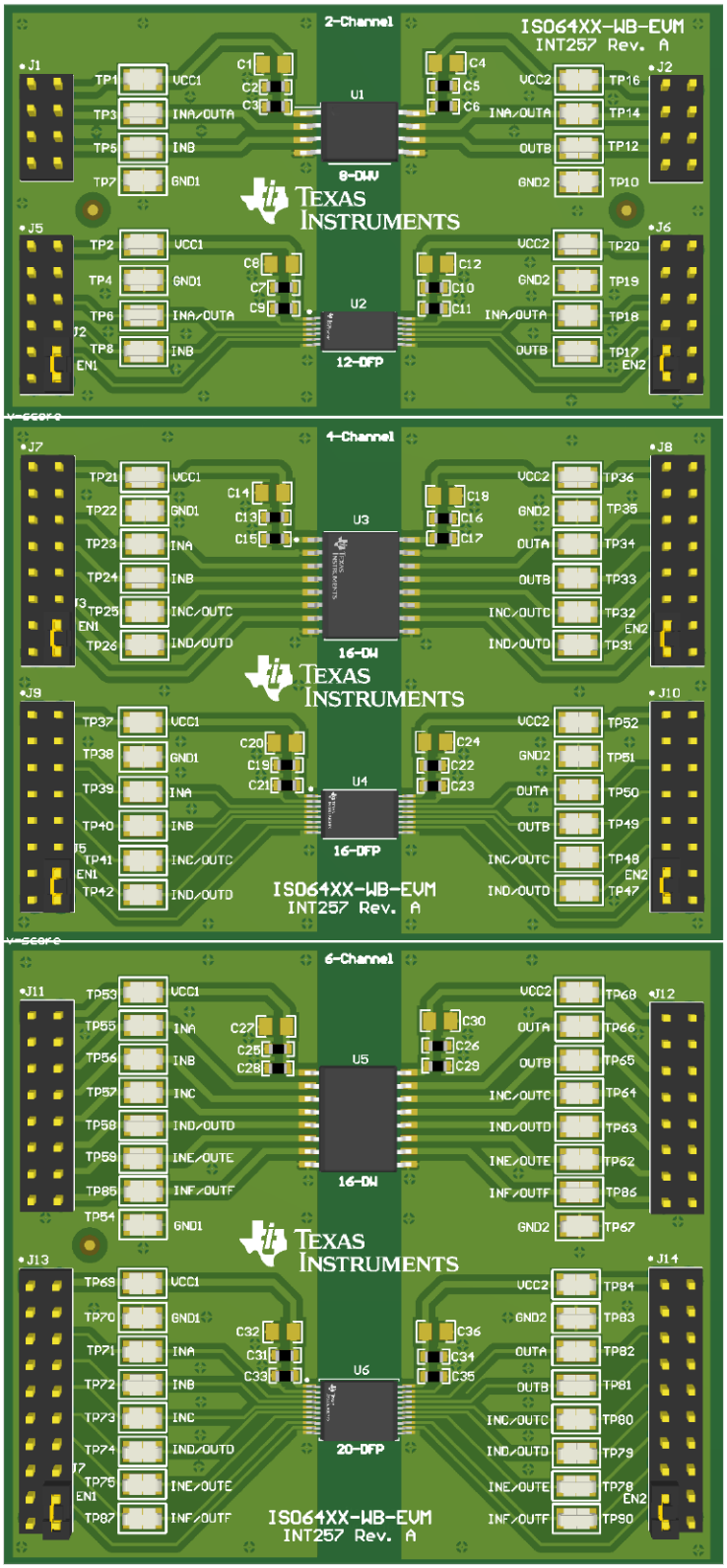


Figure 5-1. ISO64XX-WB-EVM 3D Diagram

6 Bill of Materials

Table 6-1 shows the bill of materials (BOM) for this EVM.

Table 6-1. Bill of Materials

Item	Designator	Description	Manufacturer	Part Number	Quantity
1	C2, C5, C7, C10, C13, C16, C19, C22, C25, C26, C31, C34	CAP, CERM, 1 uF, 25 V, +/- 10%, X7R, 0603	Kemet	C0603C105K3RACTU	12
2	C3, C6, C9, C11, C15, C17, C21, C23, C28, C29, C33, C35	CAP, CERM, 0.1 uF, 25 V, +/- 5%, X7R, 0603	Kemet	C0603C104J3RACTU	12
3	H1, H2, H3, H4	Bumpon, Hemisphere, 0.44 X 0.20, Clear	3M	SJ-5303 (CLEAR)	4
4	J1, J2, J3, J4	Header, 100mil, 6x2, Gold, TH	TE Connectivity	87227-6	4
3	C1, C4, C8, C12, C14, C18, C20, C24, C27, C30, C32, C36	CAP, CERM, 10 uF, 35 V, +/- 10%, X5R, 0805	MuRata	GRM21BR6YA106KE43L	12
4	H1, H2, H3, H4, H5, H6, H7, H8, H9, H10, H11, H12	Bumpon, Hemisphere, 0.25 X 0.075, Clear	3M	SJ5382	12
5	J1, J2	Header, 100mil, 4x2, Gold, TH	Samtec	TSW-104-07-G-D	2
6	J5, J6	Header, 100mil, 6x2, Gold, TH	Samtec	TSW-106-07-G-D	2
7	J7, J8, J9, J10, J11, J12	Header, 100mil, 8x2, Gold, TH	Samtec	TSW-108-07-G-D	6
8	J13, J14	Header, 100mil, 10x2, Gold, TH	Samtec	TSW-110-07-G-D	2
9	LBL1	Thermal Transfer Printable Labels, 0.650" W x 0.200" H - 10,000 per roll	Brady	THT-14-423-10	1
10	SH-J1, SH-J2, SH-J3, SH-J4, SH-J5, SH-J6, SH-J7, SH-J8	Shunt, 100mil, Gold plated, Black	Samtec	SNT-100-BK-G	8
11	TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP10, TP12, TP14, TP16, TP17, TP18, TP19, TP20, TP21, TP22, TP23, TP24, TP25, TP26, TP31, TP32, TP33, TP34, TP35, TP36, TP37, TP38, TP39, TP40, TP41, TP42, TP47, TP48, TP49, TP50, TP51, TP52, TP53, TP54, TP55, TP56, TP57, TP58, TP59, TP62, TP63, TP64, TP65, TP66, TP67, TP68, TP69, TP70, TP71, TP72, TP73, TP74, TP75, TP78, TP79, TP80, TP81, TP82, TP83, TP84, TP85, TP86, TP87, TP90	Test Point, Miniature, SMT	Keystone	5019	72
12	U1	ISO6421DWV	Texas Instruments	ISO6421DWVR	1
13	U2	ISO6421DFP	Texas Instruments	ISO6421DFPR	1
14	U3	ISO6441DW	Texas Instruments	ISO6441DWR	1
15	U4	ISO6441DFP	Texas Instruments	ISO6441DFPR	1
16	U5	ISO6462DW	Texas Instruments	ISO6462DWR	1
17	U6	ISO6462DFP	Texas Instruments	ISO6462DFPR	1

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale, TI’s General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Last updated 10/2025