Designing with the Voice-Band Audio Processor

APPLICATION REPORT: SLWA001B

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Abstract

Voice-Band Audio Processors (VBAP™) provide a full-duplex interface between voice/audio signals and a DSP. This document provides a detailed discussion of the features and operation of VBAPs. Topics discussed include VBAP functions, operating modes, gain analysis, and application design. A design for a VBAP System Evaluation Board (SEB) is also provided. Specific interface examples to a Digital Signal Processor (DSP) are included.

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Introduction

The voice-band audio processor (VBAP) provides a bidirectional interface between voice/audio and a digital system processor. It accepts audio analog signals from sources such as microphones, digitizes the signals, and outputs them to a processing system. The VBAP receives digital signals from a processing system, converts them to analog, and outputs the signal to a device, such as a speaker.

While the information contained in this document relates to the entire VBAP family, it deals more specifically with the TCM320AC36, the 5 V, 2.048 MHz version.

Reference Material

Table 1 lists the reference material available for the 5 V (TCM) and 3 V (TLV) VBAP devices.

Table 1. VBAP Data Sheet Reference Material

Primary Application	13-Bit Linear Mode And µ-Law Device	A-Law Device	Master Clock (MHz)	Supply Voltage	Data Sheet Literature Number
IS-19, IS-54-136 and digital cordless	TLV320AC36	TLV320AC37	2.048	3 V	SLWS006A
IS-19, IS-54/136 and digital cordless, noise cancellation disabled	TLV320AC56	TLV320AC57	2.048	3 V	SLWS044
DECT	TLV320AC40	TLV320AC41	1.152	3 V	SLWS045
IS-19, IS-54/136 and digital cordless	TCM320AC36	TCM320AC37	2.048	5 V	SLWS003B
GSM	TCM320AC38	TCM320AC39	2.600	5 V	SLWS004B
Reduced specification “AC36”	TCM320AC46 †	N/A	2.048	5 V	SLWS001A
IS-19, IS-54/136 and digital cordless, noise cancellation disabled	TCM320AC56	TCM320AC57	2.048	5 V	SLWS016

† Obsolete - Replace with TCM320AC36 or TCM320AC36A

Features

TCM320ACxx (5-V Version)

- Single 5 V Power Supply Operation
- Low Power Consumption Modes
- Combined ADC, DAC, and Filters
- Extended Variable Frequency Operation
  - Sample Rates up to 16 kHz
  - Passband up to 7.6 kHz
- Electret Microphone Bias-Reference Voltage Available
- Drives a Piezo Speaker Directly
- DSP Compatible
- Selectable Between 8 Bit Companded and 13 Bit (dynamic range) Linear Conversion
  - TCM320AC36 µ-Law and Linear Modes
  - TCM320AC37 A-Law and Linear Modes
- Programmable Transmit Volume Control in Linear Mode
- Three-State DOUT Allows for Wired-OR Connection
- Designed to Comply with Various U.S. and International Standards such as U.S. Analog, U.S. Digital, CT2, DECT, GSM, and for use in PCN Hand-Held Battery-Powered Telephones

TLV320ACxx (3-V Version)

- Single 3-V Power Supply Operation
- Low Power Consumption Modes
- Combined ADC, DAC, and Filters
- Extended Variable-Frequency Operation
  - Sample Rates up to 16 kHz
  - Pass-Band up to 7.6 kHz
- Electret Microphone Bias-Reference Voltage Available
- Drives a Piezo Speaker Directly
- DSP Compatible
- Selectable Between 8 Bit Companded and 13 Bit (dynamic range) Linear Conversion
  - TLV320AC36 µ-Law and Linear Modes
  - TLV320AC37 A-Law and Linear Modes
- Programmable Transmit-Volume Control in Linear Mode
- Three-State DOUT Allows for Wired-OR Connection
- Designed to Comply with Various U.S. and International Standards Such as U.S. Analog, U.S. Digital, CT2, DECT, GSM, and for use in PCN Handheld Battery Powered Telephones

Overall Functional Information

The VBAP provides an interface between voice/audio and digital systems. The VBAP operations can be divided into three groups, which can then be broken into ten major tasks or functions. The groups and their functions follow.

Transmit Channel Group

- Microphone interface/mute function
- Transmit filters function
- Transmit encoding function
- Line Interface

Receive Channel Group

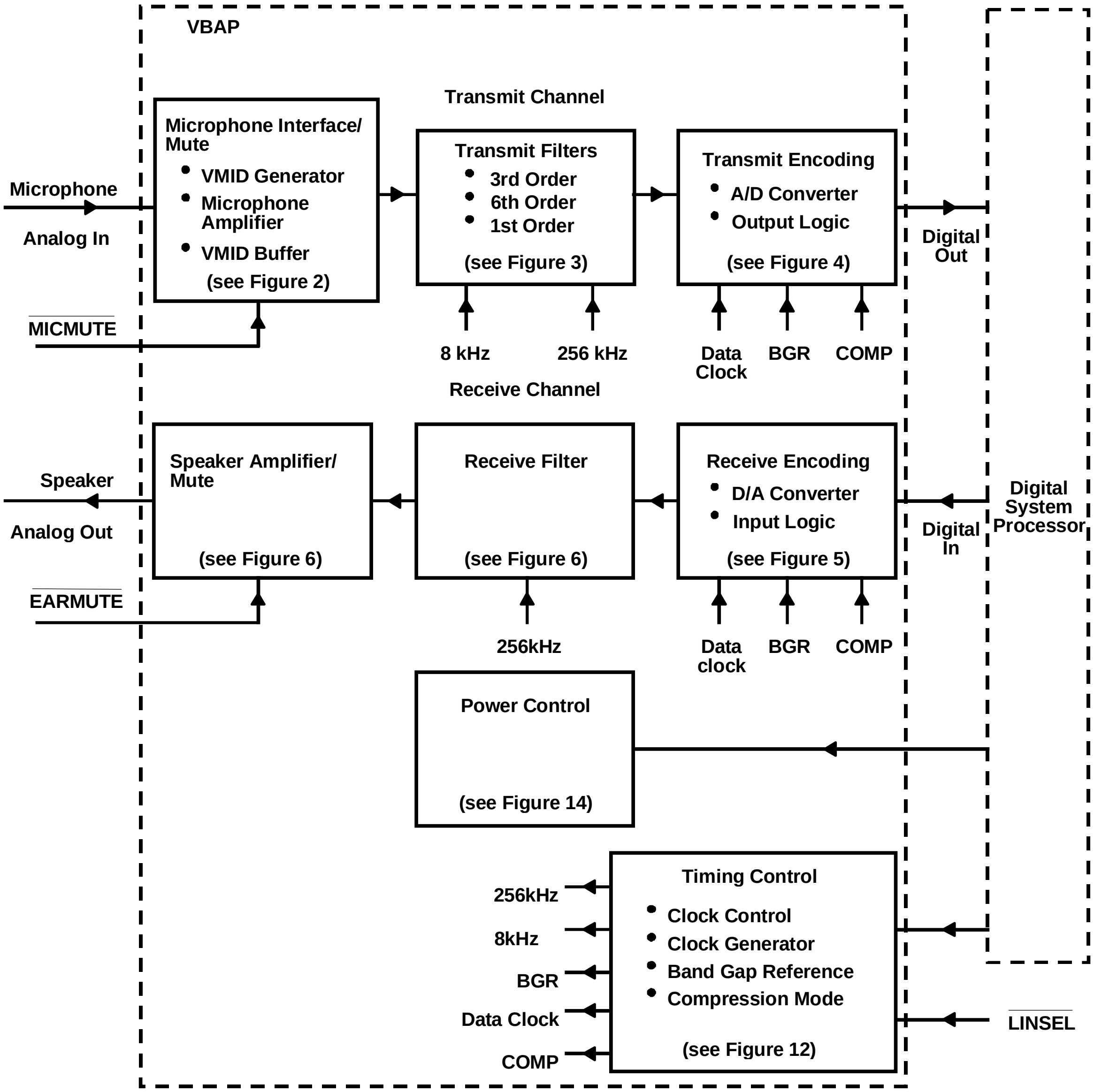
- Receive-encoding function
- Receive-filter function
- Speaker-amplifier/mute function
- Line Interface

Support Group

- Timing control function
- Power control function

Figure 1 shows the VBAP internal functions, subfunctions, and their relationships. The large dashed line box represents the chip boundary and the solid line boxes represent the functions. Functions are circuits that perform specific tasks, such as transmit encoding. Listed inside the major functions, as bulleted items, are subfunctions. Subfunctions are circuits that work together to perform a function.

Figure 1. VBAP Functional Block Diagram



Transmit Channel Group

The transmit channel group consists of the microphone interface/mute, transmit filters, and transmit encoding functions. The microphone interface/mute function buffers and amplifies the raw audio analog input signal. The transmit filters function contains anti-aliasing and bandpass filters that attenuate unwanted modulation. The transmit encoding function converts the analog signal to a digital value and places the resulting data in a shift register for reading by the host system.

Receive Channel Group

The receive channel group consists of the receive encoding, receive filter, and speaker amplifier/mute functions. The receive encoding function converts the digital data input from the receive channel shift register into analog. The receive filter function provides low-pass filtering. The speaker amplifier/mute function provides a configurable amplified analog output capable of driving a speaker or external amplifier.

Support Group

There are two support functions, timing control and power control. The timing-control function provides internal timing and selects compression mode and data rate. The compression mode selection sets the linear or compressed format. The data rate is either fixed or variable. The power control function controls the device power consumption mode.

Functions

The voice-band audio processor circuits are divided into three groups. The first group, the transmit channel, receives an analog input from a microphone, converts it to digital, and makes the resulting data available to the digital system processor. The second group, the receive channel, receives a digital signal, converts it to analog, and outputs it to a speaker. The third group, support, provides timing and power control. The three groups and their functions follow.

Transmit Channel Group

- Microphone-interface/mute (line interface) function
- Transmit-filters function
- Transmit-encoding function

Receive Channel Group

- Receive-encoding function
- Receive-filter function
- Speaker-amplifier/mute (line interface) function

Support Group

- Timing-control function
- Power-control function

Transmit Channel Group

The transmit channel group consists of the microphone interface/mute, transmit filters, and transmit encoding functions. These functions work together to convert the audio-analog input to digital. The resulting data is then made available to a digital signal processor.

Microphone Interface Function

The microphone interface function provides an interface to external gain-setting and microphone circuits as well as performs internal amplification and buffering. The function contains the microphone amplifier, VMID generator, and the VMID buffer.

A reference voltage, equal to one-half $V_{DD,}$ is provided to the VMID generator input by the voltage divider composed of R1 and R2. The VMID generator output, VMID, provides the mid-level virtual-ground reference for all internal amplifier circuits and the external microphone bias circuits.

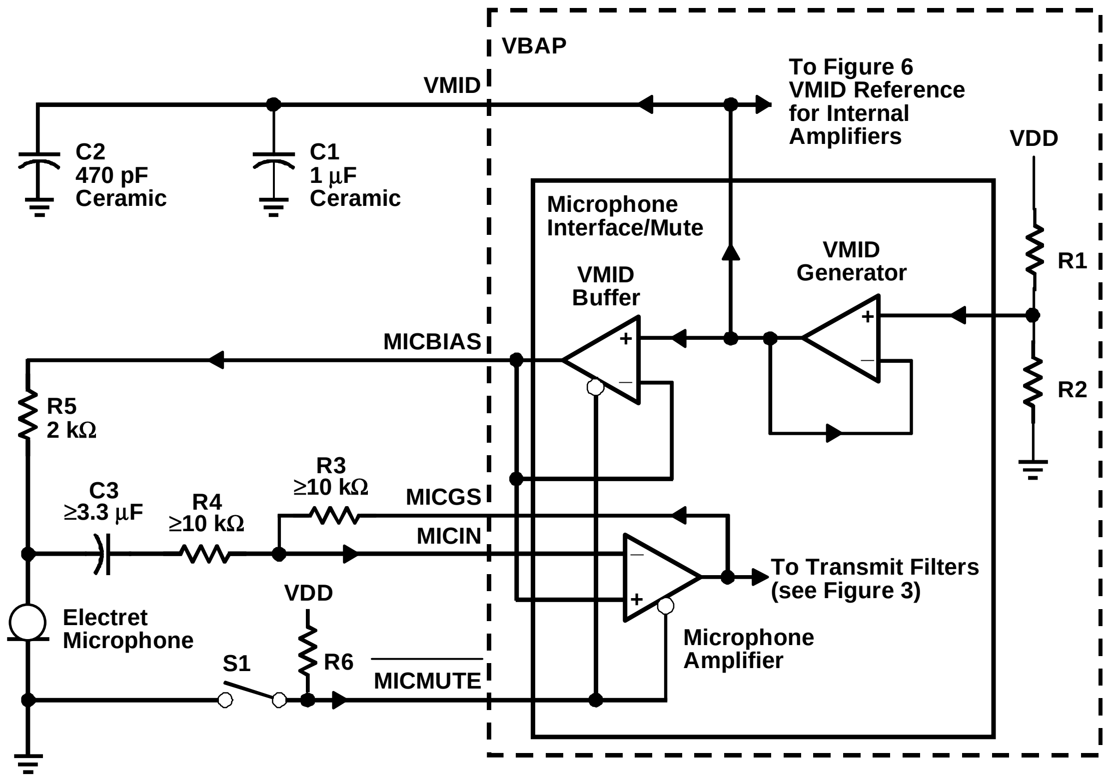
An external decoupling circuit eliminates power-supply noise on VMID. The reference voltage (VMID) is brought to an external pin to provide a place to attach an external decoupling circuit (see Figure 2). A typical external decoupling circuit consists of a 1 µF ceramic capacitor, C1, in parallel with a 470 pF ceramic-chip capacitor, C2.

The VMID buffer output, reference voltage MICBIAS, supplies bias current when used with an electret microphone. MICBIAS is also used internally to bias the microphone amplifier.

The microphone amplifier receives the microphone output signal MICIN. The gain of the microphone amplifier can be adjusted to accommodate a range of input signal levels. The gain is determined by the values of the external series capacitor C3 and the feedback resistor R3. The configuration shown in Figure 2 is typical of most applications.

A microphone mute capability is provided when switch S1 is closed holding /MICMUTE low to disable the microphone amplifier and the VMID buffer. When disabled, the output of the microphone amplifier is held at the high-impedance state. As a result, the output of the microphone amplifier is more than 80 dB down from the signal MICIN. In this state, the transmit filters remain active and the transmit-encoding function transmits zero code on DOUT.

Figure 2. Microphone Interface/Mute Diagram



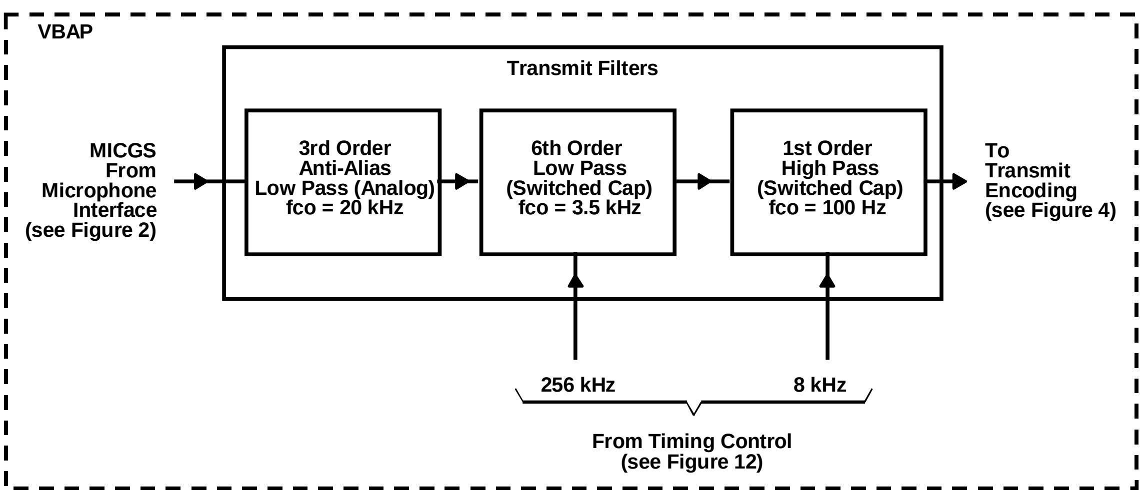
Transmit Filters Function

The amplified signal from the microphone interface function is passed through one anti-aliasing and two bandpass filters (see Figure 3) before being sent to the transmit encoding function to be digitized.

The anti-aliasing filter is an analog (continuous time) 3rd order lowpass filter with a frequency cutoff (f_{CO}) of 20 kHz. It attenuates any modulation components above one-half the sampling frequency of the next stage to avoid aliasing artifacts (Nyquist sampling theorem). The anti-aliasing filter provides more than 27 dB attenuation at one half the sampling frequency of 256 kHz, or 128 kHz, to the next filter stage.

To avoid the effects of aliasing, both bandpass filters are composed of oversampled switched-capacitor filters. The first bandpass filter is a 6th order lowpass filter with a frequency cutoff of 3.5 kHz, sampled at 256 kHz. The second is a 1st order highpass filter with a frequency cutoff of 100 Hz, sampled at 8 kHz. The effective 0 dB bandpass of these filters is from 300 Hz to 3.4 kHz. The oversampling and the clocks used by both these filters are synchronous so that anti-aliasing products can be easily controlled. The analog output is sent to the transmit encoding function.

Figure 3. Transmit Filters Block Diagram

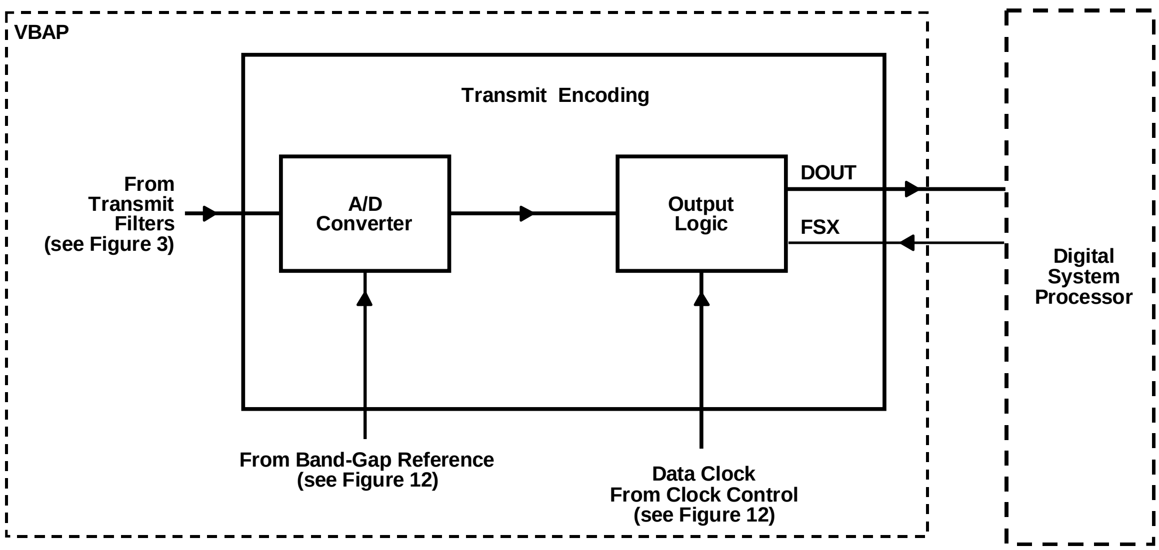


Transmit Encoding (A/D Conversion) Function

The transmit encoding function (see Figure 4) receives an analog signal from the transmit filters, converts it to digital, and holds the data for transfer to the host system. The function contains two major circuits (A/D converter and output logic) and one minor circuit (noise-reduction algorithm).

The output logic holds the data for transfer to the host system, as DOUT, in a serial-data stream. The data transfer is synchronized by the input from clock control. FSX is used in the variable-data mode. When FSX is present, the receiving device is ready to receive data.

Figure 4. Transmit Encoding Block Diagram



Circuit Operation

The encoded data word structure is available in the companded or linear formats. These are pin-selectable formats. When the companded mode is selected, the analog signal is sent to the transmit filters and input to a Compressing Analog-To-Digital Converter (COADC). The analog signal is encoded 8 bit digital representation by use of the µ-Law and A-Law encoding scheme, similar to CCITT G.711. When the linear conversion mode is selected, 13 bits of data are sent, padded with zeros to provide a 16 bit word. Both companded and linear conversion modes use 2s complement data. Data can be transmitted in either the fixed- or variable-data rate mode (see “Fixed- and Variable-Data Rate Modes” for more detail).

The A/D converter samples the output of the transmit filter at the middle of the frame and holds each sample on an internal sample-and-hold capacitor. It digitizes the analog input, starting in the second half of the frame. To minimize the delay across the VBAP, the conversion process does not complete until just before the next frame. Digital data representing the sample is transmitted at the start of the next frame. The transmit data is output on DOUT. Transmit data is clocked out on consecutive positive transitions of the serial data clock, (CLK) in the fixed-data-rate mode and DCLKX in the variable-date-rate mode.

For more information about the master clock and frame synchronization timing considerations, refer to the timing control function. For both companded and linear modes, the sign bit is transmitted first followed by the MSB and the LSB transmitted last. Since the A/D conversion rate is the frame sync rate and the bandpass switched-capacitor filter clocks are integer submultiples of the master clock, unwanted aliasing results are eliminated.

Noise Reduction Algorithm

Some members of the VBAP family incorporate a patented Texas Instrument circuit that reduces transmit noise to extremely low levels. These circuits reduce the transmit audio when the analog input falls below a set level and is used in the companded mode only. The level at which the noise reduction circuits are enabled includes hysteresis for further improved performance. These levels are about -55 and -60 dB. When the VBAP detects these low audio-input conditions, it outputs a zero code (1111 1111 in µ-Law, 0101 0101 in A-Law, similar to CCITT G.711 specifications). This differs from the normal output under idle channel noise conditions, which typically consists of a random sequence of codes around zero (LSB and/or second LSB and MSB sign bit toggling arbitrarily).

Receive Channel Group

The receive channel group consists of the receive encoding, receive filter, and the speaker amplifier functions. The receive-encoding function receives digital audio data and converts it to an analog signal. The receive filter provides low pass filtering. The speaker amplifier controls the analog output levels. The functions work together to provide an analog output signal used to drive an external amplifier or speaker.

Receive Encoding Function

The receive encoding function contains the input logic and digital to analog converter (D/A) circuits. The input logic receives digital data bits from the digital input (DIN). The input logic contains a buffer that provides temporary storage for data sent from the digital system processor.

The D/A converter converts its digital input into an analog output. It also contains volume control circuitry. The volume control circuitry uses data sent from the digital system processor to attenuate the analog output.

Data can be received in either the fixed or variable data rate modes (see “Fixed- and Variable-Data Rate Modes” for more detail).

The VBAP can operate in the linear and companded modes. When receiving in the linear mode, the VBAP works with 16 bit data words. Thirteen of the bits are used for data. The remaining three bits control the volume. These volume control bits originate from a digital system processor or other device that interfaces with the VBAP. The bits are used to attenuate the VBAP analog output in seven steps of 3 dB each. The volume control bits are not latched into the VBAP so they must be present in each received data word. If the volume control bits are missing, the VBAP circuitry assumes the three volume control bits are zero (0 dB attenuation). In the companded mode, programmable attenuation is not used. Table 2 lists the 3 bit volume control codes and their associated attenuation.

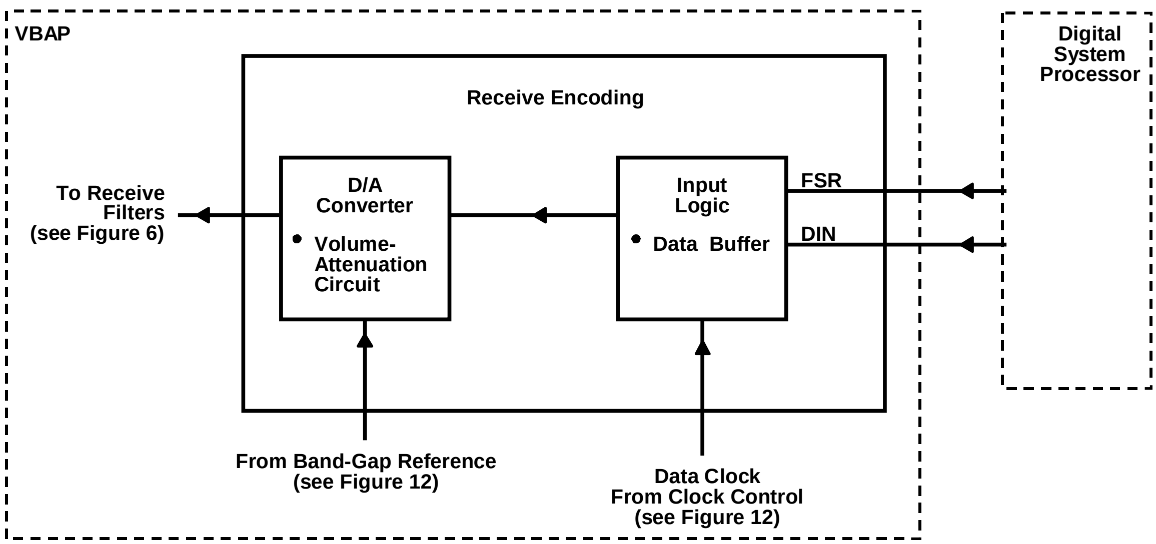
In the companding mode, the serial-data word is received at DIN on the first eight clock cycles. The decoding section converts the 8 bit PCM data into an analog signal with 12 bits of dynamic range. In the linear mode, the serial data word is received in the first 16 clock cycles. In both the companded and linear modes, input data is clocked in on consecutive negative transitions of the receive clock, which is CLK in the fixed-data-rate mode and DCLKR in the variable date rate mode. Digital-to-analog conversion is performed, and the corresponding analog sample is held on an internal sample-and-hold capacitor. The sample is transferred to the receive filter during the next frame.

Table 2. Receive Channel Volume Control Settings

Bits 14† -16 In Din Input Data Stream	Resulting Receive Channel Attenuation
000	0 dB
001	-3 dB
010	-6 dB
011	-9 dB
100	-12 dB
101	-15 dB
110	-18 dB
111	-21 dB

† Bit 14 is the most significant bit (MSB) of the volume control

Figure 5. Receive Encoding Block Diagram



Receive Filter Function

The receive filter is a switched-capacitor 6^{th} order lowpass filter with a frequency cutoff of 20 kHz. It provides passband flatness and stopband rejection that is similar to both the AT&T D3/D4 specifications and CCITT recommendations for G.712. The filter also contains the (sin x)/x correction response of such decoders.

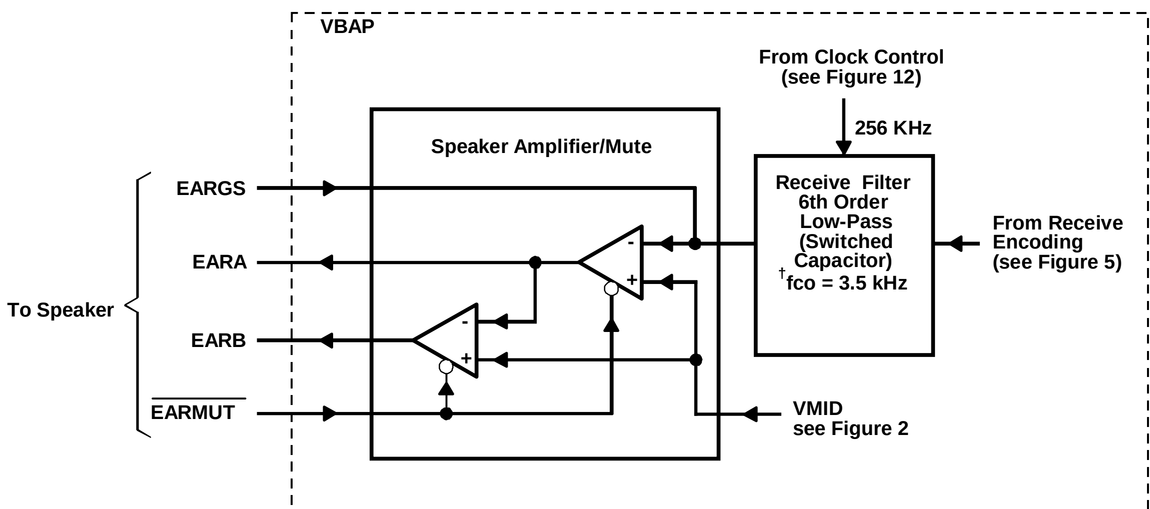
Speaker Amplifier/Mute Function

The VBAP incorporates an analog-output power amplifier. This amplifier can drive transformer hybrids or low-impedance loads in either a differential or single-ended configuration.

An external speaker-amplifier circuit in a differential configuration can be used for volume control, in addition to the volume control bits (see “External Speaker-Amplifier Circuit Configurations” for more information about external speaker-amplifier circuit configurations and “Receive Encoding Function” for more information about the volume control bits).

The speaker-amplifier output typically assumes a dc offset of approximately 40 mV. This is a normal consequence of using switched capacitors in the VBAP design. Potential biasing problems can be avoided by the use of an AC coupling capacitor.

Figure 6. Speaker Amplifier/Mute and Receive Filter Block Diagram



† fco is the -3db cut-off frequency.

External Speaker-Amplifier Circuit Configurations

The VBAP output can be routed to a speaker through an external circuit. There are two types of circuit configurations: differential gain and single ended. The differential-gain circuit determines the gain of the VBAP internal speaker-amplifier circuit. The differential-gain circuit is composed of a resistor network. The value and configuration of the resistors determine the VBAP speaker-amplifier circuit gain. The single-ended circuit configuration has fixed external gain.

NOTE:
When the VBAP is in linear mode, the volume can also be controlled by an external device (see the receive encoding function).

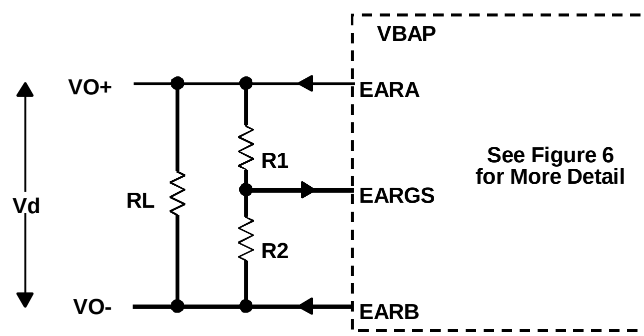
Speaker-Amplifier/Differential Gain Configurations

The differential gain circuits determine the VBAP speaker-amplifier circuit gain. This gain has a direct effect on the speaker volume. The configuration of the circuit and the value of the resistors used determine the amount of gain or volume. There are three variations of the fully differential gain circuit shown in Figure 7. These variations provide gains of 1 dB, 0.625 dB, and 0.25 dB, respectively.

Fully Differential Gain Configuration

For connection to a transformer primary, the fully differential gain configuration is recommended to provide maximum output or voltage swing. A piezo speaker can also be interfaced to the VBAP in the differential configuration. Figure 7 shows the VBAP in a fully differential gain configuration.

Figure 7. Fully Differential Gain Configuration



EARA and EARB are low-impedance complementary outputs. The total output voltage available for the speaker load (RL) is Vd = VO+ - VO-. Resistors R1 and R2 form a gain setting resistor network with a center tap connected to the EARGS input.

The value of R1 + R2 should be greater than 10 kΩ and less than 100 kΩ because the parallel combination R1 + R2 and RL sets the total loading. The total parasitic capacitance of EARGS along with the parallel combination of R1 and R2 define a time constant that must be minimized to avoid inaccuracies in the gain calculations.

The resistor gain control actually consists of attenuating the full differential output voltage. The equation to determine the value of the attenuation constant A, is as follows:

$$A = \frac{1 + (R1/R2)}{4 + (R1/R2)}$$

which can also be expressed as:

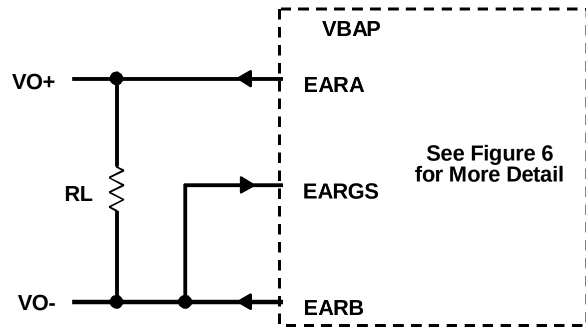
$$A = \frac{R1 + R2}{4(R2 + R1/4)}$$

Depending on the values of the gain setting resistors R1 and R2, the attenuation constant A can have a value of 0.25 dB to unity (1), or about 12 dB of voltage adjustment.

Fully Differential Maximum Gain Configuration

The maximum output gain (A = 1 dB) can be obtained by maximizing R1 and minimizing R2, (see Figure 7). This can be done by letting R1 = • and R2 = 0. The actual maximum gain configuration is shown in Figure 8. Using this configuration achieves a maximum gain of approximately 3 Vpp.

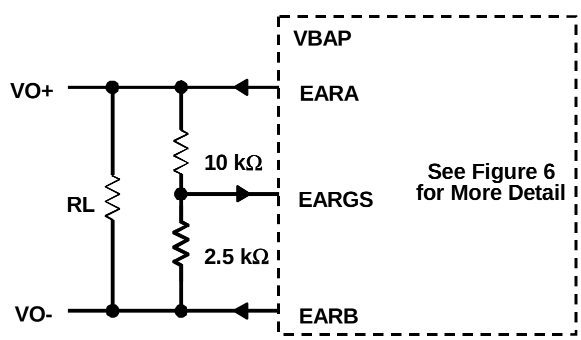
Figure 8. Fully Differential Maximum Gain Configuration (A = 1)



Fully Differential Middle Gain Configuration

The VBAP in the middle gain configuration is shown in Figure 9. This configuration uses an R1 of 10 kΩ and an R2 of 2.5 kΩ. This configuration results in a gain of A = 0.625 dB.

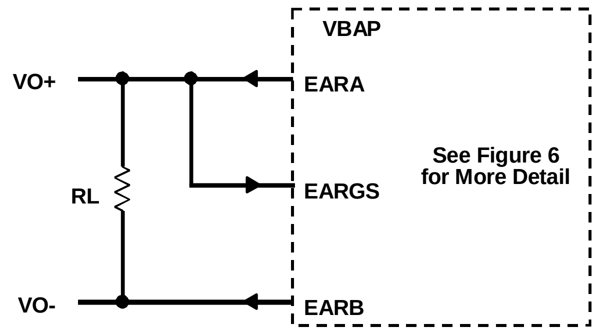
Figure 9. Fully Differential Middle Gain Configuration (A = 0.625 dB)



Fully Differential Minimum Gain Configuration

A minimum gain configuration of A = 0.25 dB is shown in Figure 10. In this configuration, R1 = 0 Ω (common EARGS and EARA) and R2 = • (refer to Figure 7).

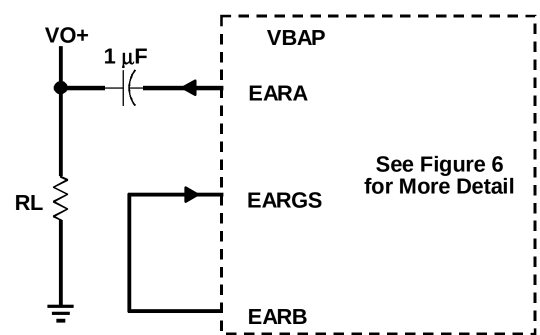
Figure 10. Fully Differential Minimum Gain Setting Configuration (A = 0.25 dB)



Speaker-Amplifier, Single-Ended Configuration

In the single-ended configuration, EARB and EARGS are common (as in the maximum differential gain configuration) and the load is connected between EARA and ground. The output drives a single ended load with the output signal voltage centered on 1/2 V_{DD}. For that purpose, a DC blocking capacitor of approximately 1µF is recommended in the single ended mode. This gives a highpass response with a -3 dB cut-off frequency of 265 Hz with an RL of 600 Ω. Resistor-network gain control is not available in this mode. As in all single-ended configurations, the output voltage swing is one-half the full-differential voltage swing. The single-ended mode is most commonly used when interfacing to a succeeding stage that is referenced to true ground. Figure 11 shows the VBAP in a single-ended configuration.

Figure 11. Single-Ended Configuration



The VBAP is specified and tested to drive 600 Ω loads. Although laboratory characterization has shown that it can drive loads as low as 50 Ω, the VBAP is not guaranteed to meet all parametric specifications with loads lower than 600 Ω.

Support Group

The support group consists of the timing control and the power control functions. These functions work together to provide operational support for the other VBAP functions.

Timing Control Function

The timing control function, shown in Figure 12 contains the clock-control, clock-generator, and band-gap reference circuits. These circuits work together to provide VBAP timing control.

Clock Control Circuit

The clock control circuit gates and synchronizes the VBAP internal clock and framing pulses, and monitors frame pulses FSX and FSR for standby mode operation. Active low signal /LINSEL controls function COMP. COMP selects transmit or receive data word format (8 or 13 bit).

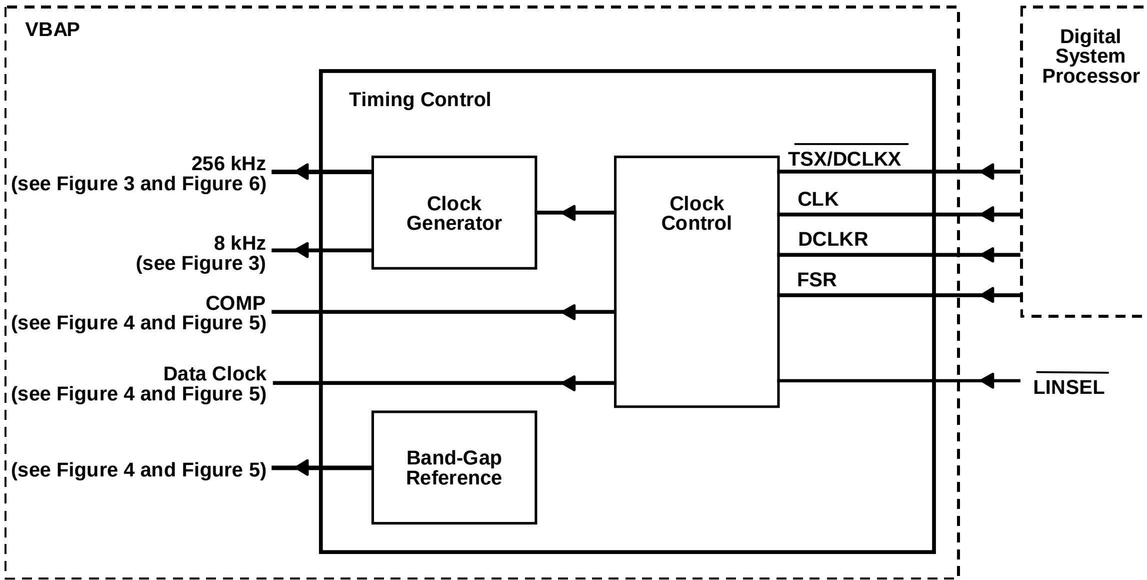
Clock Generator Circuit

The clock generator circuit uses the master clock input to generate the internal 256kHz clock. These clocks drive the internal counters that drive the VBAP filters and converters.

Band Gap Reference Circuit

A precision band-gap reference voltage is generated internally and is used to supply all required references for operation of both the transmit and receive channels. The gain in each channel is trimmed during the manufacturing process. This process ensures accurate, stable gain performance over the variations in supply voltage and temperature.

Figure 12. Timing Control Block Diagram



Master Clock and Frame Synchronization

The VBAP requires a master clock and frame synchronization. The master clock is used for many internal functions, most notably to clock the switched capacitor filters, and for A/D and D/A conversion. The VBAP family supports a variety of master clock frequencies, as shown in Table 3.

Table 3. VBAP Master Clock Frequencies

Device Suffix (XX)	Master Clock (MHz)
36,37,56	2.048
38,39	2.600
40,41	1.152
42	1.944
44	1.536

When using any of the VBAP master clock rates listed in Table 3, the following device clocking guidelines should apply.

- ❑ The master clock and frame sync are synchronized internally. The data clock does not need to be a submultiple of the master clock.
- ❑ Each VBAP must maintain a specific ratio of master clock to frame sync. If the ratio is too low (frame sync frequency is too high with respect to the master clock), the VBAP A/D and D/A conversion processes might not be complete when the next

frame sync arrives. Likewise, if the ratio is too high (frame-sync frequency is too low with respect to the master clock), data corruption can occur.

- The ratio for the correct master clock-to-frame sync ratio for each VBAP can be determined by the following equation:

  Ratio = master clock frequency/8000

- While each VBAP is optimized to function with its respective master clock frequency for low noise, distortion, and pass band characteristics at an 8 kHz sampling rate, there are occasions when a higher sampling rate is desired. This is allowable providing the calculated ratio between master clock and frame sync is maintained. For example, to operate a TCM/TLV320AC36 VBAP at 16 kHz, first calculate the master clock to frame sync ratio:

  Ratio = 2.048 MHz/8000 = 256

- To maintain the same ratio with a frame sync of 16 kHz, the master clock must be increased. Again, using the original formula for the ratio:

  256 = master clock frequency/16,000

  the master clock becomes 256 x 16,000 = 4.096 MHz

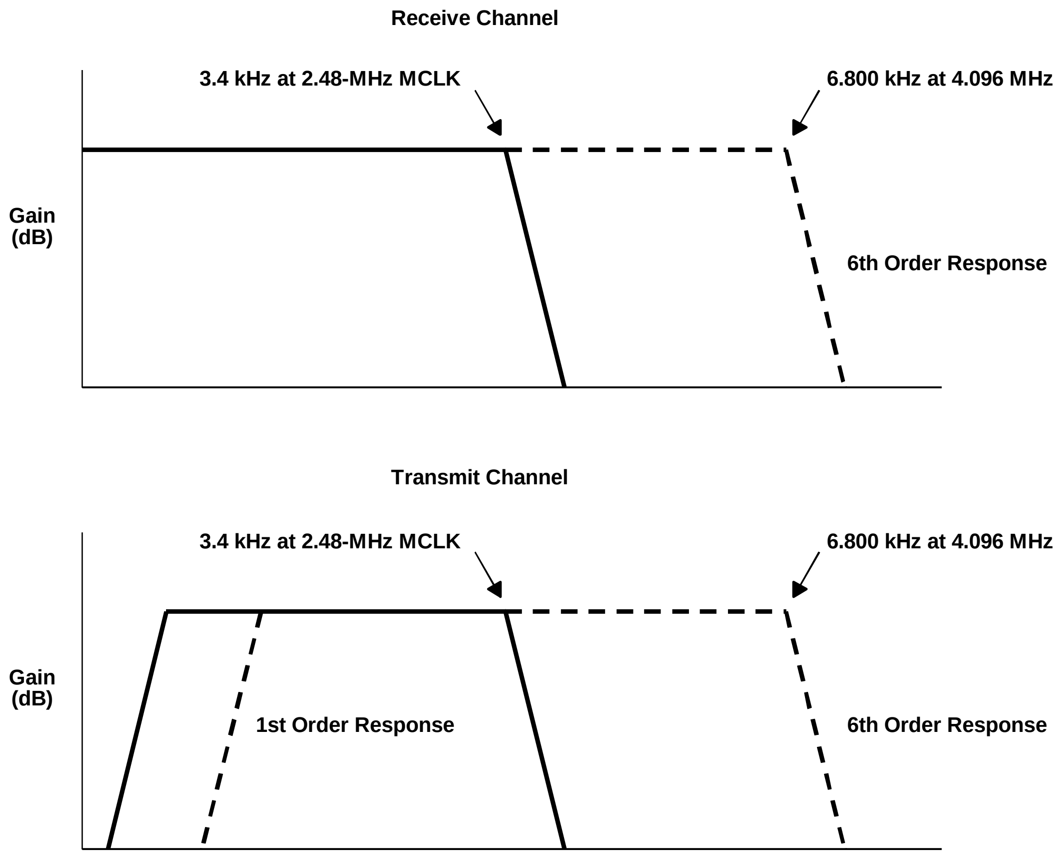
- Altering the master clock frequency changes the device transmit and receive passbands. The VBAP series is designed for a 0 dB pass band of 300 Hz to 3.4 kHz. When the master clock frequency is increased or decreased, the switched capacitor's filter minimum and maximum cutoff points change proportionally. The continuous time filters are unaffected. This results in narrowing or widening the filters' pass band. The effect of the master clock frequency on filter characteristics is shown in Figure 13.

- The data clock (DCLK) signals should be synchronous with the master clock signal (CLK), but DCLK does not need to be a submultiple of CLK. Synchronous means that the edges of DCLK should occur at the same point in each signal of CLK. If the two clocks are allowed to free run with respect to each other, a slight but acceptable increase in idle-channel noise can be expected. To reduce the idle-channel noise, both clocks should be as synchronous as possible.

Effect of Master Clock-to-Frame Sync Ratio on Filter Characteristics

Using a TCM/TLV320AC36 VBAP with a master clock frequency of 2.048 MHz (and a frame sync of 8 kHz) yields a 0 dB pass band, of 300 Hz to 3.4 kHz (corresponds to 120 Hz and 3.5 kHz 3 dB cutoff points) in the transmit channel. If the master clock frequency is increased to 4.096 MHz (with a frame sync of 16 kHz), the high-pass cutoff of 300 Hz shifts to 600 Hz and the low-pass cutoff shifts from 3.4 kHz to 6.8 kHz, as shown in Figure 13.

Figure 13. Master Clock Frequency Effect on Filter Characteristics Diagram



The receive channel is identical except that it does not have a high pass filter and the VBAP has approximately a 0 dB filter response at frequencies below 300 Hz.

By using the following formula, the absolute cutoff frequency can be calculated for any new master clock frequency:

$$\text{Absolute cutoff freq (kHz)} = \frac{\text{normalized cutoff freq (kHz) X new MCLK}}{\text{original MCLK}}$$

Where:
the absolute cutoff frequency is the new scaled cutoff frequency.
the normalized cutoff frequency is the specified cutoff frequency at the original MCLK.
the new MCLK is the new master clock frequency.

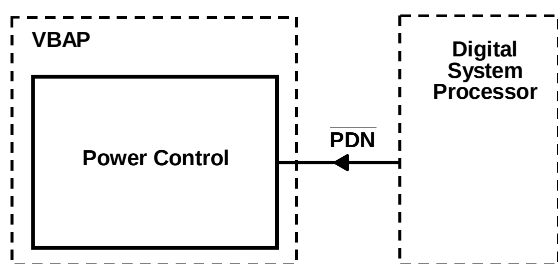
Each member of the VBAP family is designed to function with its respective master clock frequency. The master clock frequency can be increased (maintaining the same master clock/frame sync ratio) up to double the standard frequency. Beyond this frequency, the VBAP response degrades rapidly.

Power Control Function

To minimize power consumption, a power down mode and three standby modes are provided.

For power down, an external low signal is applied to /PDN (see Figure 14). In the absence of a signal, /PDN is pulled up internally to a high logic level and the device remains active. In the power down mode, the average power consumption is reduced to 2 mW.

Figure 14. Power Control Block Diagram



Standby Modes

The standby modes provide the option to put the entire device on standby or to put only the transmit or receive channels on standby. The standby modes are entered by removing one or both of the frame syncs. Table 4 lists all VBAP power down and standby modes of operation.

Table 4. TCM/TLV320ACXX VBAP Power Down and Standby Procedures

Device Status	Procedure	Typical Power Consumption		Digital Output Status
		5 V	3 V	
Power on	/PDN = high FSX = pulses FSR = pulses	40 mw	20 mw	Active
Power down	/PDN = low FSX/FSR = X/X	3 mw	2 mw	/TSX and DOUT in the high-impedance state
Entire device on standby	FSX = low FSR = low /PDN = high	5 mw	5 mw	/TSX and DOUT in the high-impedance state
Receive only (transmit standby)	FSX = low FSR = pulses /PDN = high	20 mw	10 mw	/TSX and DOUT in the high-impedance state within 5 frames
Transmit only (receive standby)	FSR = low FSX = pulses /PDN = high	20 mw	10 mw	Active

Note: X/X = Don't care

Principles of Operation

To minimize crosstalk, the VBAP design uses independent converters and filters for the transmit and receive channels.

The VBAP family of devices represents a line of highly specialized single supply (5 V or 3 V) CODECs, specifically designed for use in battery powered personal communications systems. The VBAP uses the TI LinEPICZ1™ 1 µm semiconductor process, which results in very low power consumption. In addition, a patented TI process is used to maintain extremely low noise specifications. The VBAP device provides an interface between voice and digital system processors, and incorporates three major functions: transmit encoding (A/D conversion), receive decoding (D/A conversion), and transmit and receive filtering (see Figure 15). The VBAP family supports a serial data connection in either 8 bit companded µ-Law or A-law modes, along with a pin-selectable 13 bit linear-conversion mode. The VBAP uses switched capacitor filters to provide filtering compatible with most personal communication specifications, including EIA/TIA/IS-54/136 for the U.S. digital cellular telephones and is similar to the CCITT G.711 and G.712 µ-law and A-law filtering requirements. The VBAP also provides direct microphone and speaker interface.

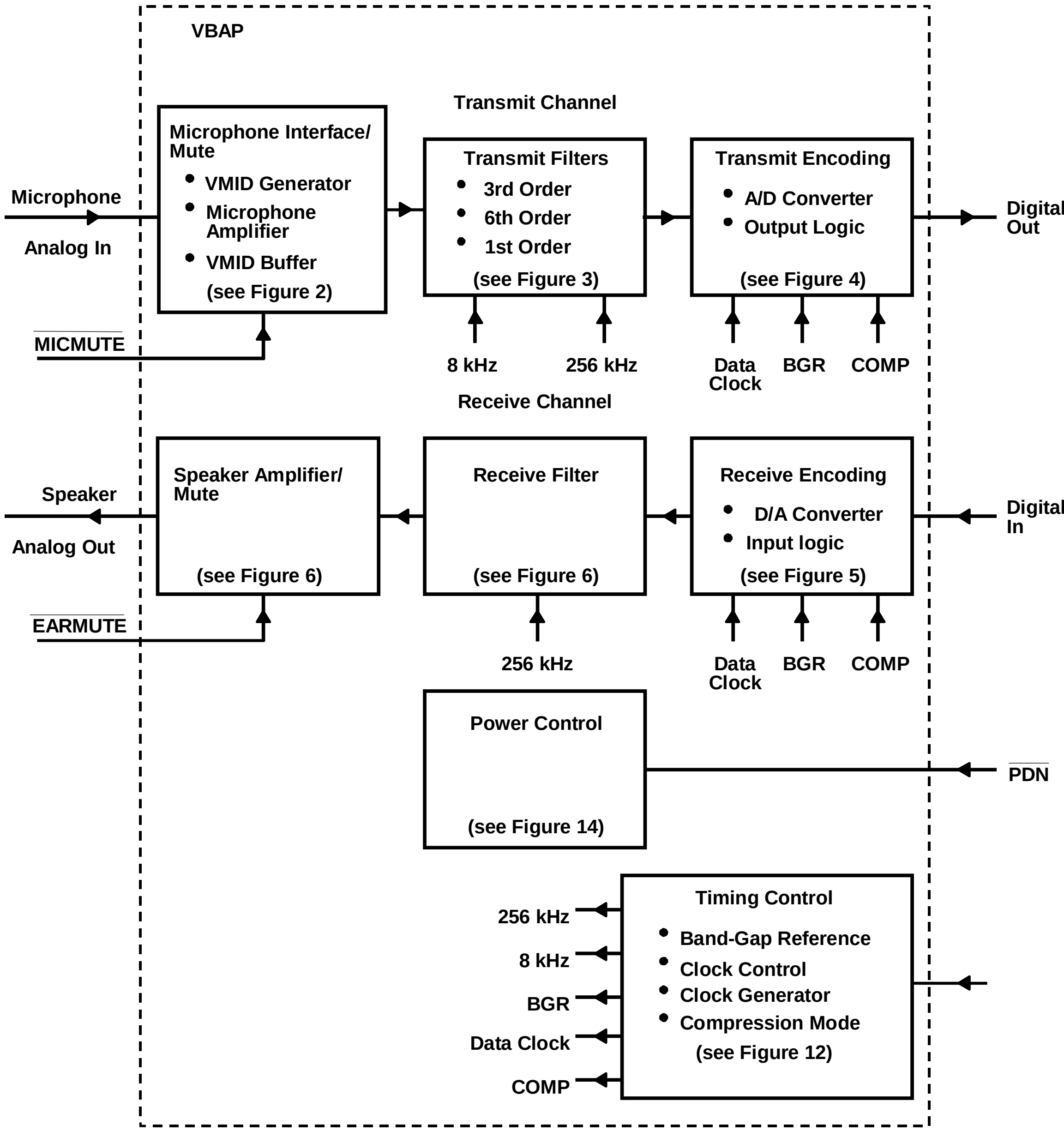
The TCM prefix denotes the 5-V version, and the TLV prefix denotes the 3-V version.

The VBAP devices are available in 20 pin N (dual-in-line plastic), DW (wide body surface mount), and S-PQFP (shrink-plastic-quad-flatPack, PT, <1.7 mm height) packages.

NOTE:

All discussion of timing is based on a 2.048 MHz Master Clock and an 8 kHz frame sync rate.

Figure 15. VBAP Block Diagram



Fixed- and Variable-Data Rate Modes

The VBAP is designed to operate in both the fixed-data-rate and variable-data-rate modes. The mode of operation is pin selectable. In the fixed-data-rate mode, the data is transmitted (or burst) and received at the rate of the master clock frequency and sampled every frame. In the variable-data-rate mode, the data is transmitted or received at a rate slower than the master clock frequency using DCLKR and DCLKX for the data clock.

The TCM/TLV320AC36 VBAP can be used in the 8 bit companded mode with variable data rate. The data is sampled every 125 µs, but the speed at which the data is transmitted and received can vary from 2.048 MHz to 64 kHz. The slowest speed of the data clock is 64 kHz. At 64 kHz, the complete frame is used to transmit or receive the data (8 bits x 8000 = 64 Kbit/sec). Likewise, the minimum variable-data-rate speed for the 16 bit linear mode is 128 kHz (16 bits x 8000).

Fixed-Data-Rate Mode

The fixed-data-rate timing is selected by connecting DCLKR to V_{DD}. In this mode, the data is transmitted or received at the MCLK speed once every frame sync. Data is transmitted on DOUT on the rising edges of each MCLK pulse and received at DIN on the falling edges of each MCLK pulse, only after the rising edge of each transmit or receive frame sync pulse (FSX or FSR). Both the transmit and receive frame sync pulse have a width equal to the master clock period.

Active low signals /TSX and /DCKLX become an output for the transmit time strobe in the fixed-data-rate mode. It remains low during the entire time each 8 or 16 bit word is transmitted from DOUT.

Variable-Data-Rate Mode

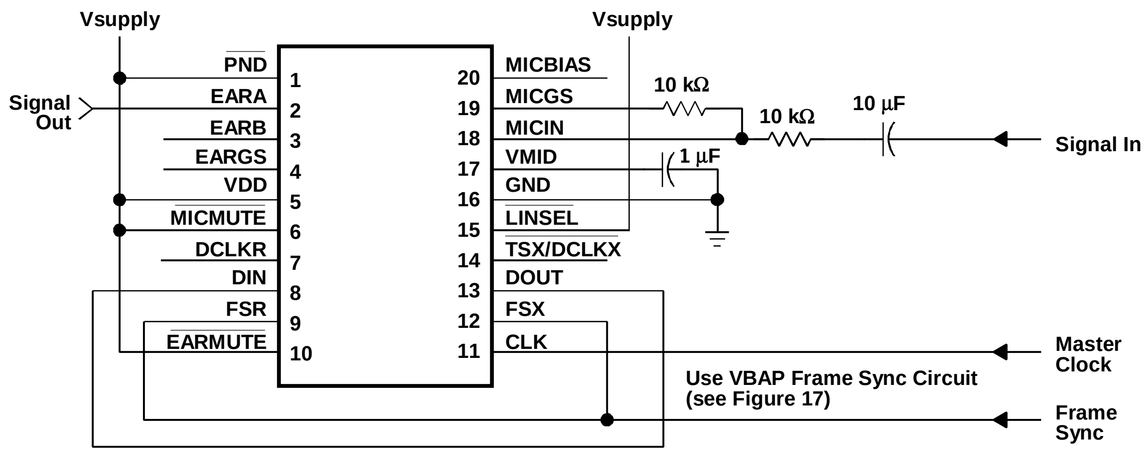
The variable-data-rate timing is selected by connecting DCLKR to an external data clock. In this mode, the data is transmitted (burst) or received at the /DCKLX or DCLKR speed once every frame sync. Data is transmitted on DOUT starting on the rising edges of each DCKLX pulse and received at DIN on the falling edges of each DCLKR pulse only after the rising edge of each transmit or receive frame sync pulse (FSX or FSR). These frame sync pulses must stay high for the duration of all transmitted or received data bits (8 bits companded, 16 bits linear).

In the transmit mode, if the FSX frame sync is held high for longer than the 8 or 16 bits, the same data word is transmitted until the frame sync is low again. New samples are not taken during that time. In this respect, the same data word can be transmitted more than once in each frame, if desired. In the receive configuration, if FSR is held high for longer than the 8 or 16 bits of data, only the first 8 or 16 bits of data are decoded and the remaining bits are not used.

VBAP Loopback Test

The VBAP full duplex capabilities can be tested with a Pulse Code Modulation (PCM) loopback test. In the loopback test configuration, the VBAP is used simultaneously as a transmitter and receiver. An analog signal is applied at MICIN, encoded by the VBAP into serial data, and looped back (DOUT to DIN) to be decoded by the VBAP from digital back into analog. The analog output and input can then be compared using an oscilloscope. Figure 16 shows the VBAP in a typical PCM loopback configuration with the VBAP in the companded, fixed-data-rate mode.

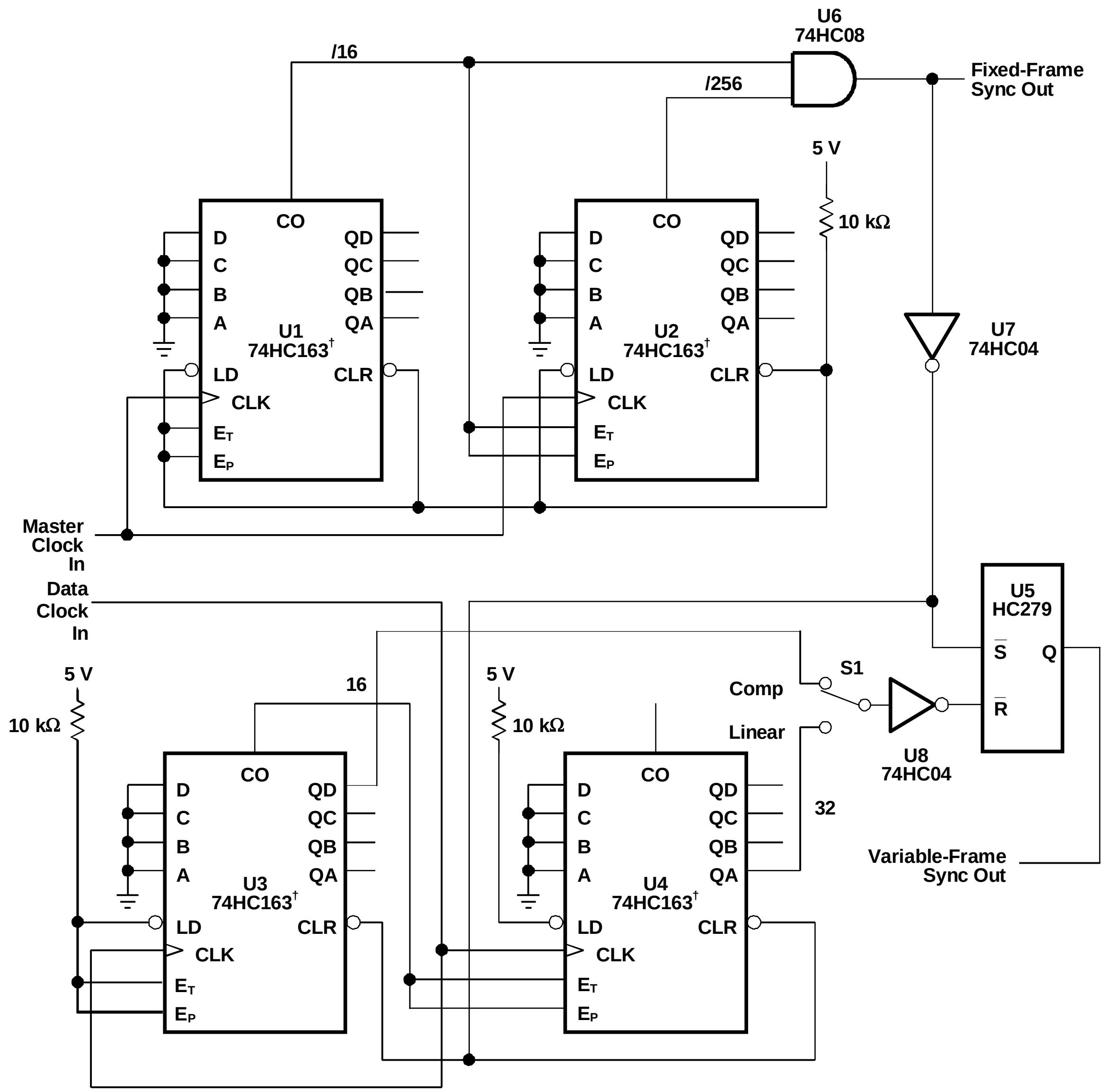
Figure 16. VBAP PCM Loopback Test Configuration Diagram



VBAP Frame Sync Circuit

Most VBAP applications use clocks generated from a digital system processor or ASIC clock generators. However, testing the VBAP in the Pulse Code Modulation (PCM) loopback configuration and selected other applications requires generation of a master clock and frame sync from discrete components. The circuit in Figure 17 generates a master clock and frame sync for the VBAP with a master clock to frame sync ratio equal to 256 to 1, as with the VBAP model TCM/TLV320AC36/37 in both the fixed- and variable-data-rate modes of operation.

Figure 17. VBAP Fixed and Variable Frame Sync Circuit Diagram



† 74LS163 counters are fully synchronous.

The circuit shown in Figure 17 performs two functions. The upper part generates the fixed frame sync pulse. The lower part generates the variable frame sync pulse.

In the upper part of the circuit, U1 and U2 74HC163 4 bit counters are clocked synchronously by the signal-master clock-in (CLK). U2 is cascaded with U1 so that it counts on each 16th master clock. The CO (carry out) on U2 outputs a pulse on every 256th master clock, and it has a period of one master clock pulse. This is required for the fixed-data rate frame sync. The carry out of 74HC163 counters produces a glitch prior to the carry out pulse. Since the VBAP frame-sync input is edge triggered, it identifies both the true carryout pulse and the glitch as frame syncs. This problem with the 74HC163 counters can be avoided by logically ANDing the carryouts of the U1 and U2 timers as shown at U6, so that only the true carryout pulse is seen at the fixed-frame sync output.

In the lower part of the circuit, RS latch U5 is set by the fixed frame sync output after the first 256 master clock pulses. Counters U3 and U4 are clocked synchronously by the signal data clock in and are connected to the U5 RS latch so that the latch resets after 8 or 16 data clocks are counted. These are selected by switch S1; the Q output of the latch is then high for the duration of the 8 or 16 bits of data required for the variable frame sync.

Gain Analysis

This section describes the VBAP absolute and throughput gains. The following topics are covered:

- Absolute transmit and receive gains
- CCITT PCM encoding format
- Absolute transmit and receive gain
- Analog input that produces the maximum digital output
- Maximum analog output
- Digital loopback test and the associated gains through the transmit and receive channels
- Analog loopback test and the associated gains through the transmit and receive channels

The VBAP develops a precision band-gap reference voltage. This reference voltage is used for both the transmit and receive channels. The gain in each channel is trimmed during the manufacturing process. This process ensures very accurate, stable gain performance over the variations in supply voltage and temperature.

Absolute Transmit and Receive Gains

The VBAP data sheet does not specify absolute gains, but does specify a 0 dB reference signal level input for µ-Law, A-Law companded, and linear conversion modes. The reference level signal shown in the receive gain and dynamic range section of the VBAP data sheet is zero transmission level (0TL). Zero transmission level is the signal level at the analog output of a CODEC (in the receive channel) when a digital milliwatt sequence is input to the device.

The reference signal level specified under the transmit gain and dynamic range section of the VBAP data sheet is not the 0TL but is the analog signal required to produce a digital milliwatt on the PCM output of the device.

A digital milliwatt, or digital milliwatt sequence, is the PCM sequence. The sequence is similar to the CCITT specification G.711. This specification is found in Volume III of *CCITT Digital Networks, Transmission Systems and Multiplexing Equipment, Recommendations G.700-G.956*. A digital milliwatt is defined as:

A sine wave signal of 1 kHz at a nominal level of 0 dBm0 is required for any voice frequency output of the PCM multiplex when the periodic sequence of the character signals of the CCITT Table 5/G.711 for the A-law and of Table 6/G.711 for the µ-Law is applied to the decoder input.

A digital milliwatt is a PCM sequence that, when converted to analog, produces a 0 dBm0 signal or analog milliwatt.

Table 5 combines both of the CCITT tables previously mentioned and shows the sequence of the eight 8 bit words for both A-Law and µ-Law that are defined as a digital milliwatt (bit 1 is MSB, bit 8 is LSB, and the words are input from top to bottom).

Table 5. Digital Milliwatt Sequences, A-Law and µ-Law

A-Law								**µ-Law**							
1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**
0	0	1	1	0	1	0	0	0	0	0	1	1	1	1	0
0	0	1	0	0	0	0	1	0	0	0	0	1	0	1	1
0	0	1	0	0	0	0	1	0	0	0	0	1	0	1	1
0	0	1	1	0	1	0	0	0	0	0	1	1	1	1	0
1	0	1	1	0	1	0	0	1	0	0	1	1	1	1	0
1	0	1	0	0	0	0	1	1	0	0	0	1	0	1	1
1	0	1	0	0	0	0	1	1	0	0	0	1	0	1	1
1	0	1	1	0	1	0	0	1	0	0	1	1	1	1	0

The following is a derivation of the analog digital milliwatt, or 0 dBm, which is defined as 0.775 Vrms into a 600 Ω load (or 0.9487 Vrms into a 900 Ω load).

$P = \frac{Vrms^2}{R}$ where P = 1 mW = .001 W

$Vrms = \sqrt{PxR}$ where R = 600 or 900 Ohms

So:

$Vrms = \sqrt{0.6} = 0.775$ Vrms for 600 Ohm load

$Vrms = \sqrt{0.9} = 0.9487$ Vrms for 900 Ohm load

CCITT PCM Encoding Format

The PCM encoding format (see Table 6) used by the VBAP family of devices is similar to that defined by CCITT specification G.711. This specification is also found in Volume III of *CCITT Digital Networks, Transmission Systems and Multiplexing Equipment, Recommendations G.700-G.956*.

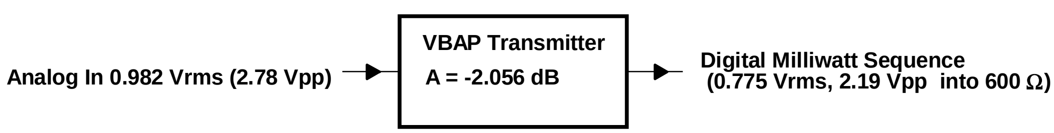
Table 6. PCM Encoding Format

Corresponding Analog Input	µ-Law Encoding	A-Law Encoding (Includes Even Bit)
V_I = full scale	1000 0000	1010 1010
V_I = 0	1111 1111 0111 1111	1101 0101 0101 0101
V_I = -full scale	0000 0000	0010 1010

Absolute Transmit Gain

In the transmit gain and dynamic range section of the VBAP data sheet, the signal level input required to produce a digital milliwatt as 0.982 Vrms (or 2.78 Vpp) if µ-Law is defined. Since the digital milliwatt is defined as 0.775 Vrms or 2.19 Vpp, the resulting transmit gain is A = 20log(0.775/0.982) = -2.056 dB (see Figure 18).

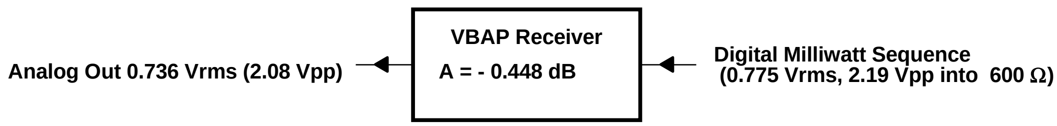
Figure 18. VBAP Absolute Transmit Gain, µ-Law



Absolute Receive Gain

In the receive gain and dynamic range section of the VBAP data sheet, the analog signal output level when a digital milliwatt is applied to the device, or the 0TL, is 0.736 Vrms (or 2.082 Vpp) if µ-Law is defined. This assumes the receive audio output is measured differentially in the maximum gain configuration, as set by the resistor chain on the VBAP output. The maximum differential gain can be set by connecting EARGS to EARB, and the output is taken between EARA and EARB. Again, since the digital milliwatt is defined as 0.775 Vrms or 2.19 Vpp, the resulting receive gain is A = 20log(0.736/0.775) = -0.448 dB (see Figure 19).

Figure 19. VBAP Absolute Receive Gain, µ-Law



Analog Input That Produces Maximum Digital Output

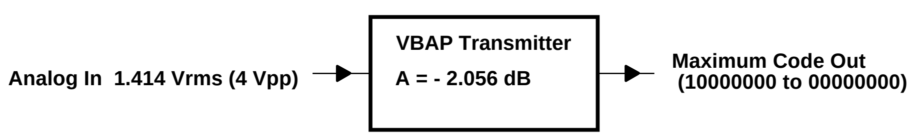
The VBAP evolved from CODECS and filters used for line card applications. In telephone line card applications, maximum audio level input and output is defined by the CCITT standard. This audio level is 3.17 dBm0 in µ-Law and 3.14 dBm0 in A-Law. A dBm0 is defined as a unit of power that is referenced to the zero transmission level (0TL). The zero transmission level is the resulting signal level at the analog output of a CODEC (in the receive mode) when a digital milliwatt sequence is input to the device. Therefore, 3.17 dBm0 is a signal that is 3.17 dB higher than the signal that is present under the digital milliwatt sequence stimulus (or 3.17 dB higher than the 0TL). The 0TL is specified in the VBAP data sheet as 0 dB transmit gain with a dynamic range of 0.982 Vrms (2.778 Vpp) in µ Law, so 3.17 dB above this reference is the maximum analog signal input permitted by a µ Law VBAP in the transmit mode.

3.17 dB = 20Log(maximum analog input signal/2.778 Vpp)

so the maximum input analog signal = A = 4 Vpp = 1.414 Vrms.

With a VBAP microphone section connected for unity gain and the device in µ-Law operation (see Figure 20), the maximum analog input signal is 4 Vpp. Any higher voltage does not produce a corresponding change in the A/D output at PCM OUT. Expect the best noise performance (S/N ratio) from the VBAP when the maximum audio input is used, so the gain of the microphone amplifier should be adjusted to output 4 Vpp whenever possible.

Figure 20. Maximum Digital Output, µ-Law



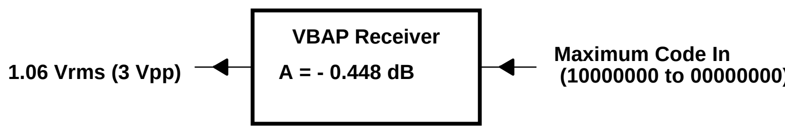
Maximum Analog Output

As previously stated, the maximum audio output of the VBAP is 3.17 dBm0 in µ-Law and 3.14 dBm0 in A-Law (measured differentially). Since 0 dB is defined in the VBAP specification under receive gain and dynamic range as 0.736 Vrms (2.08 Vpp) in µ-Law, 3.17 dB above this reference is the maximum analog signal output by the VBAP in the receive mode. See Figure 21 for the maximum analog output in µ-Law.

3.17 dB = 20Log(maximum output analog signal/2.08 Vpp)

so the maximum analog output signal = A =3 Vpp = 1.06 Vrms.

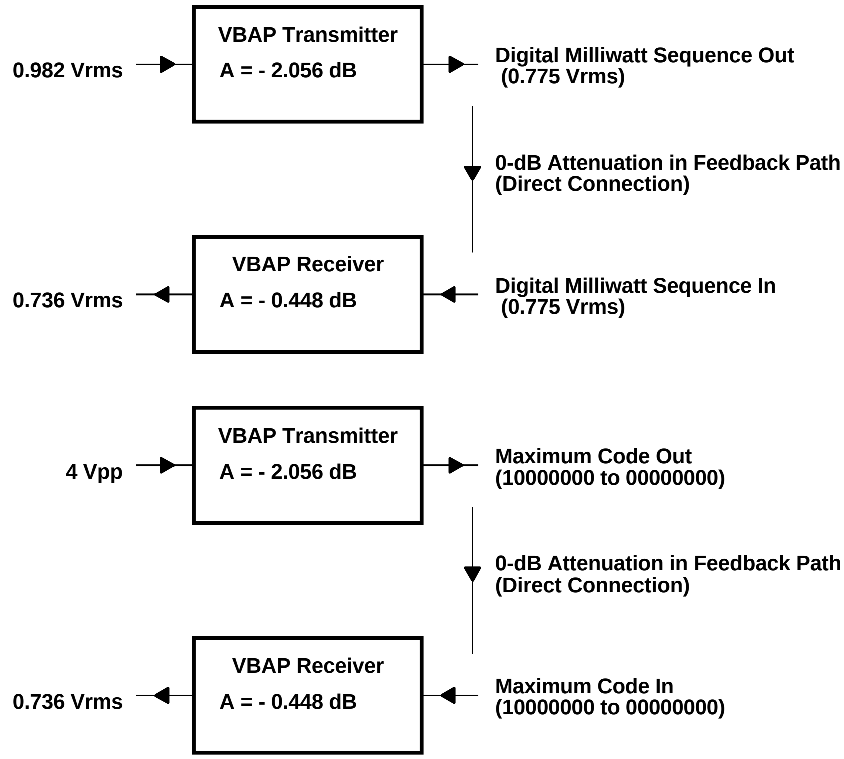
Figure 21. Maximum Analog Output, µ-Law



Digital Loopback Test and Associated Gains through the Transmit and Receive Channels

With the transmit and receive gains determined, the throughput gain of a VBAP in the digital loopback configuration (-2.056 - 0.448) = -2.504 dB), can be shown. Figure 22 illustrates the VBAP throughput gain for a digital milliwatt and for maximum input/output examples.

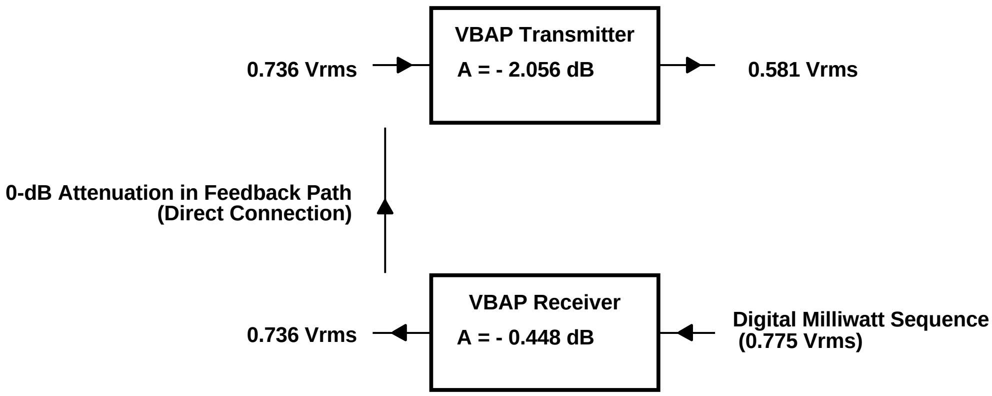
Figure 22. Digital Loopback Channel Gains



Analog Loopback Test and the Associated Gains Through the Transmit and Receive Channels.

The throughput gain of a VBAP in the analog loopback configuration is shown in Figure 23.

Figure 23. Analog Loopback Channel Gains



Application Design Considerations

The following application design considerations are discussed:

- ❑ Power supply signal-to-noise ratio
- ❑ Latch-up conditions
- ❑ Grounding and decoupling
- ❑ Power supply voltage regulator
- ❑ Variable-data rate at master clock frequency
- ❑ VBAP interfaced to a DSP
- ❑ Power-up sequence
- ❑ Power-up delay
- ❑ Typical PCM output expected from a transmit VBAP
- ❑ Audio auxiliary input
- ❑ External speaker

Power Supply Signal-to-Noise Ratio

As with most linear semiconductor devices, the VBAP can be susceptible to noise from the power supply rail. Any noise on the power supply couples directly into the switched-capacitor filters and can be detected on the output of the VBAP. Optimum design technique practices should be followed to reduce the noise on the power supply to a minimum.

The best VBAP signal-to-noise performance can be obtained when the maximum audio input is used. The gain of the microphone amplifier should be adjusted to the maximum audio output of 4 Vpp (to the internal transmit-filter channel) when possible.

Latch-Up Conditions

Latch-up is possible on all CMOS devices such as the VBAP. Latch-up is caused by the firing of a parasitic SCR. Parasitic SCRs are present due to the inherent nature of CMOS. A latch-up condition causes the device to draw excessive amounts of current through one or more pins. The result of latch-up is dependent on the capacity and the series impedance of the power supply. An overcurrent condition during latch-up can permanently damage or destroy the device. The worst case is when the device is damaged, but still partially functional. The device remains in an overcurrent condition until it is turned off and back on again or is destroyed.

To help prevent latch-up conditions, there should be a reverse biased Schottky diode (with a forward voltage drop of less than or equal to 0.4 V) between VDD and GND.

Even though the VBAP is heavily protected against latch-up, it is still possible to cause latch-up under certain conditions. The following can cause a latch-up condition:

- When GND rises momentarily above VDD potential. This can be caused from back EMF if the device is hot inserted.
- If a signal pin is connected after Vcc is connected, but before the ground is connected. This could happen if the device is mounted on a card with an edge connector and inserted with the power on. If there is any chance the VBAP will be used on a card that could be hot inserted, the ground edge connector traces should be made longer than the signal and Vcc connectors. This configuration causes the ground to be connected first.
- If a signal source is connected without the device properly grounded, and a signal source ground occurs through another signal pin. (See the device power-up sequence section for the recommended power-up sequence).

Grounding and Decoupling

For effective grounding and decoupling of the VBAP power supply, the following guidelines apply:

- Use a ground plane on the printed circuit board (PCB). The ground plane should cover as much unused area as possible.
- Digital switching creates high-frequency voltage transients. These voltage transients result in high current consumption. Capacitive loading on the power supply rail helps regulate the supply voltage (install a high-quality 0.1 µF ceramic capacitor directly across the VBAP power supply pins). Ceramic capacitors have a low ESR (equivalent series resistance) or high Q and are well suited to suppress high-frequency voltage transients.
- The VMID generator output VMID is used as a reference voltage by the VBAP internal amplifiers. VMID is developed internally from VDD. Any power supply noise on VMID is normally detected at the output of the VBAP. To reduce output noise on VMID, it is made available at an external pin that provides a means to attach an external filter circuit. The recommended filter circuit uses two external capacitors. The optimum capacitor combination is a 1 µF ceramic in parallel with a 470 pF ceramic chip capacitor (see Figure 2).

Power Supply Voltage Regulator

A voltage regulator is used to reduce noise on the power supply rail, even when using battery power. Batteries have high internal impedance that allows the DC voltage to vary under instantaneous current consumption during digital switching. The resultant change in voltage manifests itself as noise on the power supply rail.

To reduce lower frequency transients, a 10-µF capacitor is used across the power supply rails on the PCB. This serves the same purpose as the ceramic capacitor, except that it responds well to lower frequency transients.

Locate all power supply traces close to the ground plane in order to add parallel capacitance.

Variable Data Rate at Master Clock Frequency

In some applications, it is desirable to run the VBAP in the variable-data rate mode at a data rate equal to the master clock speed. This provides the designer with the advantages of using the variable-data rate mode, such as repeated data while frame sync is high, while still running the maximum data rate. This is the case in the fixed-data-rate mode. In the fixed-data-rate mode, the data clock is run at the master clock speed.

If the device is in the variable-data-rate mode, /DCKLX and MCLK cannot be tied together. If the master clock is used as the /DCKLX, the master clock output must be isolated before connection to /DCKLX. This is because the VBAP always powers up in the fixed-data-rate mode, and for the first several clock cycles, /DCKLX is actually an output (/TSX), as defined in the VBAP data sheet. The output /TSX is a transmit time strobe that pulls MCLK low, which corrupts MCLK if they are common external to the device. Only after the first several master clock cycles does the device assume a variable-data-rate mode and /DCKLX becomes an input.

VBAP Interfaced to a DSP

A more common application for the VBAP is as an interface to a DSP. The VBAP performs the analog-to-digital and digital-to-analog conversions, along with filtering, while the DSP performs more complex functions with the encoded speech. For example, in a cellular telephone application, the DSP would typically perform the equalization and speech coding of the encoded speech through the use of algorithms (code) executed by the DSP. The circuit in Figure 24 illustrates a typical VBAP-to-DSP interface. The fixed-data-rate-mode conversion and variable-data-rate mode conversion timing diagrams are shown in Figure 25 and Figure 26.

Figure 24. VBAP-to-DSP Interface Configuration

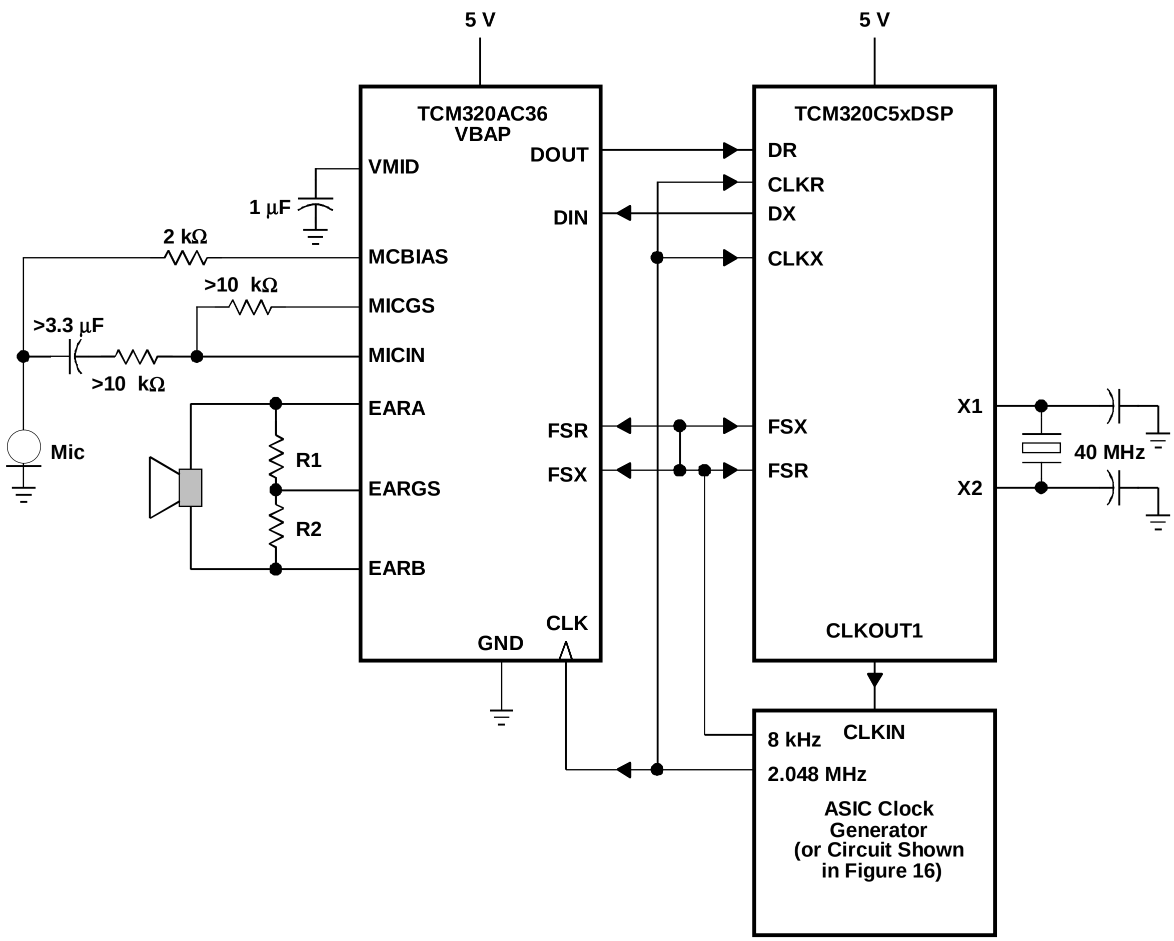
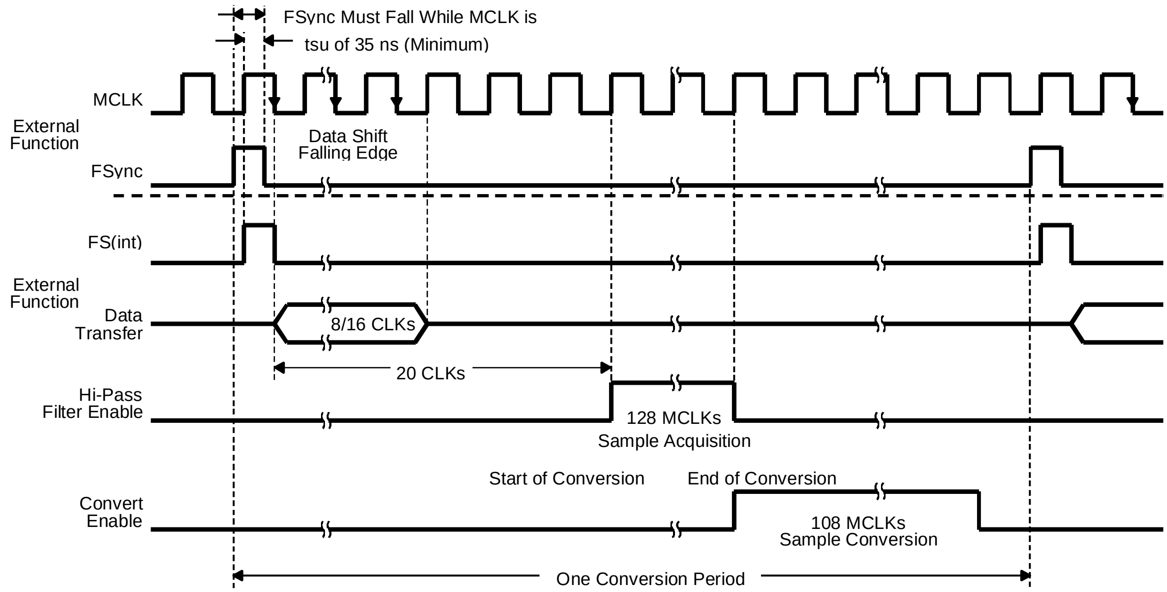
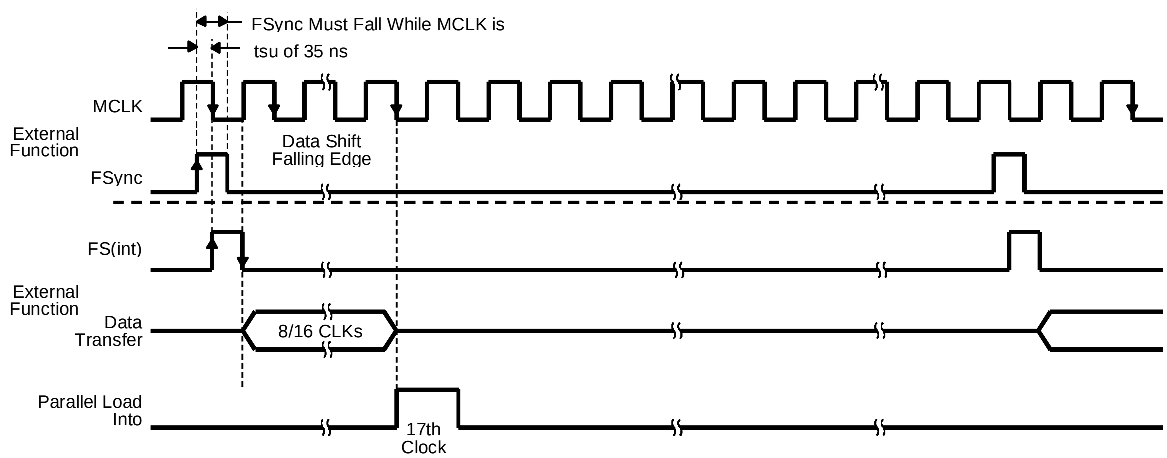


Figure 25. VBAP Fixed-Data-Rate Mode Conversion Timing Diagram

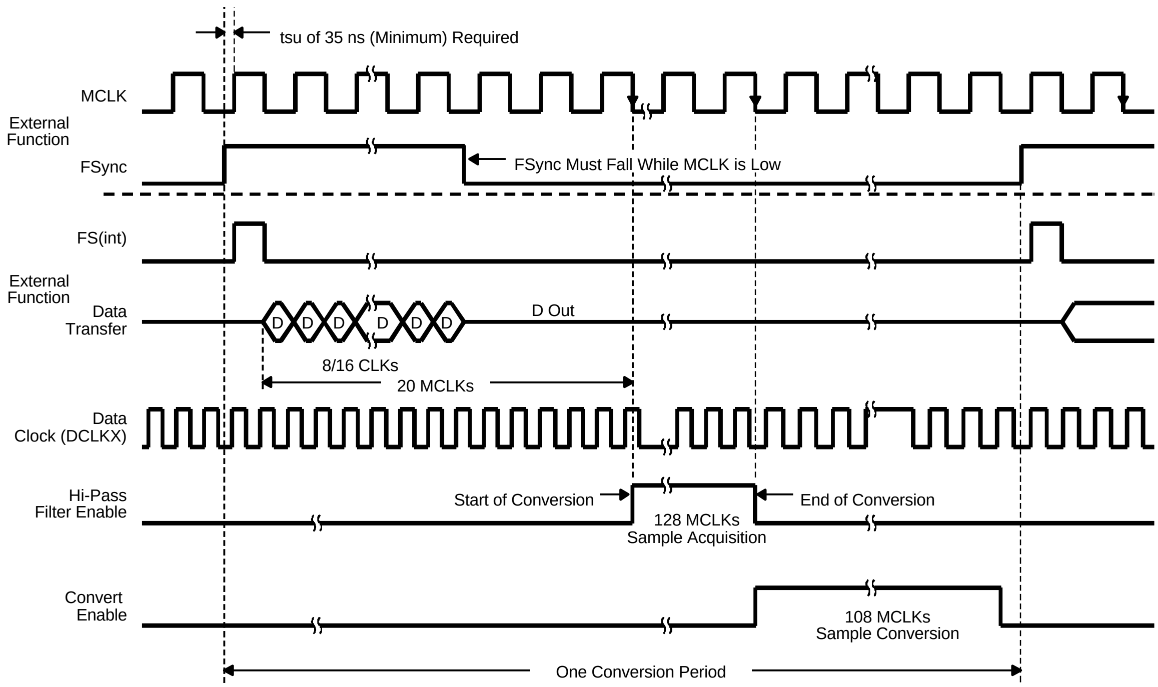


THIS REPRESENTS ONE SAMPLE CONVERSION FOR THE TRANSMIT DIRECTION

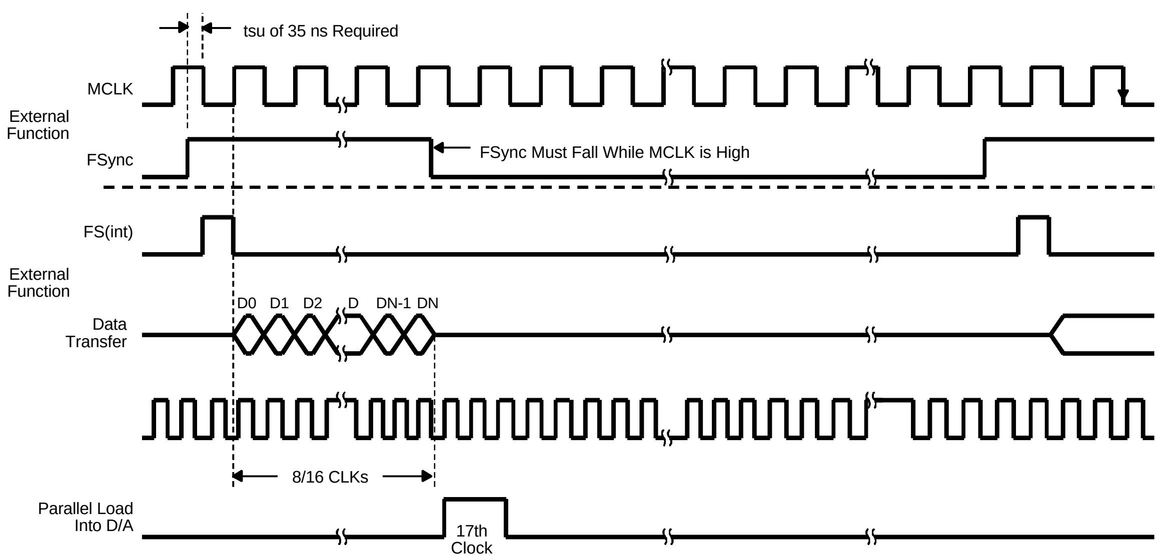


THIS REPRESENTS ONE SAMPLE CONVERSION FOR THE RECEIVE DIRECTION

Figure 26. Variable-Data-Rate Mode Conversion Timing Diagram



THIS REPRESENTS ONE SAMPLE CONVERSION FOR THE TRANSMIT DIRECTION (MICIN TO DOUT)



THIS REPRESENTS ONE SAMPLE CONVERSION FOR THE RECEIVE DIRECTION

Power-Up Sequence

To ensure proper operation of the VBAP, and as a safeguard against latch-up, it is recommended that Schottky diodes with forward voltages less than or equal to 0.4 V be connected from GND to V_{CC}, and that the following power-up sequence is always used:

1) Apply GND
2) Apply V_{DD}
3) Apply low to /PDN
4) Connect master clock
5) Connect Data clock (if used)
6) Remove low to /PDN
7) Apply FSX and/or FSR synchronization pulses

NOTE:
Input signals should not be applied until after the power-up sequence is completed.

Power-Up Delay

After power up or the application of V_{DD}, DOUT and /TSX are held in the high impedance state for approximately four frames (500 µs for an 8 kHz frame sync). The analog circuits in the transmit channel require approximately 60 ms to reach an equilibrium value. DOUT and /TSX can become unstable after any interruption of CLK.

Typical PCM Output Expected from a Transmit VBAP

In an ideal situation, the VBAP 8 and 13 bit A/D converters are designed with a noise floor that equates to the transition of one-half the LSB. In the linear mode, one-half bit represents approximately -75 dB:

$$20 \times \log\left(\frac{2^{0.5}}{2^{13}}\right) = -75\ \text{dB}$$

This corresponds to the VBAP data sheet, which specifies the transmit noise in linear mode to be -74 dB. Using a VBAP in the receive mode, configured for a maximum output signal of 4 Vpp, the VBAP encodes this one-half bit of noise and experience about 250 µVrms of noise on the speaker output pins:

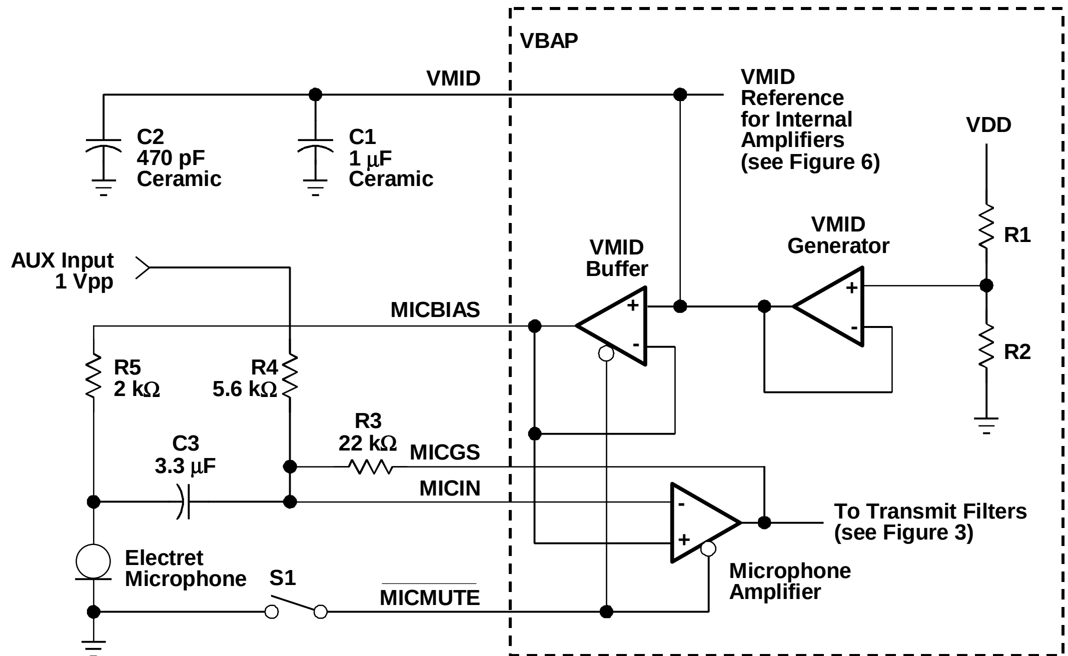
$$-75\ \text{dB} = 20 \times \log \frac{X}{1.414\ \text{Vrms}}$$

where X = output that is 75 dB down from 1.414 Vrms
X = 250 µVrms
4 V_{pp} = 1.414 Vrms

Audio Auxiliary Input

An audio auxiliary input can be added to the VBAP, as shown in Figure 27. A typical auxiliary, or AUX signal, is 1 Vpp. The maximum PCM output from the VBAP occurs when the microphone amplifier gain is adjusted so that the input to the internal transmit filter is 4 Vpp (which is where you can expect the best signal-to-noise ratio, therefore, a gain of 4 is required. Figure 27 shows the external circuitry required for a VBAP configured with a microphone and AUX input.

Figure 27. VBAP Configured with AUX and Microphone Input



External Speaker

The VBAP drives piezo speakers more efficiently than other types of speakers. Piezo speakers are highly capacitive, high-impedance voltage driven devices typically used in hand held communicators. The VBAP is specified and tested to drive 600 Ω loads. Although laboratory characterization has shown that it can drive loads as low as 50 Ω, the VBAP is not guaranteed to meet all parametric specifications with loads lower than 600 Ω.

SEB

The system emulation board (SEB) provides an aid for the design, development, testing, and debugging of communication equipment. The design of the SEB input and output sections emulates typical voice communication systems design practices. The SEB allows the designer to:

- Manipulate clock phases and synchronization
- Manipulate frame synch pulse width and timing
- Manipulate setup configuration
- Monitor all analog and digital data signals
- Employ an external or internal system clock
- Use single or dual VBAPs
- Use full and reduced power modes

SEB Configuration

The SEB provides numerous custom configuration settings. These settings allow the designer to emulate end-product functionality in the early design phase. SEB component placement is shown in Figure 30. The SEB parts are listed in Tables 16 and 17.

Table 7 provides VBAP initialization switch settings. External clock selection is shown in Table 8. System clock source/polarity and data mode/rate select switch settings are shown in Table 9. The PCM data flow direction switches are described in Table 10. Audio input select switch configurations are listed in Table 11. Table 12 describes external connectors. Table 13 lists the SEB jumpers and their functions. The variable resistor functions are listed in Table 14. Table 15 contains count data settings for U3 and U5.

Table 7. VBAP Initialization Switch Settings for DS1 (U1) and DS3 (U2)

DSn Switch	Signal	Open	Closed
1	FSX	External Source	Internal Source (D)
2	FSR	External Source	Internal Source (D)
3	DCKLX	Open (D)	Internal Source
4	DCLKR	Pulled Up (D)	Internal Source
5	EARMUTE	Speaker Amplifier Circuit Enabled (D)	Speaker Amplifier Circuit Disabled
6	/LINSEL	Companded Mode Selected	Linear Mode Selected (D)
7	/MICMUTE	Microphone Amplifier Circuit Enabled (D)	Microphone Amplifier Circuit Disabled
8	/PDN	Power Down Mode Disabled (D)	Power Down Mode Enabled

Note: D = Default

Table 8. External Timing Select Switch (DS2)

DS2-	Signal	Open (Default)	Closed
1	DCLKR (U2)	On-board Oscillator U10 Selected	External Clock Selected (J13)
2	/DCKLX (U2)	On-board Oscillator U10 Selected	External Clock Selected (J13)
3	FSR (U2)	On-board Oscillator U10 Selected	External Clock Selected (J13)
4	FSX (U2)	On-board Oscillator U10 Selected	External Clock Selected (J13)
5	FSX (U1)	On-board Oscillator U10 Selected	External Clock Selected (J13)
6	FSR (U1)	On-board Oscillator U10 Selected	External Clock Selected (J13)
7	/DCKLX (U1)	On-board Oscillator U10 Selected	External Clock Selected (J13)
8	DCLKR (U1)	On-board Oscillator U10 Selected	External Clock Selected (J13)

Table 9. System Clock Source/Polarity and Data Mode/Rate Select Switches

Switch	Function	Position 1	Position 2
S6	System Clock (CLK) source for U1 and U2	Internal Oscillator	External Clock
S7	System Clock source for SEB counter circuits	Internal Oscillator	External Clock
S8	System Clock (CLK) polarity select for U1	True	Inverted
S9	System Clock (CLK) polarity select for U2	True	Inverted
S10	Data Mode Select	Linear	Companded
S11	Data Rate Select	Fixed	Variable

Table 10. PCM Data Flow Direction Switches

Switch	Function	Open	Closed
S2	U1 Local Loop-back Test	Test Disabled	Test Enabled
S3	Connects U1 DOUT to U2 DIN	VBAPs Disconnected	VBAPs Connected
S5	U2 Local Loop-back Test	Disabled	Enabled

Table 11. Audio Input Select Switches (S1 and S4)

Switch	Function	Position 1	Position 2
S1	Audio Source Select For U1	Auxiliary Input (J2)	Electret Microphone Input (J1)
S4	Audio Source Select For U2	Auxiliary Input (J8)	Electret Microphone Input (J7)

Table 12. External Connectors

Connector	Description
J1	Electret microphone input to VBAP (U1)
J2	Auxiliary input to VBAP (U1)
J3	PCM data input to VBAP (U1)
J4	Audio differential output (U1)
J5	Audio output (U1)
J6	PCM out (U1)
J7	Electret microphone input to VBAP (U2)
J8	Auxiliary input to VBAP (U2)
J9	PCM data input to VBAP (U2)
J10	Audio differential output (U2)
J11	Audio output (U2)
J12	PCM out (U2)
J13	External FSR, FSX, /DCKLX or DCLKR source
J14	External system clock input
J15	External 9-12 VDC power supply input
J16	External 5 VDC power supply input
J17	SEB 5 VDC ground input

Table 13. Jumpers

Jumper	Installed	Not Installed
JP1	Connects voltage regulator VR1 to SEB V_{cc}	Disconnects voltage regulator VR1 from SEB V_{cc}
JP2	Connects V_{cc} to U1	Allows for loop insertion to measure I_{dd} to U1
JP3	Connects V_{cc} to U2	Allows for loop insertion to measure I_{dd} to U2

Table 14. Variable Resistor Adjustments

Resistor	Description
R1	Adjust bias voltage to microphone at J1
R3	Gain adjustment for U1 audio input
R5	Gain adjustment for U1 audio output
R6	Adjust bias voltage to microphone at J7
R10	Gain adjustment for U2 audio input
R12	Gain adjustment for U2 audio output

Table 15. U3 and U5 Counters Set-Up (DS4)

DS4-	Function
1	Frame length counter (B0) LSB
2	Frame length counter (B1)
3	Frame length counter (B2)
4	Frame length counter (B3) MSB
5	Data clock counter (B0) LSB
6	Data clock counter (B1)
7	Data clock counter (B2)
8	Data clock counter (B3) LSB

System Clock and Data Rate Modes

The transmit and receive frame sync as well as the data clock are derived from the system clock. A counter chain of four, 4 bit counters (U3, U4, U5, and U6) are used to develop SEB timing.

Both counter pairs (U3/U4 and U5/U6) are configured to permit variations in count length. These variations allow the user to duplicate system level problems. Dip switch DS4 is used to define the preload for the lower four bits of these counters. Switches DS4-1 through DS4-4 are used with the word length counters to allow the manipulation of the length of the frame synch pulse in variable-data rate-modes (linear and companded). DS4-4 is the least significant bit (LSB) in the counter preload. Switches DS4-5 through DS4-8 are used to modify the data clock rate by changing the divide down of the system clock**.** Modifying the data clock rate also affects the frame sync when operating in the fixed frame length mode; DS4-8 is the LSB in the counter preload. Table 15 lists the functions of dip switches DS4-1 through DS4-8. Switches DS4-1 through DS4-4 provide counter data for U5. Switches DS4-5 through DS4-8 provide counter data for U3.

System Clock

The system clock provides the timing for both VBAPs and the SEB support circuitry. The system clock can be generated externally and input to the SEB at J14 (see Figure 28) or taken from an on-board 2.048 MHz oscillator (U10).

Switches S6, S7, S8, and S9 allow the system developer to configure system clock distribution to simulate end product configuration and the effects of line length, which causes skewing of, clock synchronization. See Table 9 and Figures 28 and 29 for more information about system clock distribution.

Data Rate Modes

Data rate switch S11 selects the SEB data rate mode of operation. The SEB can transfer data in either the fixed or variable-data-rate modes. Data transfers in the fixed-data-rate mode are either 8 or 16 bits in length. The variable-data-rate mode can transfer linear or companded data words. Data word size is determined as a function of whether linear or companded is selected by the data mode switch S10. The linear mode uses a 16-bit word, the first 13 bits are data and the last 3 bits represent the volume level. The companded mode uses an 8-bit data word. In both modes, the most significant bit (MSB) is the sign bit followed by the resulting data pattern. In the variable frame length mode, frame sync (FSX/FSR) is only high during data transfer time. Transfer time is 8 data clock periods for the companded data mode and 16 data clock periods in the fixed frame length mode. The signal DOUT is three-stated during the second 8 data clock periods while operating in the variable frame length mode.

The first counter (U3) generates the data clock at one-fourth of the system clock frequency (2.048 MHz / 4 = 512 kHz). The count length of U3 can be manipulated by DS4-5 through DS4-8. The ripple-carry of U3 gates the second counter (U4) to generate the frame sync pulse (when operating in the fixed-data-rate mode) at a count length of 256 counts. This equates to a frequency of 2.048 MHz/256 = 8 kHz.

Fixed Data Rate Operation

In the fixed-data-rate mode, the counters U3 and U4 RCO outputs are NANDed at U7A to produce the Frame Sync (FSX/FSR) pulse. This logical operation eliminates the cascaded RCO glitch. The pulse is routed to both VBAPs through S11.

Variable Data Rate Operation

In the variable-data-rate mode the second counter pair (U5/U6) generates the frame sync pulse. The first counter pair (U3/U4) frame sync pulse output, at U7A pin 3, clears the second counter pair (U5/U6), insuring time slot compliance. The count length of the second counter pair determines the frame data output time and the timing for both the linear and companded data rate mode frame sync pulses. The data mode is selected by switch S10. The counters, U5 and U6, divide the data clock by 64 (companding mode) or 128 (linear mode). The counter chain is also pre-loadable for manipulation of the count length by DS4-1 to DS4-4.

To allow design flexibility, the frame sync pulse can originate from either an on or off board source. The on board frame sync pulse is routed to VBAP U1 through DS1-1 and DS1-2 and VBAP U2 through DS3-1 and DS3-2. The off board pulse enters the SEB at J13.

Table 15 lists the DS4 switches and their functions. The switches DS4-1 to DS4-4 are used to set the maximum length of the frame sync pulse in the variable rate mode. The switches control the frame length count to counter U5. The default count length is data clock/count. The range is 0/data clock to 15/data clock. The switches DS4-5 to DS4-8 are used to set the data clock rate. The switches control the count to U3. The data clock rate is system clock/count. The range is system clock/n; where n is 4, 8, 12, 16, 20, 24, 28, 32, 36, 40, 44, 48, 52, 56, 60, or 64.

Audio Input Signals

The SEB has audio input connectors and support circuitry for two VBAPs (U1/U2). The connectors provide an electret microphone and an auxiliary audio input for each VBAP, J1/J2 for U1 and J7/J8 for U2. Variable resistors R1 and R3 are used to adjust the audio input to U1. Variable resistors R6 and R10 are used to adjust the audio inputs to U2. Switches S1 and S4 are used to select the audio input source for U1 and U2, respectively.

NOTE:

Audio input signal waveforms must conform to the input specifications of the VBAP data sheet.

When an electret microphone is used, the VBAP sources the required bias current. This bias current is adjusted for optimum signal levels by variable resistors R1 for U1 and R6 for U2. The VBAP provides optimum signal encoding when the inputs are adjusted for unity gain by comparing the signal MICGS with respect to the signal source. This gain adjustment is accomplished using variable resistors R3 and R10. When adjusted for unity gain, the maximum input signal level is 4 V P-to-P.

External Speaker Amplifier Circuits

The VBAP output can be routed to a speaker through an external circuit. There are two types of circuit configurations: differential- and single-ended gain. The differential-gain circuit determines the gain of the VBAP internal speaker-amplifier circuit. The differential-gain circuit is composed of a resistor network. The value and configuration of the resistors determine the VBAP speaker-amplifier-circuit gain. The single-ended circuit configuration has fixed external gain.

Differential-Gain Configurations

The differential-gain circuit configuration determines the VBAP speaker-amplifier circuit gain. The gain is set using variable resistors R5 for U1 and R12 for U2. These levels are set according to user requirements.

Single-Ended Gain Configuration

When the end-equipment requires a single-ended configuration, set variable resistors R5 and R12 to 0 ohms. This effectively shorts pin 3 (EARB) and pin 4 (EARGS)

Setup and Testing Configurations

This section contains VBAP and SEB configuration and test information.

Standard VBAP Configuration Procedure

Follow the procedure below to configure VBAP U1 for optimum operation:

1) Set DS2-1 through DS2-8 to open.
2) Set DS4-1 through DS4-8 to closed.
3) Set DS1-1 through DS1-4 and DS3-1 through DS3-4 to closed.
4) Set DS1-5 through DS1-8 and DS3-5 through DS3-8 to open.
5) Set switch S1 to connect the intended audio source at either J1 or J2.
6) Set S2 to enable local loopback mode.
7) Input an analog signal into the VBAP at J1 or J2.
8) Adjust variable resistor R3 for 3.0 V P-to-P at U1 pin 19.
9) Observe the waveform at U1 pin 2 or 3. Adjust variable resistor R5 to approximately half the P-to-P waveform amplitude on pin 19.

This procedure can be repeated for VBAP U2. This procedure will hold true regardless of the compression mode or data rate.

Custom VBAP Configurations

- To operate in the linear mode, close switch position DS1-6 for U1 and DS3-6 for U2.

- To mute the microphone inputs of U1 and U2, close DS1-7 and DS3-7 respectively.
- To mute the speaker outputs of U1 and U2, close DS1-5 and DS3-5 respectively.
- To place the VBAPs in the power-down mode, close DS1-8 for U1 and DS3-8 for U2.
- The VBAPs can be placed in the standby mode by closing DS1-1 and DS1-2 for U1 and DS3-1 and DS3-2 for U2.
- If only the transmit function is required, close DS1-1 and open DS1-2 for U1 or close DS3-1 and open DS3-2 for U2.
- If only the receive function is required, open DS1-1 and close DS1-2 for U1 or open DS3-1 and close DS3-2 for U2.
- The system clock can be configured to operate in or out of phase with the VBAP clock input CLK. System clock phasing is controlled by S8 for U1 and S9 for U2.

System Level SEB Configuration

- The data clock and frame synch generation circuits are shared by both VBAPs. Each VBAP must be configured to function in the same mode.
- To operate in the fixed-data-rate mode, open position DS1-5 for U1 or DS3-5 for U2. This places the DCLKR input pin of each respective VBAP at a fixed logic high.
- To apply frame synch pulses to the respective VBAPs, close DS1-1 and DS1-2 for U1 and DS3-1 and DS3-2 for U2. Switch S11 must be set to the fixed-data-rate mode to establish correct pulse synchronization and duty cycle.
- To operate in the variable-data-rate mode, open DS1-1 and DS1-2 for U1 and DS3-1 and DS3-2 for U2.
- To select SEB linear or companded encoding and decoding, use S10. To select VBAP companded or linear mode use, DS1-6 for U1 and DS3-6 for U2.

I_{dd} Measurement

The SEB was designed to allow as much design flexibility as practical. An additional feature allows for the measurement of the I_{dd} for each VBAP while still maintaining circuit integrity. Jumpers JP2 or JP3 can be removed and replaced with wire loops for the purpose of measuring the current at each VBAP under the desired set of conditions.

Basic Single VBAP Operation

Each of the VBAPs are capable of independent operation. The simplest SEB configuration requires an audio source, speaker, and power supply. To accomplish this for VBAP U1:

- Connect the audio input to J1 or J2
- Set S1 to the corresponding input connector
- Connect a speaker to J4 or J5 (to monitor the output signal)

In this configuration, J6 can be used to monitor the PCM data from VBAP U1. Connector J3 provides a PCM data direct input to VBAP U1.

The VBAP U2 is also capable of independent operation using J7, J8, S4, J10, J11, J12, and J9.

The system clock can be supplied from an external source using connector J14. This input is buffered and represents a single SN74HCxx load with a 51 ohm termination.

If it becomes desirable to input or output PCM data through the VBAPs, for VBAP U1, the input is J3 and the output is J6. For VBAP U2 the input is on J9 and the output is J12. These connectors are not buffered or terminated, but are connected directly to the VBAPs.

Connectors P1 and P2 provide an interface between the SEB an external digital circuitry.

Figure 28. SEB Schematic (sheet 1 of 2)

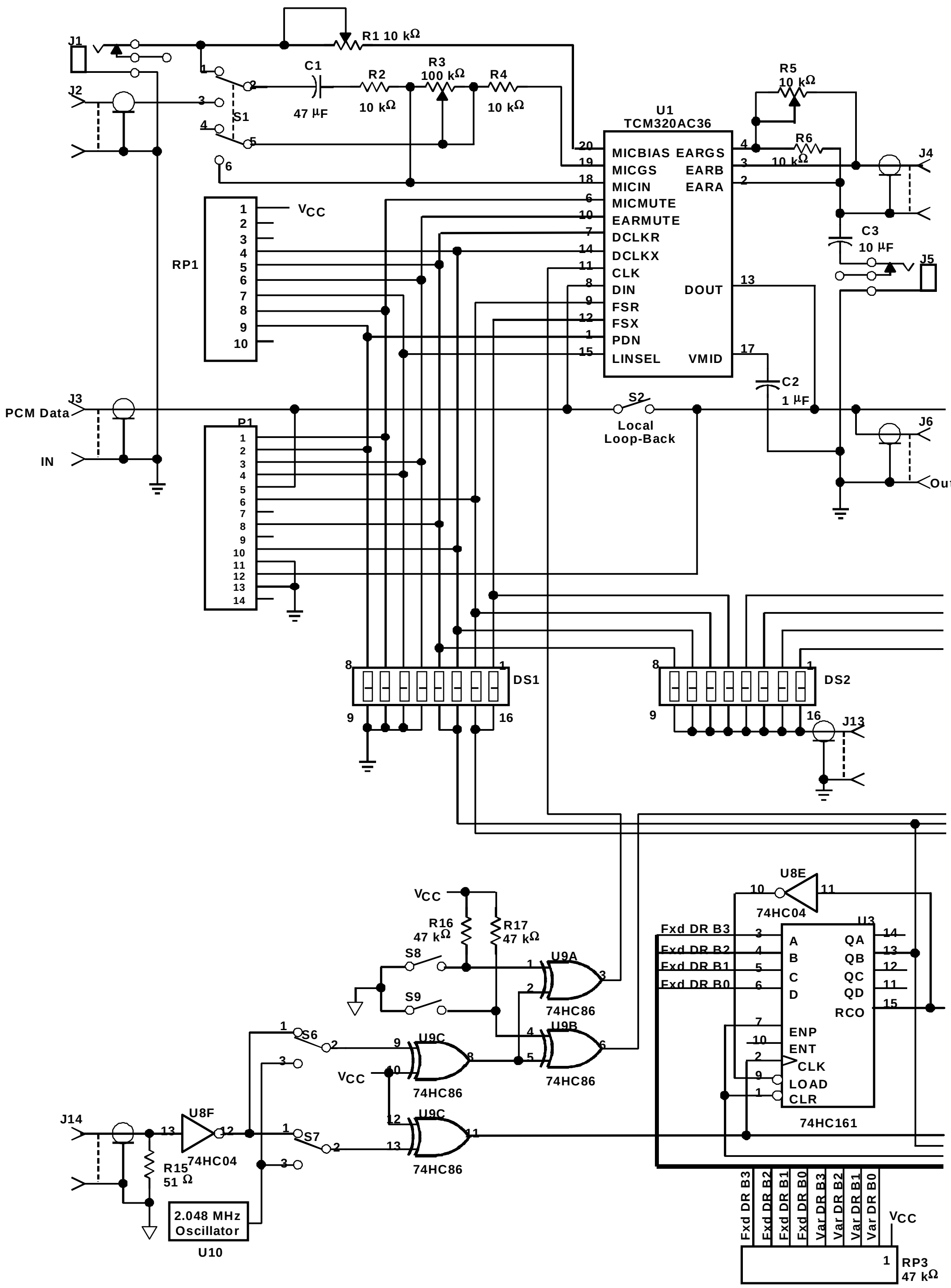


Figure 29. SEB Schematic (sheet 2 of 2)

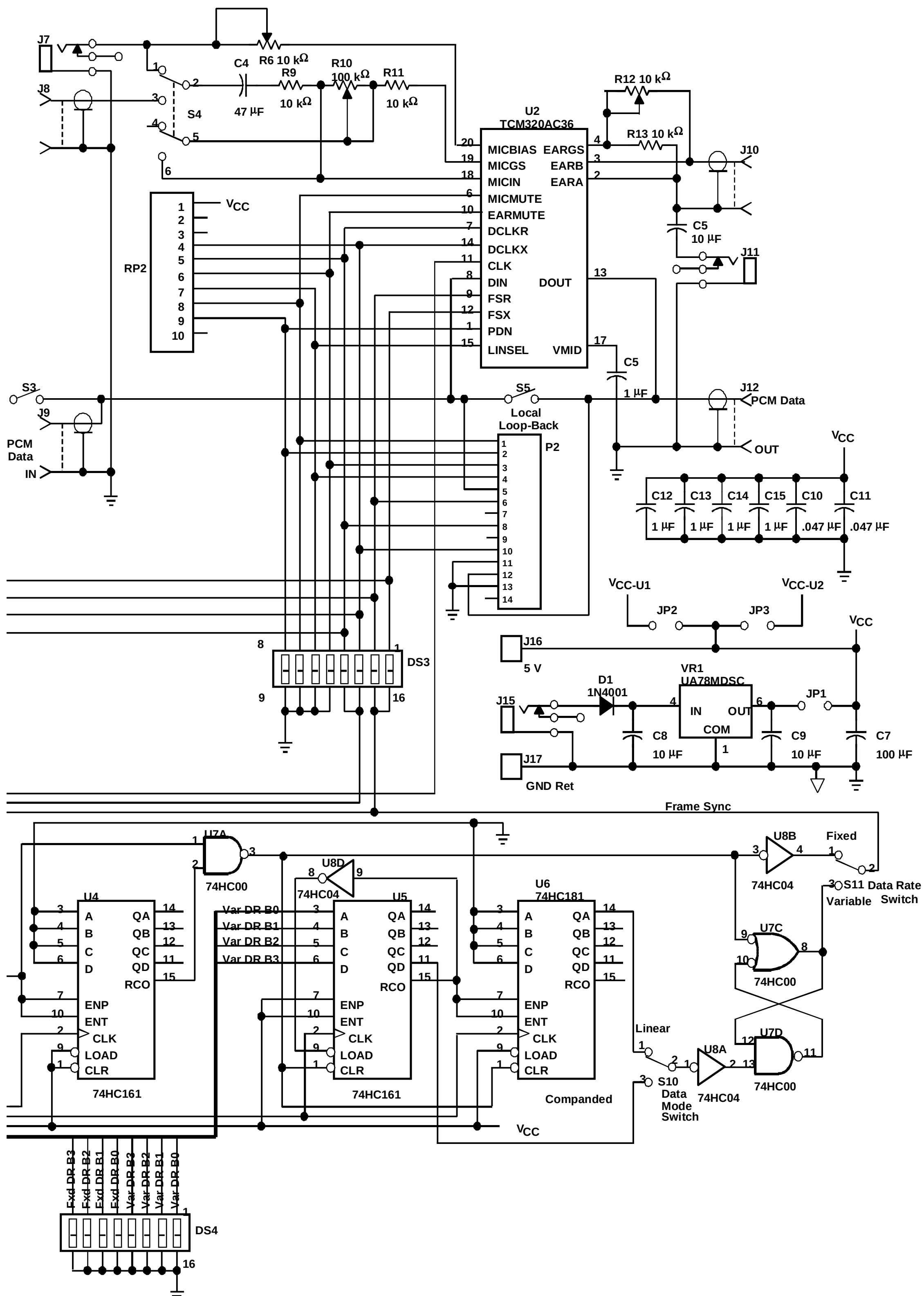


Figure 30. SEB Component Placement

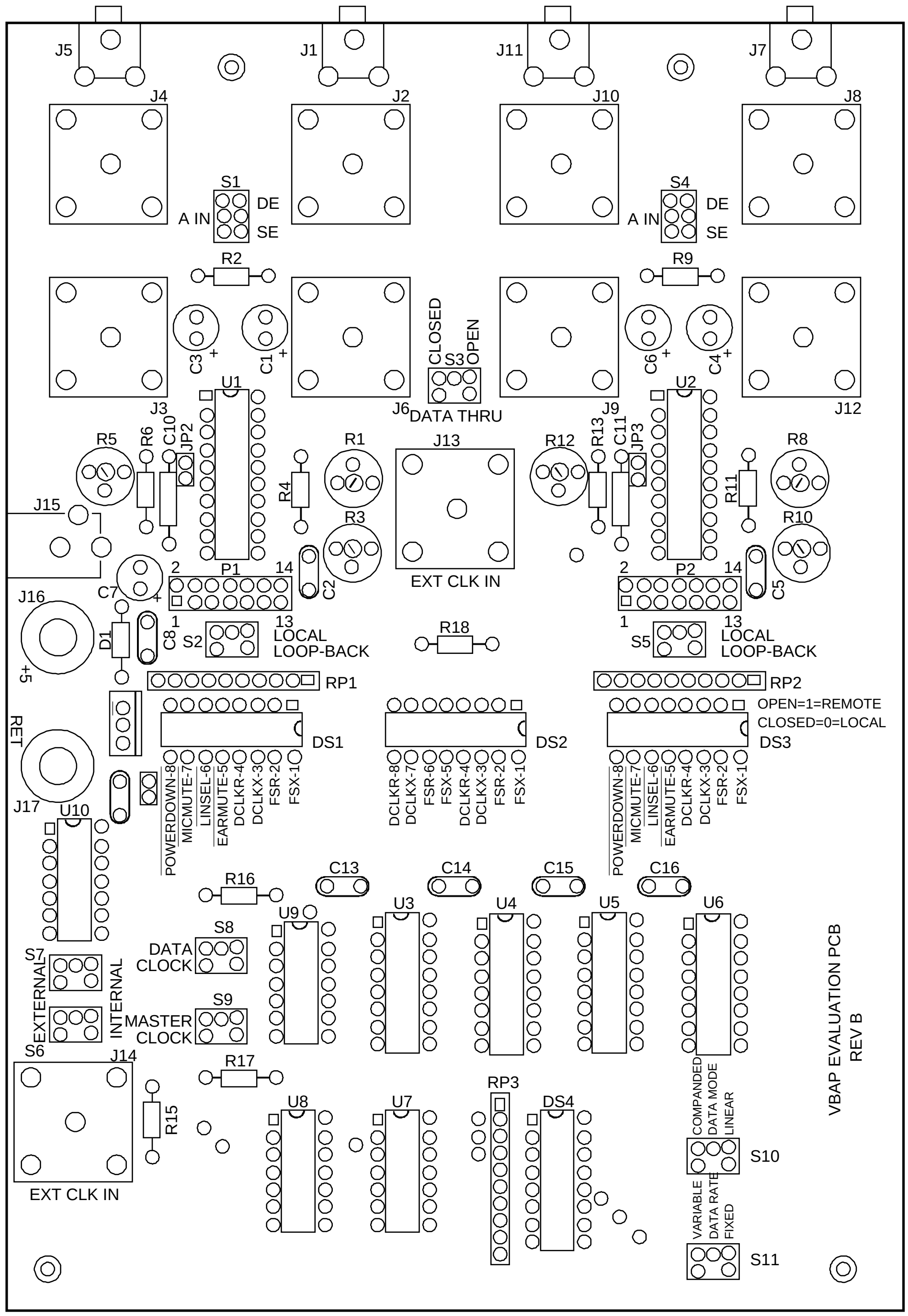


Table 16. SEB Parts List

Part	Description	Style	Qty.	Reference Designator
PCB			1	
Capacitors	47µF		2	C1, C4
	10µF		2	C3, C6
	1.0µF	CK06	4	C2, C5, C8, C9
	100µF		1	C7
	0.047µF	X7R dielectric	2	C10, C11
	0.1µF	CK06	4	C12, C13, C14, C15
Connectors	CC MINI JACK		4	J1,J5,J7,J11
	BNC		10	J2,J3,J4,J6,J8,J9,J10,J12,J13,J14
	Power		1	J15
	Banana-Jack(Red)		1	J16
	Banana-Jack(Blk)		1	J17
	7x2 berg-pins		2	P1,P2
	1x2 berg-pins		3	JP1,2,3
	Jumper		3	
Diodes	1N4001		1	D1
DIP-Switches	8-POS raised toggle		4	DS1-4
Integrated Circuits				
For 5 V build	SN74HC00N	N-PKG	1	U7
	SN74HC04N	N-PKG	1	U8
	SN74HC86N	N-PKG	1	U9
	SN74HC161N	N-PKG	4	U3-U6
	TCM320AC36CN	N-PKG	2	U1, U2

Table 17. SEB Parts List (continued)

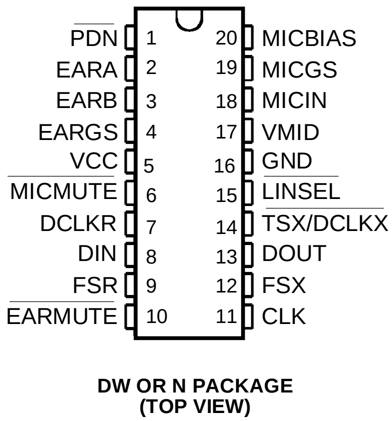
Part	Description	Style	Qty.	Reference Designator
	uA78M05	TO-220	1	VR1
Oscillator				
5 V part	2.048 MHz Osc	SG51	1	U10
Resistors	51Ω, 1/8 or 1/4w, 10%	RC07	2	R15, R18
	10KΩ, 1/8 or 1/4w, 10%	RC07	6	R2, R4, R6, R9, R11, R13
	47KΩ, 1/8 or 1/4w, 10%	RC07	2	R16, R17
Resistor Pak	10-Pin, 47k Ω	SIP	3	RP1,RP2,RP3
Resistors, Variable	10kΩ	5-mm	4	R1, R5, R8, R12
	100kΩ	5-mm	2	R3, R10
Sockets, optional	14-pin IC		4	U7-U10
	16-pin IC		4	U3-U6
	20-pin IC		2	U1,U2
Switches	DPDT toggle		2	S1, S4
	SPDT toggle		9	S2, S3, S5, S6, S7, S8, S9, S10, S11

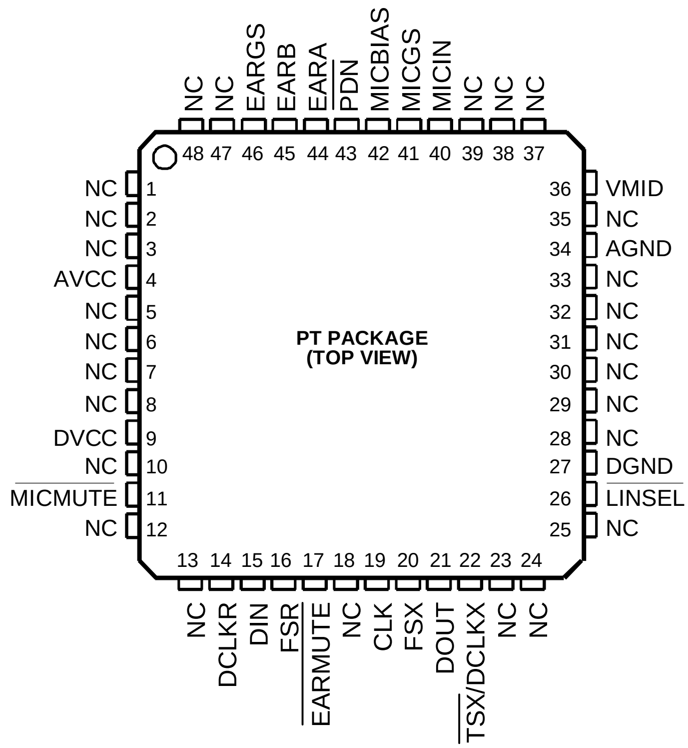
Summary

The voice band audio processor (VBAP) provides a bidirectional interface between analog devices, such as microphones and speakers, and digital system processors. While the information contained in this document relates to the entire VBAP family, it deals more specifically with the TCM320AC36, the 5 V, 2.048 MHz version. This report describes VBAP features, internal circuit functions, principles of operation, data-rate modes, test procedures, circuit-gain analysis, and chip packaging specifications.

Appendix A. Packaging

Figure 31. DW, N, and PT Package Pinout/Signal Name





NC - No internal connection