Application Report
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Junction Temperature of TRF1123/TRF1223 and Recommended PCB Layout Guidelines

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ABSTRACT

The reliability of a semiconductor is determined by the junction temperature, which in turn is dependent on several factors including device layout and mounting, package thermal resistance, PCB layout, heat sink interface, and ambient operating temperature. This application note describes PCB layout guidelines for the best thermal performance and reports on junction temperature measurements of the TRF1123 and the TRF1223. Finally, the failure rate of the TRF1123 and the TRF1223 are calculated using measured junction temperatures and known reliability data for the MESFET process.

The TRF1123 and TRF1223 are GaAs Monolithic Integrated Circuit MMICs packaged in a low-cost, 5 mm x 5 mm, 32-lead leadless plastic chip carrier (LPCC) package. The package has an 8 mil thick copper base (paddle) that extends through the bottom of the package. The package is designed to solder reflow the paddle to a ground pad on the PCB so that a low thermal resistance and excellent RF performance is achieved. The die is attached to the copper paddle using high thermal conductivity silver epoxy: Ablestik Ablebond 84-1 LMIS. The epoxy thickness is kept to a minimum. For the junction temperature test, the die are mounted in packages which have the tops removed so that the surface of the die is visible for infrared temperature measurement.

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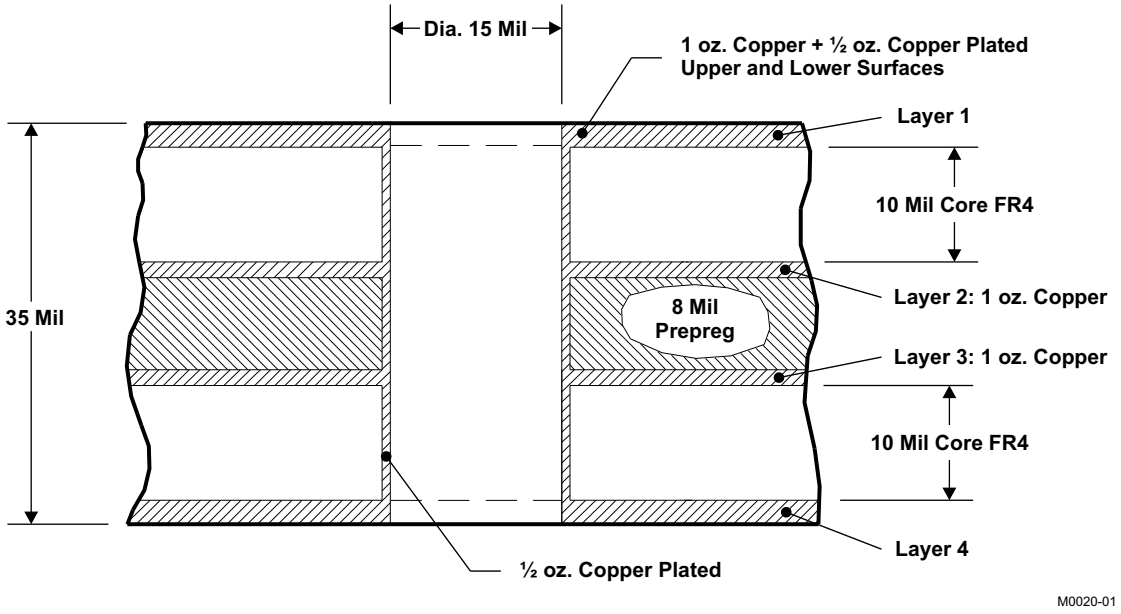
1 PCB Layout and Heatsink Interface

Layout of the PCB is critical to thermal and RF performance. It is extremely important to consider the heat source and how the heat will be removed before completing the electromechanical design. For most applications, the TRF1123 and TRF1223 are mounted in outdoor, environmentally sealed housings and heat removal is by conduction only. There is no internal air flow and consequently heat flow is entirely through the package paddle, through the mounting PCB, and then ultimately through a metal heatsink to ambient temperature. For this configuration, the lowest thermal resistance would be achieved using the minimum number of and thinnest PCB layers using the thickest copper possible. Practical PCB layout requires four layers for trace routing and shielding. Texas Instruments recommends the PCB cross section shown in Figure 1. This configuration is achieved by starting with two 10 mil thick cores of FR4 with 1-oz copper (1.4 mils thick) on each side. (Note: alternative PCB materials such as Park Nelco N4000-13 may be used for circuits that require precise dielectric constant.) The 1-oz copper aids in heat spreading and is thin enough to allow precision etch of most microwave structures. Texas Instruments recommends the thickest copper possible for all layers. Plating with additional copper improves thermal performance but the final copper thickness must be balanced with cost and minimum circuit geometry on the PCB. Layer 1 is the top layer, layer 2 is a RF ground layer, layer 3 is trace route layer, and layer 4 is a ground layer. The final PCB is made by bonding the two starting cores using an 8 mil thick prepreg. A 1/2 oz of copper is plated to connect vias and a final finish plate of white immersion tin is recommended for solder ability while maintaining flat surface.



NOTE: Top and bottom sursface finish: copper flash with 50-70µin white tin immersion

Figure 1. PCB Cross Section and Via Hole Dimensions

The copper pad on layer 1 should be the same dimensions as the copper paddle on the LPCC package. A copper pad on each layer under the LPCC paddle is required to increase heat spreading The pad on layers 2, 3, and 4 should be as large as possible and include the whole layer if possible. To aid heat flow through the PCB the pad under the paddle has a minimum of 25 via holes that are connected to the pads on all layers as shown in Figure 1. It is important not to use *thermal relief* vias or remove copper around the via connections to each layer.

The leads and paddle surfaces on the LPCC package are planar and require a flat PCB surface for proper solder reflow. For example, there must not be any solder mask on the ground pad (on layer 1) that lifts the LPCC package up and impact solder reflow. The solder mask is typically generated in an automatic fashion and solder mask will be present on the leads that are connected to ground or tied together. The solder mask must be manually removed in these cases before gerber file generation otherwise the solder mask will be present on the fabricated boards.

There should not be any solder mask on the bottom side of the PCB (layer 4) that is attached to a heat sink. Any solder mask here impedes heat flow and increase thermal resistance. Blind vias may be used to prevent trace interconnects from extending through to layer 4 or spot reliefs in the metal housing may be used to prevent trace interconnects from shorting to the heatsink case.

Screws that clamp the PCB to the heat sink should be located as close as possible to the LPCC package. In our case, we use 4 #2-56 screws separated by 0.6” surround the TRF1223/TRF1223. Additional screws hold the 4” x 4” PCB to an aluminum heatsink.

A thin layer of heat sink compound should be applied to the bottom of the PCB (under the LPPC heat source) before the PCB is attached to the heatsink.

2 Junction Temperature Measurements

The junction temperature of Texas Instruments power MMICs TRF1223 and TRF1123 were measured using a infrared microscope when the packaged devices were mounted on a 4” x 4” PCB and attached to a metal heatsink simulating actual operating conditions.

A cross section of the TRF1123 and TRF1223 when mounted as described above is shown in Figure 2. In this configuration all heat flow is through the copper paddle on the bottom of the LPCC package, through the PCB and into the aluminum (Al) heatsink.

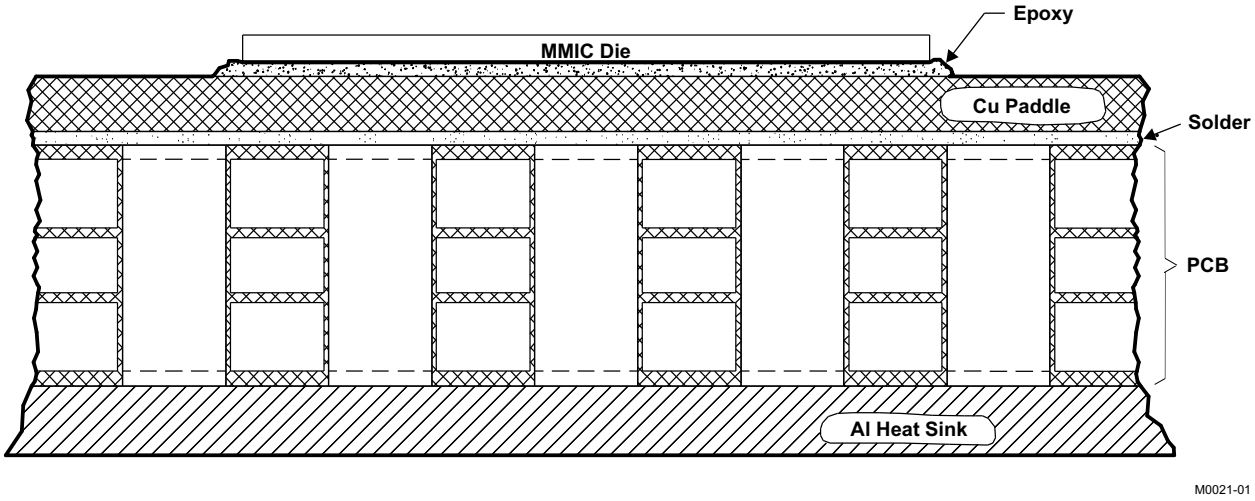


Figure 2. Cross Section of the TRF1123 and TRF1223, PCB and Mounting Interface

The PCB layout for the TRF1223 is shown in Figure 3 for the measurements. The layout for the TRF1123 is similar and can be found in the data sheet for the TRF1123. The PCB is attached to an aluminum heat sink with screws. A thin layer of heat sink compound was used at the mating surface of the PCB to the aluminum base. In a typical application the aluminum base would be a heat sink and maintained at an ambient temperature.

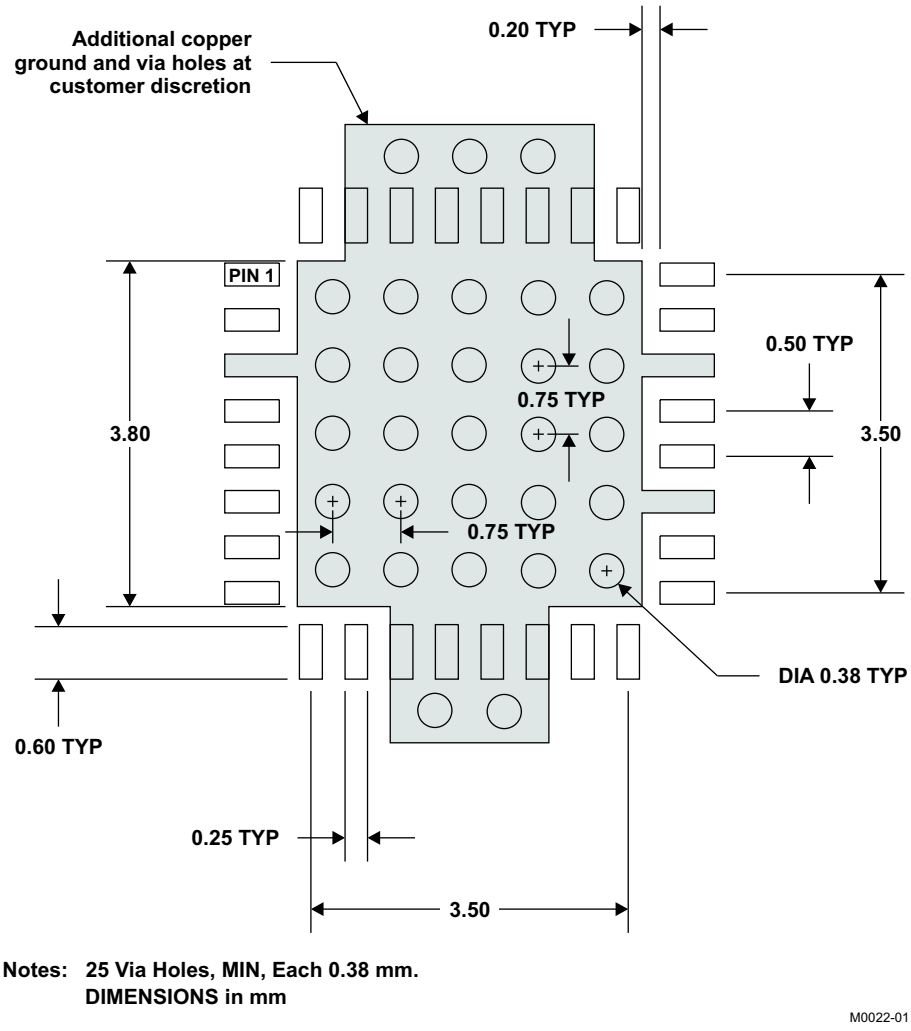


Figure 3. Layout for TRF1223

For our device measurements, infrared microscope imaging was used at high resolutions to find the peak channel temperature. For these junction (channel) temperature measurements the baseplate is maintained at approximately 85°C so that the emissivity of the device could be determined without any power dissipation. The exact base plate temperature was monitored and recorded before each measurement and used in the final thermal resistance calculations. For both the TRF1123 and the TRF1223, the measurements were made with all amplifier stages biased to normal operating levels, with no RF applied and the highest device temperature was recorded along with power dissipation of each stage. For both the TRF1123 and TRF1223, the highest junction temperature is on the output FET.

2.1 Measurement Results

Three units each of the TRF1123 and TRF1223 were measured as described above. A typical infrared image of the TRF1123 and the TRF1223 is shown in Figure 4 and Figure 5, respectively. The thermal resistance measured for the devices are from the junction (highest temperature) to the metal heatsink below the PCB and is representative of how the part will be used, i.e., they include the thermal resistance of the PCB.

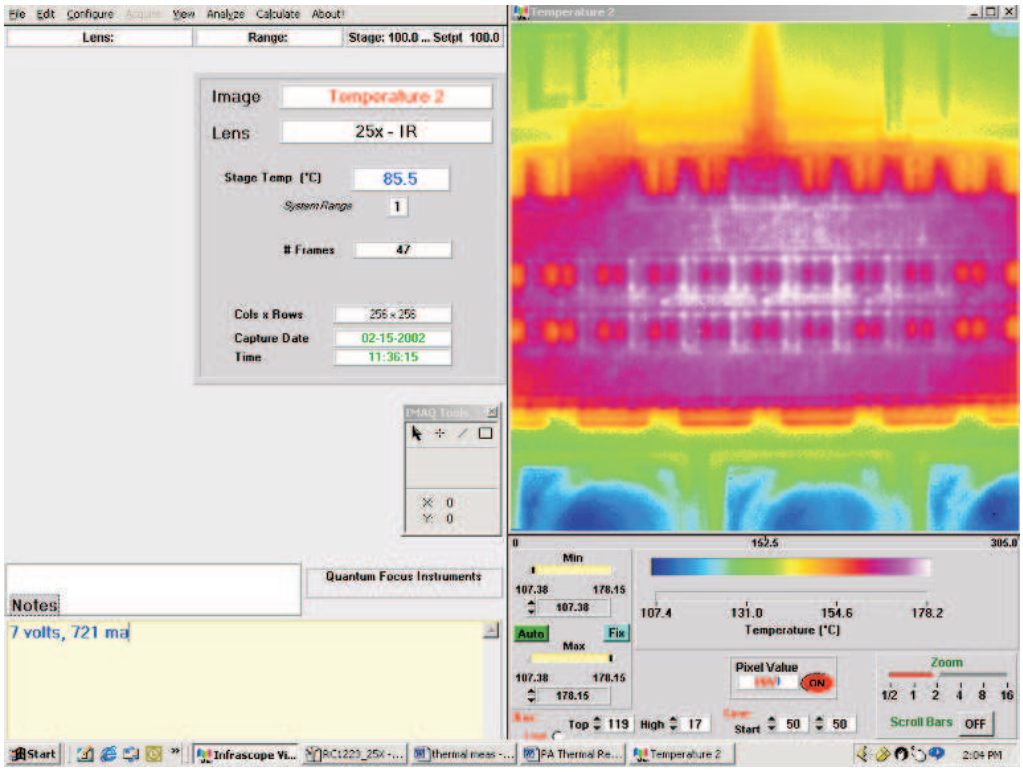


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Figure 4. Infrared Picture of Output FET of TRF1123, Baseplate is 85°C

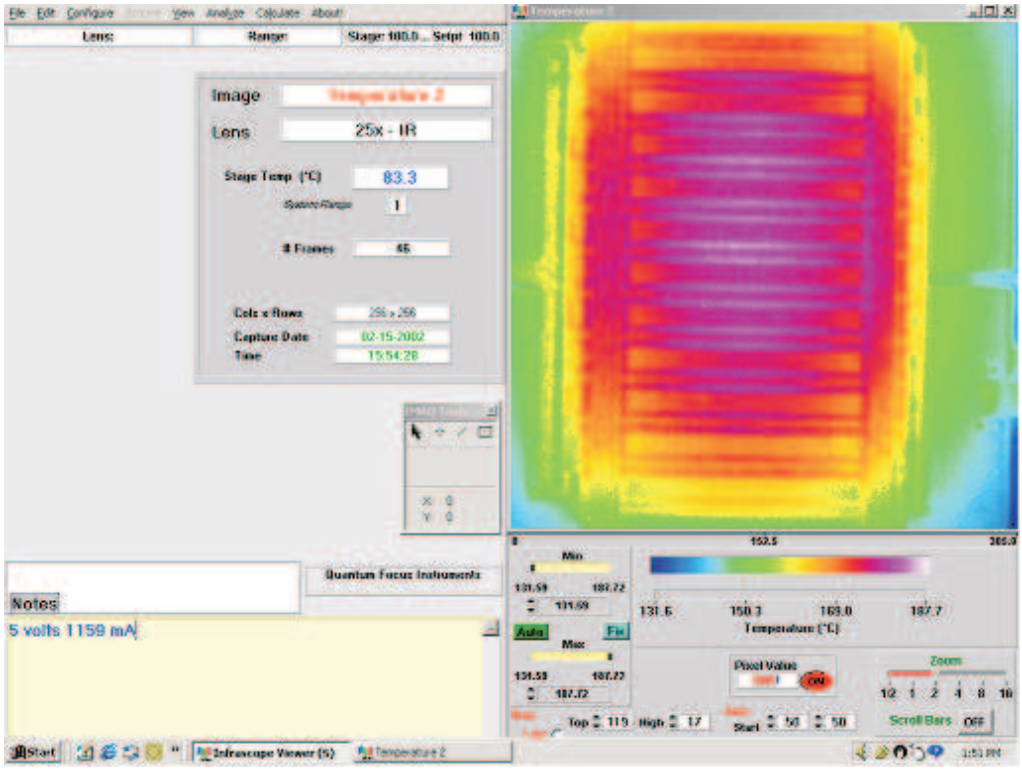

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Figure 5. Infrared Picture of Output FET of TRF1223, Baseplate is at 85°C

For the four TRF1123 devices measured the maximum channel temperature ranged from 176.8°C to 179.4°C yielding thermal resistances of 20.5°C/W to 21.3°C/W. For the TRF1223 the maximum channel temperature ranged from 182.5°C to 186.4°C yielding thermal resistances of 19.1°C/W to 19.6°C/W.

Table 1 shows summary of the measurements made.

Table 1. Measured Junction Temperature of the TRF1123 and TRF1223 From Peak Junction Temperature to Metal Baseplate

	TRF1123				TRF1223			
	SN#1	**SN#2**	**SN #3**	**SN #4**	**SN #1**	**SN #2**	**SN #3**	**SN #4**
Vdd (V)	7	7	7	7	5	5	5	5
Ids (mA)	0.637	0.64	0.635	0.616	1.021	1.037	1.034	1.031
Pd (W)	1.159	4.48	4.445	4.312	5.105	5.185	5.17	5.155
Tbp (°C)	85	85	85	85	85	85	85	85
Tjmax (°C)	179.2	176.9	179.4	176.8	182.5	186.4	186.4	185.3
Rj-bp(°C/W)	21.1	20.5	21.2	21.3	19.1	19.6	19.6	19.5
Average Rj-bp (°C/W)	21				19.4			

Measurements were also made on the top of the PCB next to the package and on top of the package near the edge of the chip in order to estimate the thermal resistance of the PCB. Based on these measurements, the PCB thermal resistance was approximately 5°C/W.

3 Lifetime Predictions and Maximum Baseplate Temperature

3.1 Lifetime Predictions

The median time to failure (MTTF) can be estimated using the Arrhenius Equation:

$$tf2 = tf1 \times \exp\left[\frac{Ea}{k} \times \left(\frac{1}{T2} - \frac{1}{T2}\right)\right]$$

Where:

tf = time to failure

Ea = activation energy in eV

k = Boltzman's constant (8.6152e-5 eV/K)

T = absolute temperature in Kelvin

For GaAs MESFET devices, the activation energy (rate of progression for dominant failure mechanisms) is typically 1.8eV. Lifetimes are measured at extremely high channel temperatures and the data used to predict the lifetimes at more moderate temperatures where typical lifetimes are too long to measure. Based on lifetime measurements of GaAs MESFET devices, the Arrhenius Equation can be re-written as:

$$tm = tmo \times \exp\left(\frac{Ea}{kT}\right)$$

Where:

tm = median lifetime

T = channel temperature in Kelvin

tmo = 9.116e-15 for GaAs MESFET

For a continuous channel temperature of 175°C, the median lifetime is greater than 1.6 million hours (182 years). This can also be expressed in failure units (FIT), which is becoming the more accepted unit of measure for failure rates of semiconductor devices. One FIT is equal to one failure per billion device hours (0.0001% per thousand hours). At 175°C the failure rate would be 625 FIT or 0.0625% per thousand hours. A junction temperature of 175°C is generally accepted as the maximum allowable channel

temperature for GaAs MESFET devices. The above failure rates are calculated for continuous junction temperature of 175°C while in practice the junction temperature varies due to ambient temperature variation. In some systems the TRF1123 and TRF1223 are only turned on for the transmit duration using the PACNT digital control resulting in a lower average temperature and longer MTBF. For every 6.8°C increase (or decrease) in temperature, the failure rate increases (or decreases) by a factor of 2.

3.2 Maximum Base Temperatures and Power Dissipation

In order to maintain channel temperatures less than 175°C, it may be necessary to limit the baseplate temperature and/or the power dissipation. The maximum base-plate temperature allowable can be calculated using the following equation:

$$Tbp = T_J - [(\theta_{JC} + \theta c\text{-}bp) \times Pd$$

Where:

Tbp = baseplate temperature (in °C)

T_J = Junction temperature (channel temperature in °C)

θ_{JC} = Junction to case thermal resistance (thermal resistance from channel to backside of package in °C/W

θc-bp = case to baseplate thermal resistance (PCB thermal resistance in °C/W

Pd = Power dissipated in Watts

For T_J = 175°C, θ_{JC} = 15°C/W, θc-bp = 5°C/W, and Pd = 5W:

$$Tbp = 175 - [(15 + 5) \times 5] = 75°C$$

If baseplate temperatures of greater than 75°C are desired, it may be necessary to reduce the power dissipation in order to ensure peak channel temperatures of less than 175°C. The following equation can be used to calculate the maximum power dissipation for a given ambient temperature:

$$Pd = \left(\frac{T_J - Tbp}{\theta_{JC} + \theta c\text{-}bp} \right)$$

For the case above, if ambient temperatures of 85°C (Tbp = 85°C) are required, the maximum allowable power dissipation would be:

$$Pd = \left(\frac{175 - 85}{15 + 5} \right) = 4.5 \text{ W}$$

A typical outdoor transceiver will have an ambient temperature specification of 50°C. The housing will have thermal rise dependent on surface area and design but a typical value is between 10 and 20°C and a solar load of 5°C. Consequently, the baseplate temperature in a typical application will be between 65°C and 75°C, which is at or below the reliable limit for GaAs junction temperature when the recommendations on PCB design are followed.

4 Conclusion

We have presented PCB layout guidelines for the TRF1123 and TRF1223 to provide lowest thermal resistance when the heat path is through the PCB and into a metal heatsink. Junction temperature measurements of devices mounted in this configuration show maximum junction temperature of 175°C is achieved with a maximum baseplate temperature of 75°C. The baseplate temperature is consistent with outdoor, environmentally sealed transceiver specifications and design. Thermal measurements and reliability data show that excellent product reliability is achievable.

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