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3Q 2001

Issue 1

Sine On™

AN ANALOG AND MIXED-SIGNAL PRODUCT CATALOG

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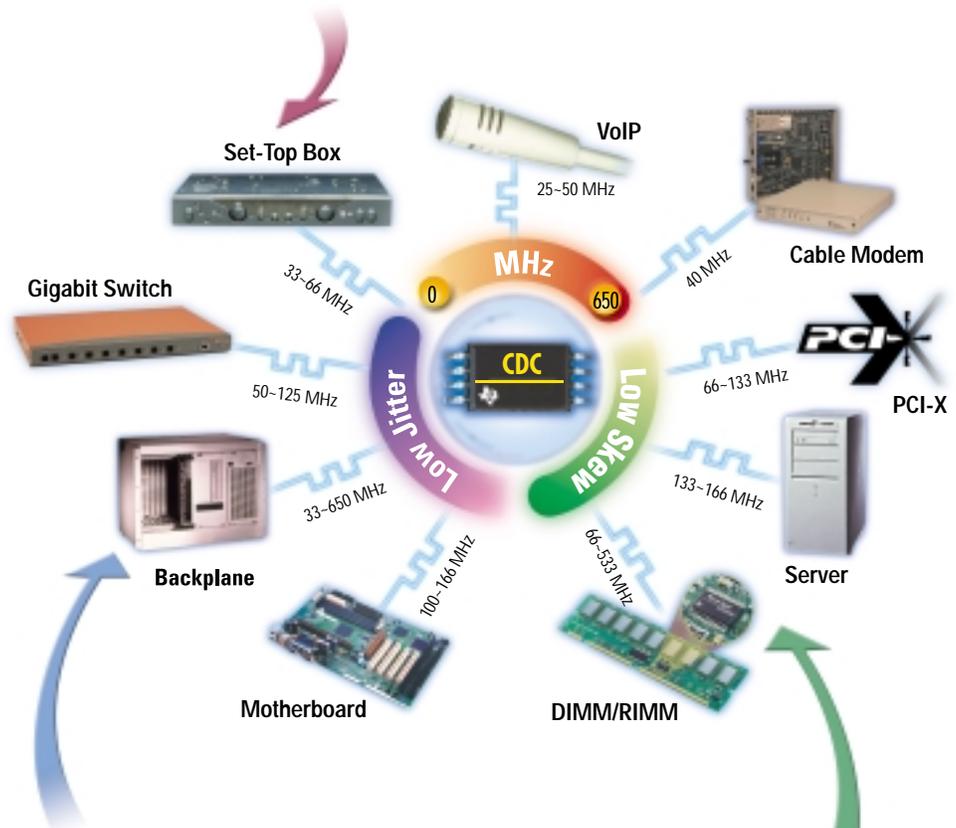
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Clock Buffers

LVPECL clock driver with nine outputs

CDC111, CDCVF111

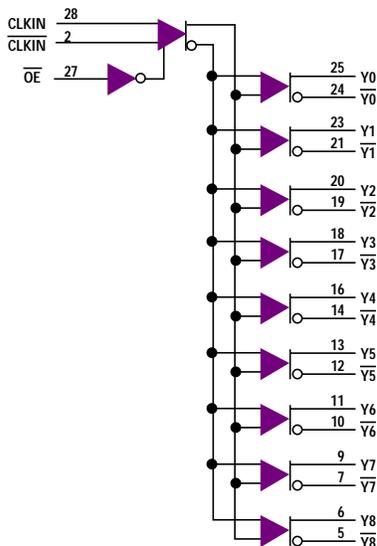
Get samples, datasheets and app reports at:
www.ti.com/sc/device/CDC111
www.ti.com/sc/device/CDCVF111



- Distributes one pair of differential clock inputs to nine pairs of differential clock outputs
- Low-voltage pseudo-ECL (LVPECL)-compatible inputs and outputs
- Operating frequency up to 650 MHz
- Operates from 3.3-V supply
- Low output and pulse skew for clock-distribution applications
- Output reference voltage, V_{REF} , allows distribution from a single-ended clock input
- Single-ended LVPECL compatible output enable
- Packaging: available in 28-pin plastic chip carrier

CDC111 and CDCVF111 logic diagram

The CDC111 and CDCVF111 distribute one pair of differential LVPECL clock inputs to nine pairs of differential clock outputs with minimum skew for clock distribution up to 650 MHz.



- Applications include:
- Telecom
 - Networking
 - Backplane
 - Other general-purpose applications

High-performance TTL-compatible clock driver with eight outputs

CDC341

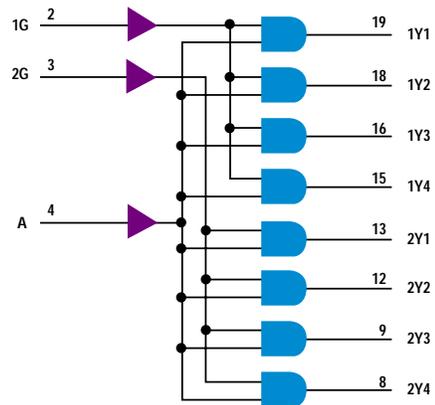
Get samples, datasheets and app reports at:
www.ti.com/sc/device/CDC341



- Distributes one clock input into two banks of four outputs each
- Operating frequency up to 80 MHz
- Operates from 5-V supply
- Low output and pulse skew for clock-generation applications
- TTL-compatible inputs and outputs
- EPIC-IIB™ BiCMOS design significantly reduces power dissipation
- High-drive outputs ($-48\text{-mA } I_{OH}$, $48\text{-mA } I_{OL}$)
- Packaging: available in 20-pin SOIC

CDC341 logic diagram

The CDC341 is a 5-V buffer which distributes two banks of four outputs that can be driven into a low state by the use of two control pins.



- Applications include:
- Telecom
 - Networking
 - Other general-purpose applications

Clock Buffers

LVTTTL clock driver features mixed-mode signal operation with 10 output

CDC351, CDC2351

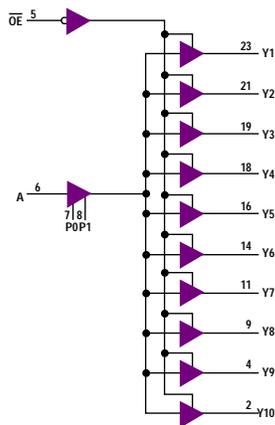
Get samples, datasheets and app reports at:
www.ti.com/sc/device/CDC351
www.ti.com/sc/device/CDC2351



- Distributes one clock input to 10 outputs
- Operating frequency up to 100 MHz
- Operates at 3.3-V V_{CC}
- Low output and pulse skew for clock-generation applications
- LVTTTL-compatible inputs and outputs
- EPIC-IIB™ BiCMOS design significantly reduces power dissipation
- Supports mixed-mode signal operation (5-V input and output voltages with 3.3 V_{CC})
- Propagation delays are adjusted at the factory to ensure part-to-part skew is minimized
- CDC2351 features additional internal series-damping resistors on the outputs to reduce transmission line effects
- Operates at 3.3-V V_{CC}
- Packaging: available in 24-pin SOIC and TSSOP

CDC351 and CDC2351 logic diagram

The CDC351 and CDC2351 distribute ten clock outputs optimized for minimal part-to-part skew.



➤ Applications include:

- Telecom
- Networking
- Basestations
- Other general-purpose applications

TTL clock driver with six outputs featuring polarity and three-state control

CDC391

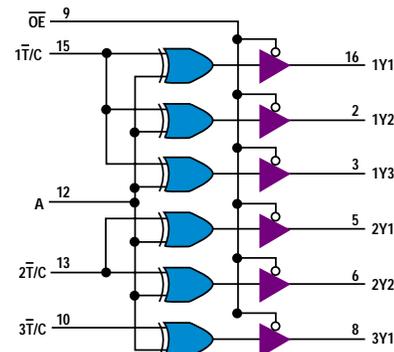
Get samples, datasheets and app reports at:
www.ti.com/sc/device/CDC391



- Distributes one clock input to six clock outputs
- Polarity control selects true or complementary outputs
- Operating frequency up to 100 MHz
- Operates from 5-V supply
- Low output and pulse skew for clock-generation applications
- TTL-compatible inputs and outputs
- EPIC-IIB™ BiCMOS design significantly reduces power dissipation
- High-drive outputs ($-48\text{-mA } I_{OH}$, $48\text{-mA } I_{OL}$)
- Packaging: available in 16-pin SOIC

CDC391 logic diagram

The CDC391 distributes six clock outputs that can be controlled for true or complementary outputs or disabled to a high-impedance state.



➤ Applications include:

- Telecom
- Networking
- Other general-purpose applications

Clock Buffers

Versatile 1:4 fanout for PCI-X and general applications

CDCV304

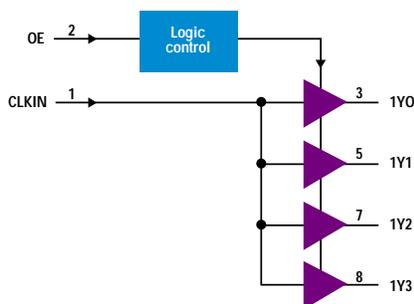
Get samples, datasheets and app reports at:
www.ti.com/sc/device/CDCV304



- Distributes one clock input to one bank of four outputs
- Operating frequency: 0 MHz to 140 MHz
- Operates from 3.3-V supply
- Output-enable (OE) control that drives outputs low when OE is low
- Low output skew: <100 ps
- Low pulse skew: <0.5 ns
- Characterized for operation from -40°C to 85°C
- Packaging: available in 8-pin TSSOP

CDCV304 block diagram

The CDCV304 is a high-performance, low-skew, general-purpose and PCI-X clock buffer that distributes four clock outputs.



➤ Applications include:

- PCI-X
- Networking
- Automotive
- Servers
- Telecom
- DSP buffer applications

High-performance 1:10 clock buffer for general-purpose applications

CDCVF2310

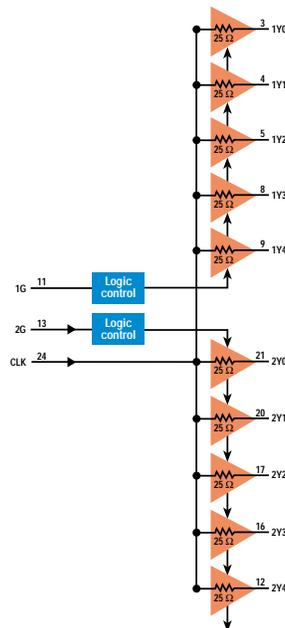
Get samples and datasheets at:
www.ti.com/sc/device/CDCVF2310



- Distributes one clock input to two banks of five outputs each
- Operates up to 200 MHz
- Pin-to-pin skew: <200 ps
- V_{DD} range: 2.3 V to 3.6 V
- Output-enable glitch suppression
- On-chip series damping resistors of $25\ \Omega$
- Characterized for operation from -40°C to 85°C
- Packaging: available in 24-pin TSSOP

CDCVF2310 typical application

The CDCVF2310 distributes two banks of five, low-skew outputs and operates up to 200 MHz.



➤ Applications include:

- Telecom
- Networking
- Motherboards
- Basestations
- Other general-purpose applications

Phase-Lock-Loop (PLL) Clock Drivers

LVTTTL 1:6 PLL clock driver with configurable and three-state outputs

CDC536, CDC2536

Get samples, datasheets and app reports at:

www.ti.com/sc/device/CDC536

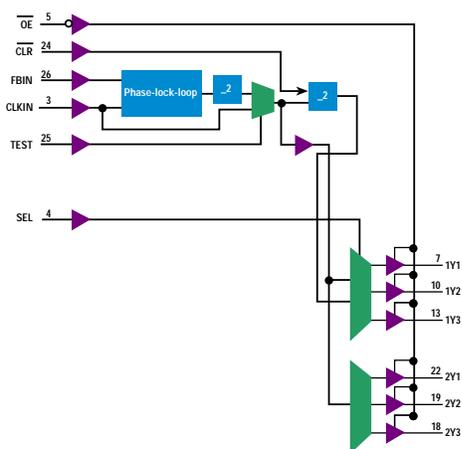
www.ti.com/sc/device/CDC2536



- Distributes one clock input to six outputs with three configurable outputs of 1/2x, 1x and 2x
- Operating frequency: 25 MHz to 100 MHz
- Low-output skew for clock-distribution and clock-generation applications
- LVTTTL-compatible inputs and outputs
- Negative edge triggered clear for half-frequency outputs
- EPIC-IIB™ BiCMOS design significantly reduces power dissipation
- External feedback terminal synchronizes the outputs to the clock input
- CDC2536 features on-chip series-damping resistors of 25 Ω
- Integrated RC PLL filter eliminates the need for external components
- Operates at 3.3-V V_{CC}
- Packaging: available in 28-pin SSOP

CDC536 and CDC2536 block diagram

The CDC536 and CDC2536 are zero-delay buffers, which distribute six clock outputs, and can be configured to 1/2x, 1x or 2x the frequency.



➤ Applications include:

- SDRAM applications
- High-speed microprocessors
- Set-top boxes
- Other general-purpose applications

LVTTTL 1:12 PLL clock driver with configurable and three-state outputs

CDC586, CDC2586

Get samples, datasheets and app reports at:

www.ti.com/sc/device/CDC586

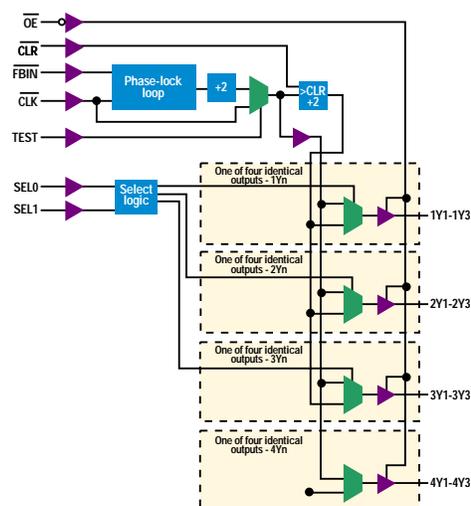
www.ti.com/sc/device/CDC2586



- Distributes one clock input to 12 outputs with nine configurable outputs of 1/2x, 1x and 2x
- Operating frequency: 25 MHz to 100 MHz
- Low-output skew for clock-generation applications
- LVTTTL-compatible inputs and outputs
- EPIC-IIB™ BiCMOS design significantly reduces power dissipation
- External feedback terminal synchronizes the outputs to the clock input
- CDC2586 features on-chip series-damping resistors of 25 Ω
- Integrated RC PLL filter eliminates the need for external components
- Operates at 3.3-V V_{CC}
- Packaging: available in 52-pin TQFP

CDC586 and CDC2586 block diagram

The CDC586 and CDC2586 are zero-delay buffers, which distribute 12 clock outputs and can be configured to 1/2, 1x or 2x the frequency.



➤ Applications include:

- SDRAM applications
- High-speed microprocessors
- Other general-purpose applications

Phase-Lock-Loop (PLL) Clock Drivers

High-performance 1:5 PLL clock driver for general-purpose applications

CDCVF2505

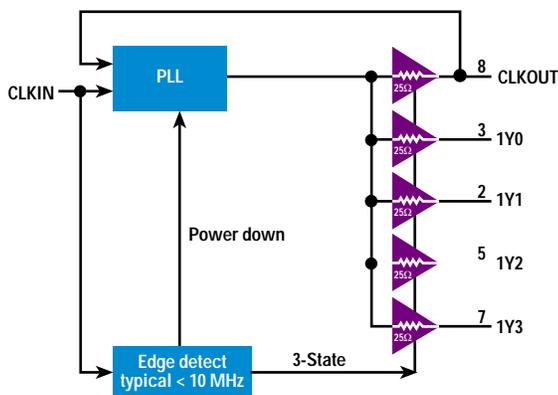
Get samples and datasheets at:
www.ti.com/sc/device/CDCVF2505



- Spread-spectrum clock compatible for reduced EMI
- Operating frequency: 24 MHz to 200 MHz
- Low jitter (cycle-to-cycle) < |150ps| over the range 66 MHz to 200 MHz
- Distributes one clock input to one bank of five outputs
- Automatically switches into power-down mode when input clock is <2 MHz
- Consumes less than 100 μ A (typ) in power-down mode
- Internal feedback loop synchronizes the outputs to the clock input
- Internal 25- Ω , on-chip series damping resistors
- Integrated RC PLL filter eliminates need for external components
- Operates at 3.3 V
- Packaging: available in 8-pin TSSOP or SOIC

CDCVF2505 block diagram

The CDCVF2505, with its 3.3-V zero-delay buffers, distributes one bank of five outputs.



➤ Applications include:

- | | |
|----------------------|---|
| • SDRAM applications | • Routers |
| • Networking | • Gigabit switches |
| • Telecom | • Automotive |
| • Set-top boxes | • Cable modems |
| • Storage | • Asynchronous transfer mode (ATM)/CO switching |

Versatile 2.5 V/3.3 V PLL clock driver with two banks of four outputs

CDCVF25081

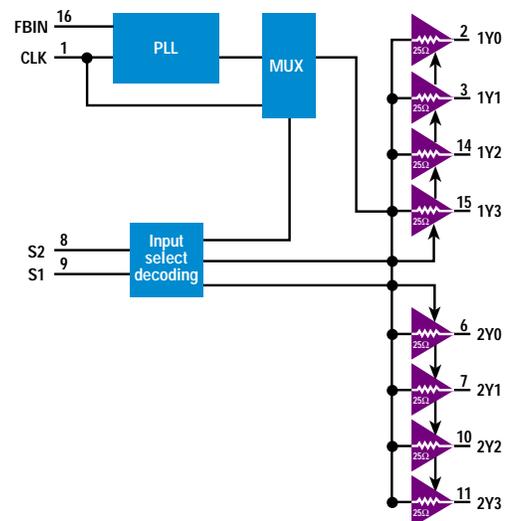
Get samples and datasheets at:
www.ti.com/sc/device/CDCVF25081



- Distributes one clock input to two banks of four outputs each
- CDCVF25081 features two banks of 1x frequencies
- Spread-spectrum clock compatible for reduced EMI
- Operating frequency: 10 MHz to 170 MHz
- Low jitter (cycle-to-cycle) < |150ps| over the range 66 MHz to 170 MHz
- Three state outputs when there are no rising edges on the input clock
- Consumes less than 200 μ A in power down mode
- 22- Ω , on-chip series damping resistors
- Integrated RC PLL filter eliminates need for external components
- Operates from 2.3 V - 3.6 V
- Packaging: available in 16-pin TSSOP and SOIC

CDCVF25081 block diagram

The CDCVF25081 distributes one clock input to two banks of four outputs each.



➤ Applications include:

- Basestation applications
- Networking
- Motherboards
- Other general-purpose applications

Phase-Lock-Loop (PLL) Clock Drivers

High-performance 1:9 or 1:10 PLL clock driver for SDRAM applications

CDCVF2509, CDCVF2510

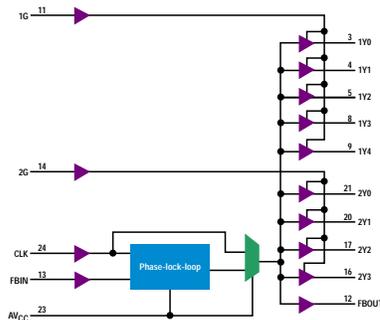
Get samples and datasheets at:
www.ti.com/sc/device/CDCVF2509
www.ti.com/sc/device/CDCVF2510



- Accepts HCSL, SSTL-II and LVTTTL levels with minimum 400-mV swing
- Designed to meet and exceed PC100/133 SDRAM registered-DIMM specification Rev. 1.1
- Spread-spectrum clock compatible for reduced EMI
- Operating frequency: 50 MHz to 175 MHz
- Static-phase error distribution is +125 ps over the range of 66 MHz to 166 MHz
- Cycle-to-cycle jitter at 66 MHz to 166 MHz: |70| ps
- Advanced deep submicron process results in more than 40% lower consumption vs. current generation PC 133 devices
- CDCVF2509 distributes one clock input to one bank of five and one bank of four outputs
- CDCVF2510 distributes one clock to one bank of 10 outputs
- External feedback terminal is used to synchronize the outputs to the clock input
- External 25-Ω, on-chip series damping resistors
- Integrated RC PLL filter eliminates need for external components
- Operates at 3.3 V
- Packaging: available in 24-pin TSSOP

CDCVF2509 and CDCVF2510 block diagram

The CDCVF2509 and CDCVF2510 are zero-delay buffers, which distributes nine or 10 outputs and can be disabled by separate control pins.



➤ Applications include:

- SDRAM applications
- Other general-purpose applications

PLL clock driver with universal input swing levels for DDR applications

CDCV850

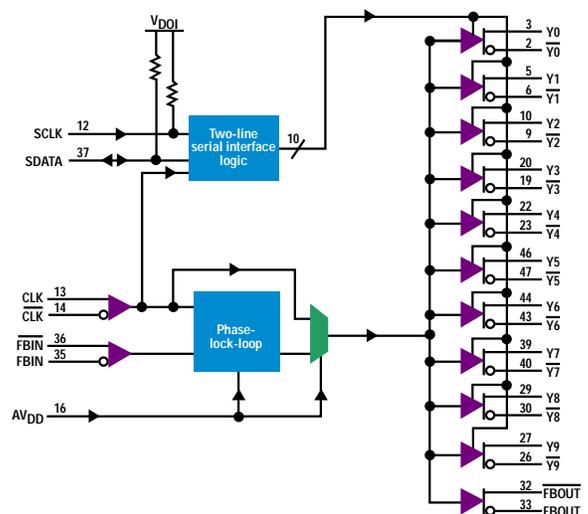
Get samples, datasheets and app reports at:
www.ti.com/sc/device/CDCV850



- Spread-spectrum-clock compatible
- Operating frequency: 60 MHz to 140 MHz
- Low jitter cycle-to-cycle: +75 ps
- Distributes one differential clock input to 10 differential outputs
- Two-line serial interface provides output enable and functional control
- Offers three-state outputs when the input differential clocks are <20 MHz
- Operates from dual 2.5-V and 3.3-V supplies
- Consumes less than 250-μA quiescent current
- External feedback pin used to synchronize outputs to the input clocks
- Packaging: available in 48-pin TSSOP

CDCV850 block diagram

The CDCV850 is a zero-delay buffer which distributes one differential pair of inputs to differential pairs of outputs controlled by a two-line serial interface.



➤ Applications include:

- Double-data rate (DDR) applications
- Translates multiple input levels to SSTL_2 output level
- Optimized for use with the CDC950 and CDC857 and ServerWorks Grand Champion™ chipset

DDR Phase-Lock-Loop (PLL) Clock Drivers

PLL clock driver for DDR applications with five outputs

CDCV855

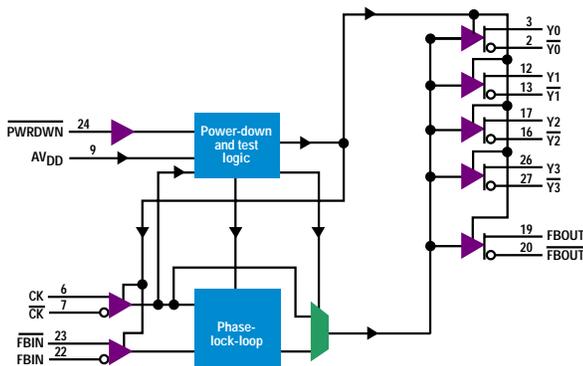
Get samples and datasheets at: www.ti.com/sc/device/CDCV855



- Distributes one differential clock input to four differential outputs plus feedback pair
- Operating frequency: 60 MHz to 200 MHz
- Operates from dual 2.5-V supplies
- Low jitter cycle-to-cycle: +75 ps
- Ultra-low power-down mode
- Enters low power mode when no clock input signal is applied or power down is low
- Spread-spectrum clock (SSC) compatible for reduced EMI
- External feedback differential pair used to synchronize the outputs to the input clocks
- Packaging: available in 28-pin TSSOP

CDCV855 block diagram

The CDCV855 is a zero-delay buffer which distributes one differential pair of inputs to four differential pairs of clock outputs plus a differential feedback pair.



- Applications include:
- Double-data rate (DDR) SDRAM memory modules
 - Other DDR or differential applications

High-performance PLL clock driver for DDR applications with 10 outputs

CDCV857, CDCV857A

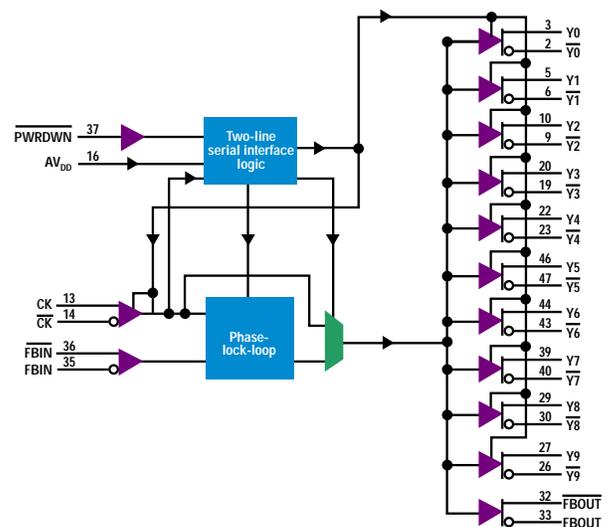
Get samples and datasheets at: www.ti.com/sc/device/CDCV857
www.ti.com/sc/device/CDCV857A



- For complete DDR DIMM solution, use with SSTV16857
- Distributes one differential clock input to 10 differential outputs
- Operating frequency: 60 MHz to 180 MHz
- Operates from dual 2.5-V supplies
- CDC857 low jitter (cycle-to-cycle): ±75 ps
- CDCV857A low jitter (cycle-to-cycle) ±50 ps
- Ultra-low power-down mode: <200 μA
- Three-state outputs and centers power down mode when the input differential clocks are <20 MHz
- Spread-spectrum-EMI reduction mode
- Optimized to work with CDC950 and CDC850
- Packaging: available in 48-pin TSSOP, 48-pin TVSOP and MicroStar™ BGA

CDCV857 and CDCV857A block diagram

The CDCV857 and CDCV857A are low-jitter zero-delay buffers which distribute one differential pair of inputs to 10 differential pairs of clock outputs plus a differential feedback pair.



- Applications include:
- Double-data rate (DDR) SDRAM memory modules
 - Other DDR or differential applications

DDR Clock Synthesizer

DDR Logic Registers

Differential clock synthesizer/driver for ServerWorks™ chipset

Registered buffer with SSTL_2 I/O for DDR memory systems

CDC950

SN74SSTV16857

Get samples, datasheets and app reports at: www.ti.com/sc/device/CDC950

Get samples, datasheets and app reports at: www.ti.com/sc/device/SN74SSTV16857

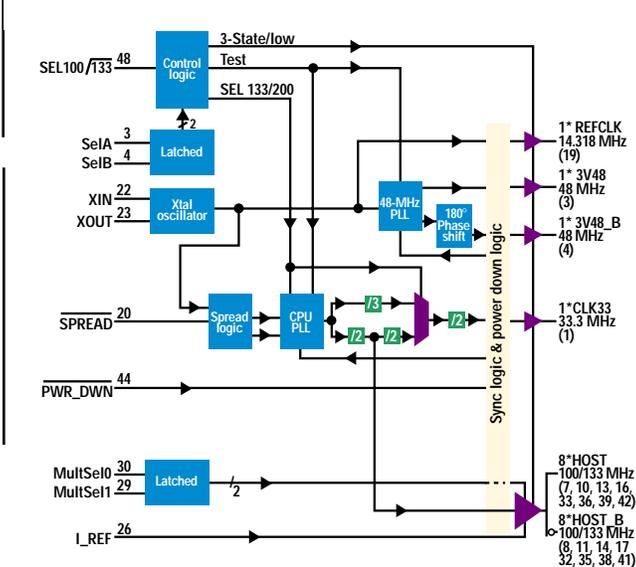


- Uses a 14.318-MHz crystal input to generate multiple output frequencies
- Includes spread-spectrum clocking (SSC), 0.6% downspread for reduced EMI
- Power management control terminals
- Low-output skew and jitter for clock distribution
- Operates from a single 3.3-V supply
- Generates the following clocks:
 - Eight Host (different pairs, 100/133 MHz)
 - One CLK33 (3.3 V, 33 MHz)
 - One REFCLK (3.3 V, 14.318 MHz)
 - Two 3V48 (3.3 V, 180° shifted pairs, 48 MHz)
- Packaging: available in 48-pin TSSOP

- For complete DDR DIMM solution, use with CDCV857A
- Designed for 2.3-V to 2.7-V V_{CC} operation
- Supports SSTL_2 data inputs
- Outputs meet SSTL_2 Class-II specifications
- Differential clock inputs
- Supports low-voltage CMOS switching levels on the Reset input
- Supports Reset input disables differential input receivers, resets all registers and forces all outputs low
- Flow-through architecture optimizes printed circuit board layout
- Latch-up performance exceeds 100 mA per JESD 78, Class II
- ESD performance of 2500-V HBM, 200-V MM and 1000-V CDM
- Provides DDR SDRAM address and control signal
- Packaging: available in 48-pin TSSOP and TVSOP
- Suggested resale price starts at \$2.51 each in quantities of 2,000

CDC950 block diagram

The CDC950 is a differential clock synthesizer/driver that generates system clock signals to support a computer system with double-data rate (DDR) memory subsystem.



➤ Applications include:

➤ Applications include:

- Generating clock signals for Pentium® 4 class microprocessors and double-data rate (DDR) memory subsystems
- Optimized for use with the CDCV850 and CDCV857 and ServerWorks Grand Champion™ chipset

- 184-pin JEDEC Standard DDR - 200/266 DIMM
- 184-pin low-profile (1U) DDR - 200/266 DIMM

Complementary devices

The CDC950 differential clock synthesizer completes TI's solution for the 184-pin DDR SDRAM module. SSTV devices are ideal solutions for address/control bus buffering in high-performance DDR memory systems.

SN74SSTV16857 features

	SN74SSTV16857
Function	1-to-1 register
Bit 2width	14-bit
V _{CC}	2.5-V
Package	48-pin TSSOP and TVSOP
Output enable	No
End equipment	184-pin DIMM

LVDS Repeaters

LVDS low power, low EMI, repeaters for clock distribution up to 315 MHz

SN65LVDS104/105/108/109/116/117

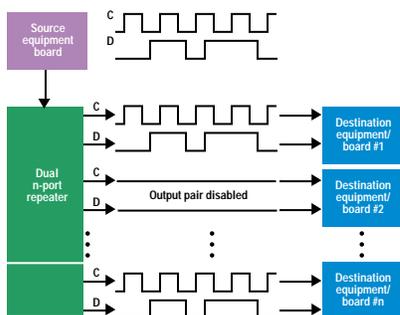
Get samples, datasheets and app reports at: www.ti.com/sc/device/partnumber

Replace *partnumber* in URL with SN65LVDS104, SN65LVDS105, SN65LVDS108, SN65LVDS109, SN65LVDS116 or SN65LVDS117



- Low-voltage differential signaling (LVDS) for 1:n port clock distribution where $4 < n < 16$
- SN65LVDS104/105 are four-channel repeaters
SN65LVDS108/109 are eight-channel repeaters
SN65LVDS116/117 are 16-channel repeaters
- Enabling logic allows separate control of each bank of four channels or 2-bit selection of any one of the four banks
- Low skews: output and pulse skews are less than 300 ps
- Flow-through pinout
- Electrically compatible with LVDS, PECL, LVPECL, LTTL, LVCMOS, GTL, BTL, CTT, SSTL or HSTL outputs with external termination networks
- Bus-pin ESD production exceeds 12 kV (15 kV for the LVDS104 and LVDS105)
- Total power dissipation 470 mW (typ) with 16 channels at 200 MHz (LVDS116)
- Driver output or receiver input at high impedance when disabled or with V_{CC} less than 1.5 V
- Propagation delay times less than 4 ns
- Packaging: available in 64-pin TSSOP (SN65LVDS116/117), 38-pin TSSOP (SN65LVDS108/109) and 16-pin SOIC and TSSOP (SN65LVDS104/105)
- Suggested resale price starts at \$2.89 each in quantities of 1,000

LVDS dual multiport repeater application



- Applications include:
 - Basestation backplane clock distribution, Sonet/SDH

LVDS Dual Multiplexed Repeaters

2x2 switch for backplane bridging, 1:2 repeater for redundant signals

SN65LVD(S/M)22

Get samples, datasheets and app reports at: www.ti.com/sc/device/partnumber

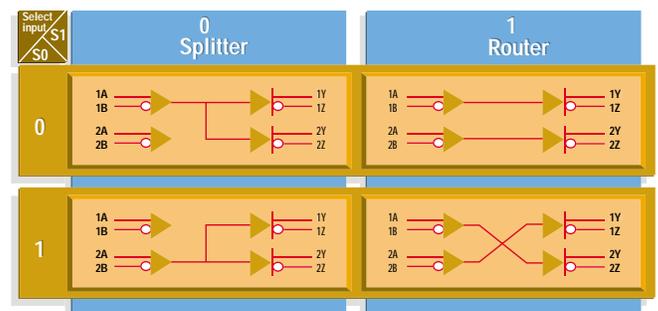
Replace *partnumber* in URL with SN65LVDS22 or SN65LVDM22



- SN65LVDM22 has twice the output current of SN65LVDS22 to support multipoint interconnections
- Repeaters bridge multiple backplanes in a rack
- Signal splitting or routing between backplanes
- Signaling rates up to 400 Mbps
- Power dissipation at 400 Mbps is 150 mW
- Hot-plugging capability: driver in high impedance when disabled or with $V_{CC} < 1.5 V$
- Fault tolerance: drive-circuit fail-safe receiver
- ESD protection exceeds 12 kV on bus bins
- Propagation time delay: 4 ns (typ)
- LVTTTL-select input levels are 5-V tolerant
- Packaging: available in 16-pin SOIC
- Suggested resale price starts at \$3.69 each in quantities of 1,000

Mux table

Select pins S0 and S1 allow four device options.



- Applications include:
 - Sonet/SDH rack-to-rack connectivity, redundant signal routing on Basestation backplanes

Selection Guide for CDC Products

Buffer-Based Clock Distribution			All packages are available in tape and reel			
Device	Description	I/O levels	$t_{SK(o)}$ max. (ns)	Frequency (MHz)	No. pins/pkg	$V_{CC}(V)$
CDC111	1:9 differential LVPECL clock driver	LVPECL/LVPECL	0.05	0-500	28/PLCC	3.3
CDC203	6:6 hex inverter/clock driver	CMOS/CMOS	0.7	0-40	20/SOIC	3.3
CDC204	6:6 hex inverter/clock driver	CMOS/CMOS	1.0	0-80	20/SOIC	5
CDC208	Dual 1:4 fanout	TTL/CMOS	1.0	0-60	20/SOIC	5
CDC318A	1:18 clock driver with two-line serial interface	LVTTTL/LVTTTL	0.25	0-100	48/SSOP	3.3
CDC319	1:10 clock driver with two-line serial interface	LVTTTL/LVTTTL	0.25	0-100	28/SSOP	3.3
CDC328A	1:6 fanout w/ sel polarity	TTL/TTL	0.5	0-100	16/SOIC/SSOP	5
CDC329A	1:6 fanout w/ sel polarity	TTL/CMOS	0.6	0-80	16/SOIC	5
CDC337	1:8 clock driver with four 1x outputs, four 1/2x outputs	TTL/CMOS	0.9	0-80	20/SOIC	5
CDC339	1:8 clock driver with four 1x outputs, four 1/2x outputs	TTL/TTL	0.9	0-80	20/SOIC/SSOP	5
CDC340	1:8 w/ fast tpd fanout	TTL/TTL	0.6	0-80	20/SOIC	5
CDC341	1:8 w/ fast tpd fanout	TTL/TTL	0.6	0-80	20/SOIC	5
CDC351/CDC2351 ¹	1:10 w/ fast tpd fanout	LVTTTL/LVTTTL	0.5	0-100	24/SOIC, SSOP	3.3
CDC391	1:6 clock driver with selectable polarity and 3-state outputs	TTL/TTL	0.5	0-100	16/SOIC	5
CDCV304	1:4 fanout for PCI-X and general applications	LVTTTL/CMOS	0.1	0-140	8/TSSOP	2.5/3.3
CDCVF2310	1:10 clock driver w/ 2 banks for general-purpose applications	LVTTTL/LVTTTL	0.17	0-170	24/TSSOP	3.3

Direct Rambus® Clock Generator						
Device	Description	I/O levels	$t_{SK(o)}$ max. (ns)	Frequency (MHz)	No. pins/pkg	$V_{CC}(V)$
CDCR61A	400-MHz Direct Rambus® clock generator lite	CMOS/RSL2	-	300, 400	16/TSSOP	1.8/3.3
CDCR83	400-MHz Direct Rambus® clock generator	CMOS/RSL2	-	267-400	24/SSOP	3.3
CDCFR83	533-MHz Direct Rambus® clock generator	CMOS/RSL2	-	267-533	24/SSOP	3.3

Clock Synthesizer/Driver for Motherboard Application						
Device	Description	I/O levels	$t_{SK(o)}$ max. (ns)	Frequency (MHz)	No. pins/pkg	$V_{CC}(V)$
CDC924	PC MB clk synthesizer/driver, 133-MHz max. freq w/ spread spectrum clock tracking	LVTTTL/LVTTTL	0.3	66, 100, 133	56/SSOP	2.5/3.3
CDC925	PC MB clk synthesizer/driver	LVTTTL/LVTTTL	0.175	100, 133	56/SSOP	2.5/3.3
CDC930	PC MB differential syn/dri w/ 133-MHz freq max. w/ spread spectrum	LVTTTL/HCSL, LVTTTL	0.5	100, 133	56/SSOP	3.3
CDC950	133-MHz differential clock syn/dri for PC motherboards w/ 3-state outputs	LVTTTL/HCSL, LVTTTL	0.1	100, 133	48/TSSOP	3.3

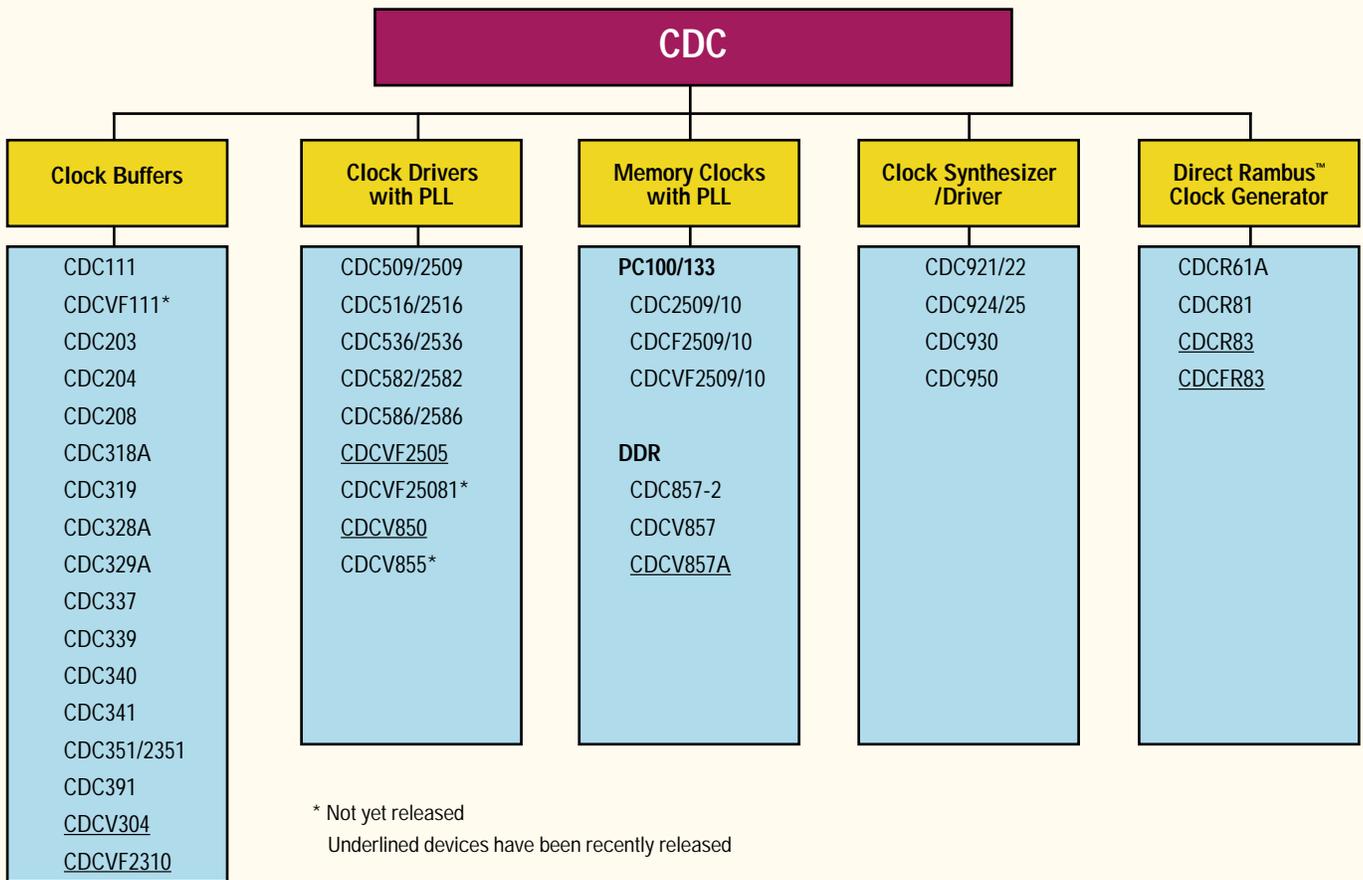
¹With series output resistors

Selection Guide for CDC Products (Continued)

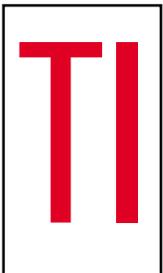
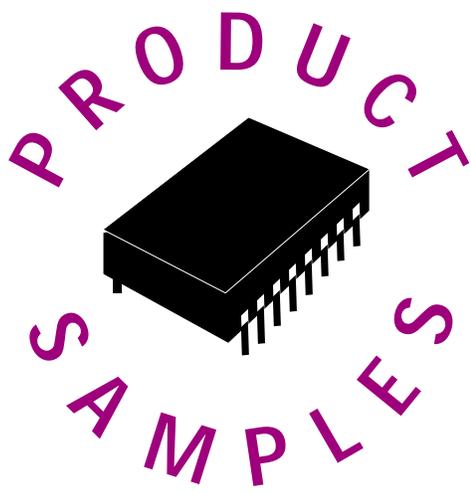
PLL-Based Clock Distribution						
Device	Description	I/O levels	$t_{SK(o)}$ max. (ns)	Frequency (MHz)	No. pins/pkg	$V_{CC}(V)$
CDC509	1:9 PLL clock driver w/ 3-state output	LVTTTL/LVTTTL	0.2	25-125	24/TSSOP	3.3
CDC516/CDC2516 ¹	1:16 PLL clock driver w/ 3-state output	LVTTTL/LVTTTL	0.2	25-125	48/TSSOP	3.3
CDC536/CDC2536 ¹	1:6 PLL clock driver w/ (3) at 1/2x or 2x output	LVTTTL/LVTTTL	0.5	25-100	28/SSOP	3.3
CDC582/CDC2582 ¹	1:12 LV diff PECL PLL clock driver w/ 9 outputs at 1/2x or 2x output	LVPECL/LVTTTL	0.5	25-100	52/TQFP	3.3
CDC586/2586 ¹	1:12 PLL clock driver w/ 9 outputs at 1/2x or 2x output	LVTTTL/LVTTTL	0.5	25-100	52/TQFP	3.3
CDC857-2/-3	1:10 SSTL-II differential PLL clock driver	SSTL-II/SSTL-II, LVTTTL	0.1	66-167	48/TSSOP	2.5/3.3
CDC2509B ¹ /C ¹	1:9 PLL clock driver w/ 3-state output with spread spectrum clock tracking	LVTTTL/LVTTTL	0.2	25-125	24/TSSOP	3.3
CDC2510B ¹ /C ¹	1:10 PLL clock driver w/ 3-state output with spread spectrum clock tracking	LVTTTL/LVTTTL	0.2	25-125	24/TSSOP	3.3
CDCF2509 ¹	1:9 PLL clock driver for PC 133 application	LVTTTL/LVTTTL	0.2	25-140	24/TSSOP	3.3
CDCF2510 ¹	1:10 PLL clock driver for PC 133 application	LVTTTL/LVTTTL	0.2	25-140	24/TSSOP	3.3
CDCV850	1:10 PLL clock driver for DDR SDRAM application, SSC compatible with two-line serial interface	HCSSL, Universal (except ECL) /SSTL-II	0.075	60-140	48/TSSOP	2.5/3.3
CDCV855	1:5 PLL differential clock driver for DDR applications	SSTL-II/SSTL-II, LVTTTL	0.075	60-180	28/TSSOP	2.5
CDCV857/CDCV857A	1:10 PLL differential clock driver for DDR applications	SSTL-II/SSTL-II, LVTTTL	0.075	60-180	48/TSSOP	2.5
CDCVF2505	1:5 PLL clock driver for general-purpose	LVTTTL/LVTTTL	0.15	24-200	8/TSSOP/SOIC	3.3
CDCVF25081	1:8 low-power PLL clock driver with two banks	LVTTTL/LVTTTL	0.15	10-170	16/TSSOP/SOIC	2.5/3.3
CDCVF2509	1:9 low-power PLL clock driver for PC 133 and beyond application	LVTTTL/LVTTTL	0.1	50-175	24/TSSOP	3.3
CDCVF2510	1:10 low-power PLL clock driver for PC 133 and beyond application	LVTTTL/LVTTTL	0.1	50-175	24/TSSOP	3.3

¹ With series output resistors

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Power Management

TL5002 Provides DDR Bus Termination Power Supply Solution, January 2000 (slva095)

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Application and Design Considerations for CDC5XX Phase-Lock-Loop Clock Drivers (scaa028)

Design and Layout Guidelines for the CDCVF2505 Clock Driver (scaa045)

High Speed Clock Distribution Design Techniques for CDC509/516/2509/2510/2516 (slma003a)

Phase-Lock-Loop (PLL) Clock Drivers: Benefits Versus Costs (scaa003a)

Understanding the Differences Between CDC2509X/10X Devices (scaa040)

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Clock Distribution in High-Performance PCs (scaa030a)

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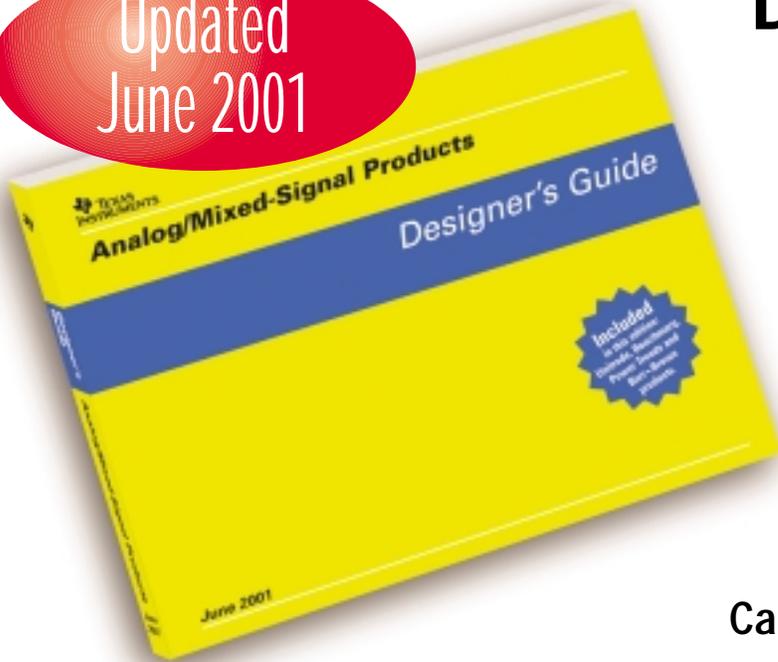
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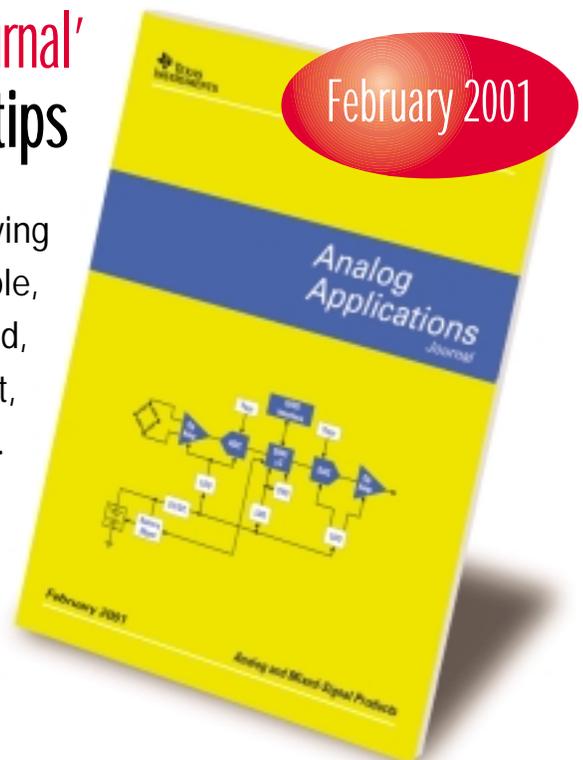
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