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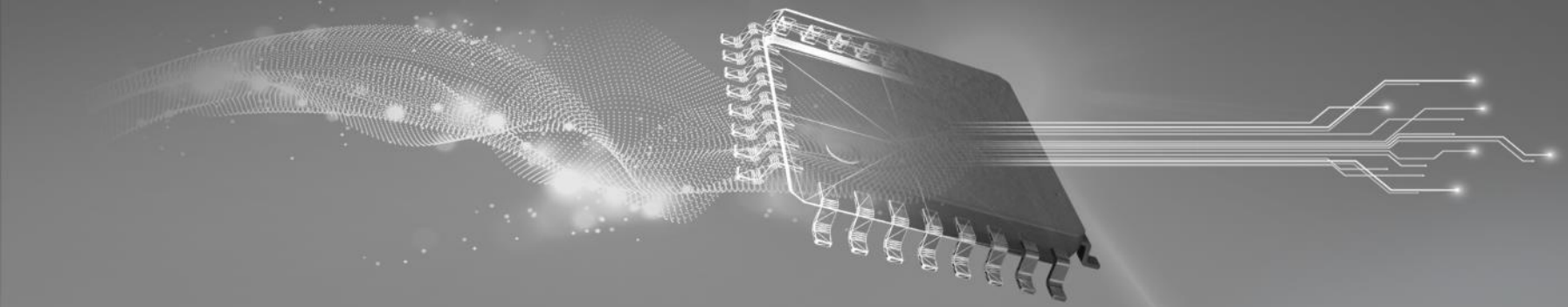

How to avoid design problems by using worst case analysis calculations

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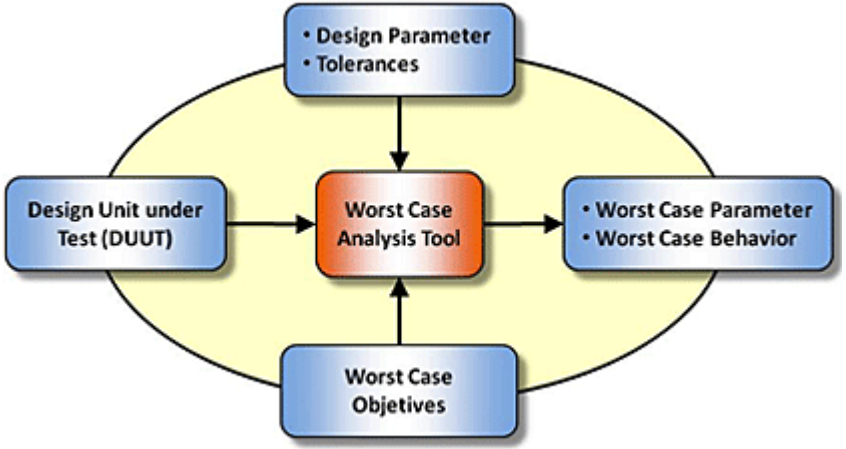
Agenda

- Discussion on what is worst case analysis
- Different types of worst case analysis – i.e.: Extreme value, RSS
- Discussion on electronic component tolerances – resistors, capacitors, and Inductors, with an inductor saturation example.
- Example 1: Output voltage regulation. UVLO, and OVLO are very similar. Reference and IC tolerance will be added here.
- Example 2: MOSFET Power dissipation. FET and Diode tolerances will be added here.
- Example 3 : BJT Transistor Beta

Worst case analysis definition

- A worst-case analysis is an assessment of a circuits functional performance, accounting for tolerances, such as **Beginning of life (BOL)**, environmental **(Temperature),** aging **End of Life (EOL)**, and, in the case of Space applications, radiation tolerances.



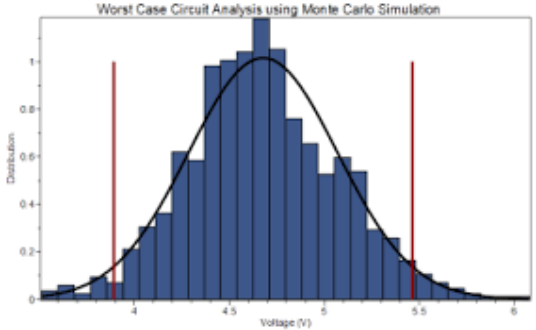
Worst case analysis method types

- **Extreme Value Analysis (EVA)** This is an estimate of the most extreme limits of the circuit's components and function.

- **Root Sum Square (RSS)** method works on a statistical approach. It assumes that most of the components fall to the mid of the tolerance zone rather than at the extreme ends.

$$\Delta Y = \sqrt{\sum_{i=1}^{n} \delta_i^2}$$

- **Monte Carlo analysis**, in which parameters are randomly selected from a distribution, and the circuit simulated, anywhere from 1000 to 100000 times.



Worst case analysis component tolerances

Resistor Tolerances

EOL obtained from component manufacturer, or engineering APL

$delT := 75$

$tol\_rd1\_bol := 0.1 \cdot \%$	$tol\_rd1\_eol := 0.5 \cdot \%$	$tol\_rd1\_temp := 25 \cdot 10^{-6} \cdot delT$	ppm /C
$tol\_rd2\_bol := 1 \cdot \%$	$tol\_rd2\_eol := 0.5 \cdot \%$	$tol\_rd2\_temp := 100 \cdot 10^{-6} \cdot delT$	ppm /C
$tol\_rd3\_bol := 1 \cdot \%$	$tol\_rd3\_eol := 0.5 \cdot \%$	$tol\_rd3\_temp := 250 \cdot 10^{-6} \cdot delT$	ppm /C
$tol\_rd4\_bol := 10 \cdot \%$	$tol\_rd4\_eol := 0.5 \cdot \%$	$tol\_rd4\_temp := 2000 \cdot 10^{-6} \cdot delT$	ppm /C

Variations

$k1 := (tol\_rd1\_bol + tol\_rd1\_eol + tol\_rd1\_temp)$

$k2 := (tol\_rd2\_bol + tol\_rd2\_eol + tol\_rd2\_temp)$

$k1 = 7.875 \cdot 10^{-3}$

$k2 = 0.023$

$xr23 := 53.6 \cdot k$

$xr23min := xr23 \cdot (1 - k1)$

$xr23max := xr23 \cdot (1 + k1)$

$xr23min = 5.318 \cdot 10^{4}$

$xr23max = 5.402 \cdot 10^{4}$

Worst case analysis component tolerances

Capacitor Tolerances

EOL obtained from component manufacturer, or engineering APL

$delT := 75$

$tol\_npo\_bol := 5 \cdot \%$ $tol\_npo\_eol := 0.5 \cdot \%$ $tol\_npo\_temp := 30 \cdot 10^{-6} \cdot delT$

$tol\_bx\_bol := 10 \cdot \%$ $tol\_bx\_eol := 21 \cdot \%$ $tol\_bx\_temp := 15 \cdot \%$

$tol\_x7r\_bol := 10 \cdot \%$ $tol\_x7r\_eol := 21 \cdot \%$ $tol\_x7r\_temp := 15 \cdot \%$

BX characteristics are identical to X7R dielectric, with the added restriction that the Temperature-Voltage Coefficient (TVC) is not to exceed -25% ΔC at rated voltage, over the operating temperature range (-55°C to 125°C).

Variations

$k3 := (tol\_npo\_bol + tol\_npo\_eol + tol\_npo\_temp)$ $k3 = 0.057$

$k4 := (tol\_bx\_bol + tol\_bx\_eol + tol\_bx\_temp)$ $k4 = 0.46$

$k5 := (tol\_x7r\_bol + tol\_x7r\_eol + tol\_x7r\_temp)$ $k5 = 0.46$

$a1c12 := 39 \cdot p$

$a1c12min := a1c12 \cdot (1 - k3)$

$a1c12max := a1c12 \cdot (1 + k3)$

$a1c12min = 3.833 \cdot 10^{-11}$

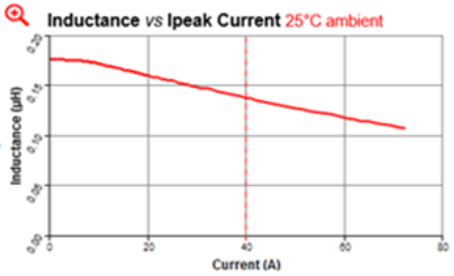
$a1c12max = 3.967 \cdot 10^{-11}$

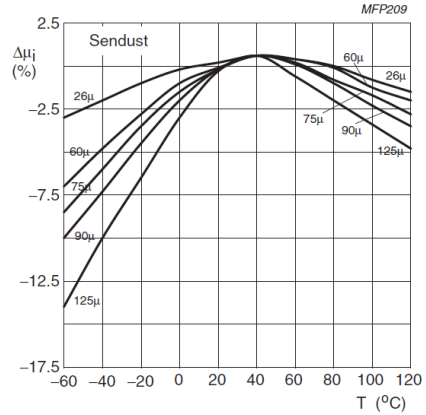
Worst case analysis component tolerances

Inductor Tolerances

5. DC current at 25°C that causes an inductance drop of 30% (typ) from its value without current.

Part number[1]	Inductance[2] ±20% (µH)	DCR (mOhms)[3] typ	DCR (mOhms)[3] max	SRF typ[4] (MHz)	Isat[5] (A)	Irms (A)[6] 20°C rise	Irms (A)[6] 40°C rise
XAL7030-161ME_	0.16	1.15	1.26	158	60.0	24.9	32.5
XAL7030-301ME_	0.30	1.75	1.92	101	41.0	21.0	27.6
XAL7030-601ME_	0.60	3.00	3.30	72	36.0	18.0	23.0
XAL7030-102ME_	1.0	4.55	5.00	52	28.0	16.1	21.8
XAL7030-152ME_	1.5	7.60	8.36	39	23.5	11.9	15.0
XAL7030-222ME_	2.2	13.7	15.07	29	18.0	10.0	12.9
XAL7030-272ME_	2.7	15.7	17.30	32	12.8	9.2	11.4
XAL7030-332ME_	3.3	19.5	21.45	25	12.3	8.0	10.0
XAL7030-472ME_	4.7	26.1	30.00	21	10.1	6.9	9.0
XAL7030-562ME_	5.6	28.1	32.32	17	9.8	5.3	7.3
XAL7030-682ME_	6.8	45.0	51.75	15	8.7	4.4	6.8
XAL7030-822ME_	8.2	53.0	60.94	13	8.4	2.9	5.9
XAL7030-103ME_	10	60.4	69.46	12	7.7	2.6	5.3





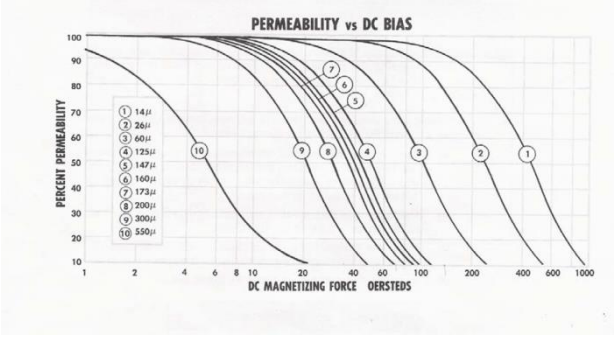


Fig.2 Initial permeability as a function of temperature.

$$L := \frac{.4 \cdot 3.14 \cdot u \cdot turns^2 \cdot (Ae)}{le \cdot 10^8}$$

Where:

Linductance = Henry's

µ = core permeability

N = number of turns

Ae = core cross-section (mm^2)

*l*e = core magnetic path length (mm)

Worst case analysis inductance rolloff example

Example of saturation current

Vin =12V	Vo = .9V
Vinmax = 13.2V	Iomax = 40A
Vinmin = 10.8V	Iomin = 4A
f = 650khz	

Lout = 160nH

I_peak = 45.6A Peak inductor current

Now what happens if I push Iomax to 60A and reduce the inductance by 30%

Vin =12V	Vo = .9V
Vinmax = 13.2V	Iomax = 60A
Vinmin = 10.8V	Iomin = 4A
f = 650khz	

Lout = 112nH

I_peak = 68.7A Peak inductor current

Rule of thumb derate Isat by 30 to 40%

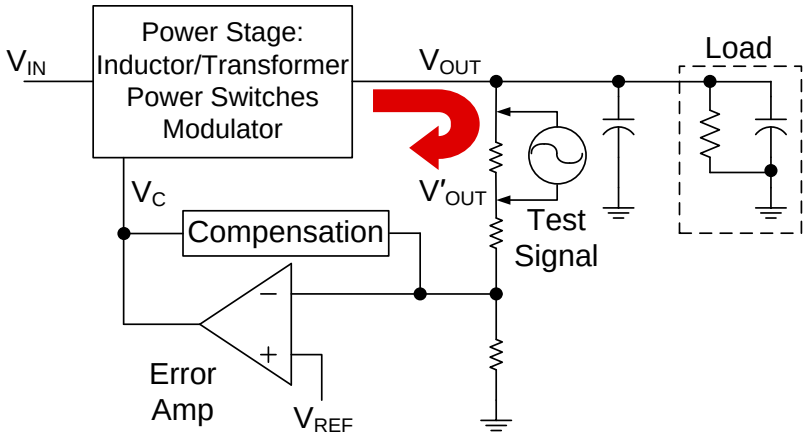
Worst case analysis output regulation example

Problem statement

- What is my worst case output voltage regulation

Procedure

- Find tolerances for Vref, error-amp, and resistor divider.
- Write equation for feedback regulation
- Calculate sensitivity of variables.
- Solve equation



Worst case analysis output regulation example

Reference tolerance

$tol\_TL431\_bol := 0.5 \cdot \%$ $tol\_TL431\_eol := .25 \cdot \%$ $tol\_TL431\_temp := 60 \cdot 10^{-6} \cdot delT$

Reference Variation

$Vref := 2.495$

$TL431vrefmin := Vref \cdot (1 - tol\_TL431\_bol) \cdot (1 - tol\_TL431\_eol) \cdot (1 - tol\_TL431\_temp)$

$TL431vrefmin = 2.465$

$TL431vrefmax := Vref \cdot (1 + tol\_TL431\_bol) \cdot (1 + tol\_TL431\_eol) \cdot (1 + tol\_TL431\_temp)$

$TL431vrefmax = 2.525$

- Reference Voltage Tolerance at 25°C
  - 0.5% (B Grade)
  - 1% (A Grade)
  - 2% (Standard Grade)

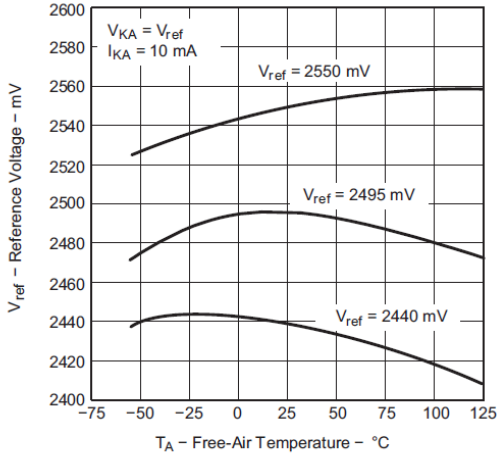


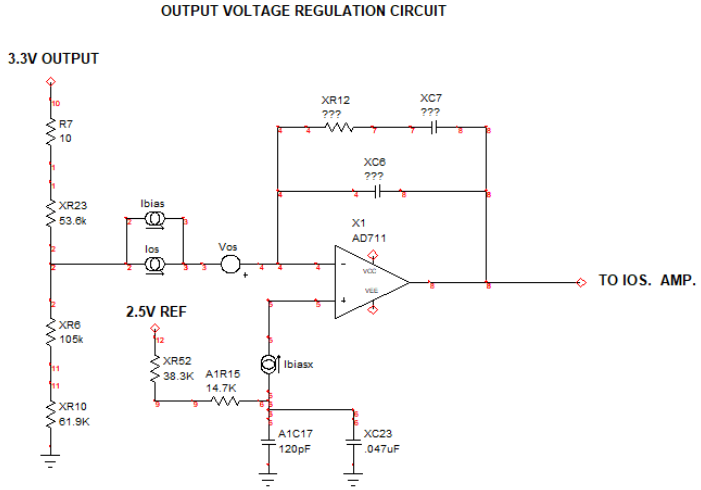
Figure 1. Reference Voltage vs Free-Air Temperature

Worst case analysis output regulation example

Op-amp tolerance

Op-amp dc error sources include:

- Input offset voltage VOS
- Input bias current IB
- Input offset current IOS
- Open loop gain



From LM158 Data sheet:
Vos_bol = 7mV from -55c to 125c
Vos_temp = 15uV/c
Vos_eol = hard to find check with Manufacturer

Ib_bol = 300nA from -55c to 125c,
Ios_bol = 100nA from -55c to 125c
Ios_temp = 200pA/c, Ios_eol = hard to find check with Manufacturer

Open loop gain min = 35V/mV =35000 Open loop gain typ = 140V/mV = 140000

Worst case analysis output regulation example

Below is a sensitivity calculation to show which parts should be minimized or maximized

$$Vonom(Vref, Vos, Vbiasnom, Vbias\_gainnom, xr23, r7, xr10, xr6) := \begin{pmatrix} Vref + Vos \ ... \\ + Vbiasnom \ ... \\ + Vbias\_gainnom \end{pmatrix} \cdot \frac{(xr23 + r7 + xr10 + xr6)}{xr10 + xr6}$$

$$\frac{d}{dVref} Vonom(Vref, Vos, Vbiasnom, Vbias\_gainnom, xr23, r7, xr10, xr6) = 1.321$$

$$\frac{d}{dVos} Vonom(Vref, Vos, Vbiasnom, Vbias\_gainnom, xr23, r7, xr10, xr6) = 1.321$$

$$\frac{d}{dVbiasnom} Vonom(Vref, Vos, Vbiasnom, Vbias\_gainnom, xr23, r7, xr10, xr6) = 1.321$$

$$\frac{d}{dVbias\_gainnom} Vonom(Vref, Vos, Vbiasnom, Vbias\_gainnom, xr23, r7, xr10, xr6) = 1.321$$

$$\frac{d}{dxr23} Vonom(Vref, Vos, Vbiasnom, Vbias\_gainnom, xr23, r7, xr10, xr6) = 1.504 \cdot 10^{-5}$$

$$\frac{d}{dr7} Vonom(Vref, Vos, Vbiasnom, Vbias\_gainnom, xr23, r7, xr10, xr6) = 1.504 \cdot 10^{-5}$$

$$\frac{d}{dxr10} Vonom(Vref, Vos, Vbiasnom, Vbias\_gainnom, xr23, r7, xr10, xr6) = -4.83 \cdot 10^{-6}$$

$$\frac{d}{dxr6} Vonom(Vref, Vos, Vbiasnom, Vbias\_gainnom, xr23, r7, xr10, xr6) = -4.83 \cdot 10^{-6}$$

Worst case analysis output regulation example

Resistor divider tolerance

$$Reqmax := \frac{1}{\left(\frac{1}{xr23max + r7max} + \frac{1}{xr10min + xr6min}\right)}$$

$Reqmax = 4.074 \cdot 10^{4}$

$a1r15max = 1.503 \cdot 10^{4}$

$$Reqmin := \frac{1}{\left(\frac{1}{xr23min + r7min} + \frac{1}{xr10max + xr6max}\right)}$$

$Reqmin = 4.041 \cdot 10^{4}$

$a1r15min = 1.437 \cdot 10^{4}$

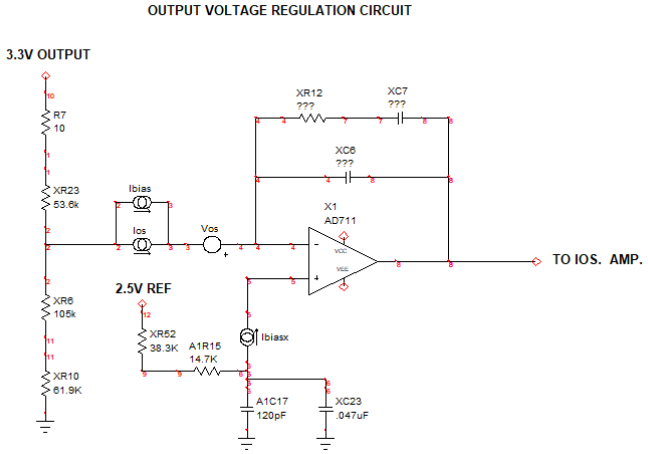
Worst case analysis output regulation example

Voltage error due to the offset current, bias current, A1r15 and Req

$Vbiasmin := Reqmin \cdot (Ibias - Ios) - Ibias \cdot (a1r15max + xr52max)$ $\quad Vbiasmin = -6.685 \cdot 10^{-4}$

$Vbiasmax := Reqmax \cdot (Ibias + Ios) - Ibias \cdot (a1r15min + xr52min)$ $\quad Vbiasmax = 1.748 \cdot 10^{-4}$

$Vbiasnom := \frac{Vbiasmax + Vbiasmin}{2}$ $\quad Vbiasnom = -2.469 \cdot 10^{-4}$



Voltage error due to the gain in the error amplifier

Vout = (Vpos - Vneg) x Av **Vin = Vpos - Vneg** **Vbias gain = Vin**

$voh := 5$ **Voh is the Vdd voltage on the error amp. therefore the maximum ouput voltage on the error amp.**

$Vbias\_gainmax := \frac{voh}{OLGmin}$ $\quad Vbias\_gainmax = 1.429 \cdot 10^{-4}$

$Vbias\_gainmin := \frac{voh}{OLGmax}$ $\quad Vbias\_gainmin = 3.571 \cdot 10^{-5}$

This is the min. and max. voltage required for op-amp operation

$Vbias\_gainnom := \frac{Vbias\_gainmax + Vbias\_gainmin}{2}$ $\quad Vbias\_gainnom = 8.929 \cdot 10^{-5}$

Worst case analysis output regulation example

The total output voltage error due to Vref, Vos, Vbias, Req, and A1r15

$$Vomax := (vrefmax + Vos + Vbiasmax + Vbias\_gainmax)\cdot\frac{(xr23max + r7max + xr10min + xr6min)}{xr10min + xr6min} \qquad Vomax = 3.37$$

$$Vomin := (vrefmin - Vos + Vbiasmin + Vbias\_gainmin)\cdot\frac{(xr23min + r7min + xr10max + xr6max)}{xr10max + xr6max} \qquad Vomin = 3.236$$

The percent delta for Vout is as follows

$$Vonom := 3.3$$

$$Vodelta\%pos := \frac{Vomax - Vonom}{Vonom}\cdot 100 \qquad Vodelta\%pos = 2.126$$

$$Vodelta\%neg := \frac{Vonom - Vomin}{Vonom}\cdot 100 \qquad Vodelta\%neg = 1.926$$

Worst case analysis MOSFET power dissipation example

Problem statement

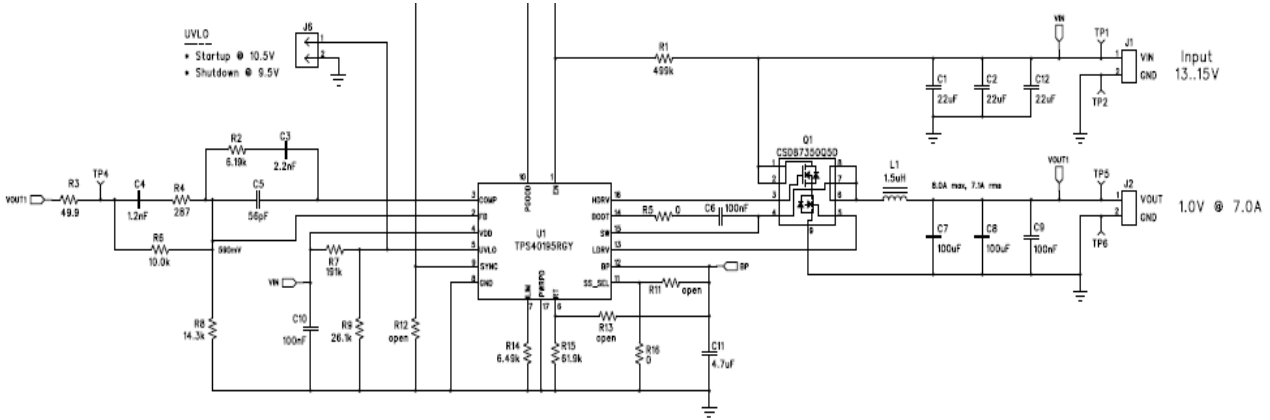
- The FET's in my PS are getting hot

Possible causes

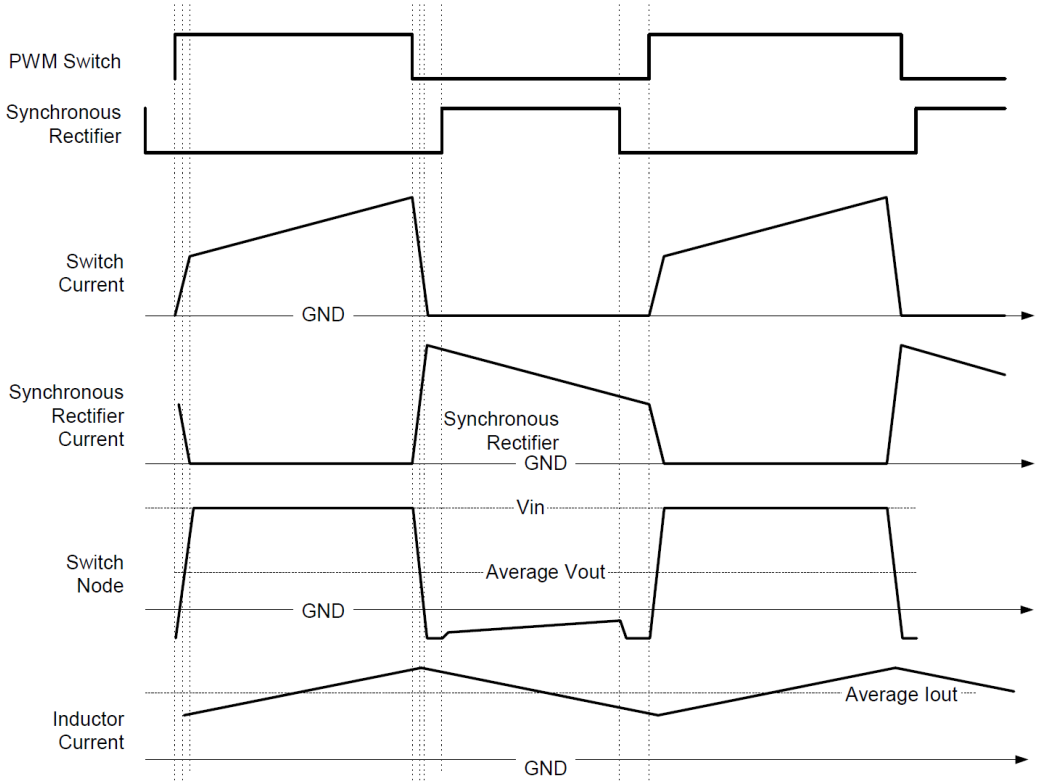
- Not enough heat sink
- Shoot through

Solution

- WCA on FET power dissipation



Worst case analysis MOSFET power dissipation example



Procedure

- Find tolerances for Rds, Qg total gate charge, Qgs charge gate to source, Qgd charge gate to drain, Qoss output charge, body drain diode forward voltage, and controller dead time.
- Write equation and Analyze Rds conducted losses, switching loss, and gate drive loss for top FET.
- Write equation and Analyze Rds conducted losses, body drain diode loss, and gate drive loss for bottom FET
- Add up all losses

Worst case analysis component tolerances

MOSFET tolerance

CSD87350Q5D Synchronous Buck NexFET™ Power Block

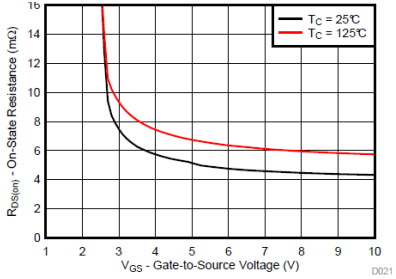


Figure 20. Control MOSFET $R_{DS(on)}$ vs V_{GS}

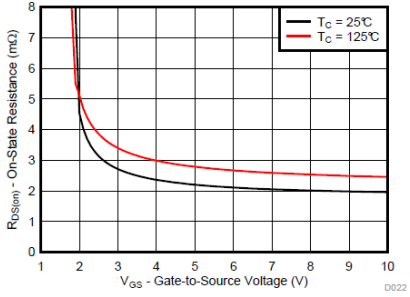


Figure 21. Sync MOSFET $R_{DS(on)}$ vs V_{GS}

Rds goes up as temp goes up

Rds_bol = 20%

Rds_tempmax = 63%

Rds_tempmin = -40%

$Rdson\_top := 5 \cdot 10^{-3} \cdot \Omega$

$Rdsmin\_top = 2.4 \times 10^{-3}\,\Omega$

$Rdsmax\_top = 9.78 \times 10^{-3}\,\Omega$

$Rdson\_bot := 1.2 \cdot 10^{-3} \cdot \Omega$

$Rdsmin\_bot = 5.76 \times 10^{-4}\,\Omega$

$Rdsmax\_bot = 2.347 \times 10^{-3}\,\Omega$

Total gate charge

$qtotal\_top := 8.4nC$

$qtotal\_bol := 30\%$

$qtotal\_bot := 20nC$

$qtotal\_min\_top = 5.88 \times 10^{-9}\,C$

$qtotal\_max\_top = 1.092 \times 10^{-8}\,C$

$qtotal\_min\_bot = 1.4 \times 10^{-8}\,C$

$qtotal\_max\_bot = 2.6 \times 10^{-8}\,C$

Gate charge gate to drain and gate to source

$Qgd\_top := 1.6nC$

$Qgd\_bol := 30\%$

$Qgs\_top := 2.6nC$

$Qgs\_bol := 30\%$

$Qgd\_min\_top = 1.12 \times 10^{-9}\,C$

$Qgd\_max\_top = 2.08 \times 10^{-9}\,C$

$Qgs\_min\_top = 1.82 \times 10^{-9}\,C$

$Qgs\_max\_top = 3.38 \times 10^{-9}\,C$

Worst case analysis component tolerances

MOSFET tolerance

Qoss output charge

Qoss_bol := 30%

Qoss_top := 9.7nC

$Qoss\_min\_top = 6.79 \times 10^{-9} C$

$Qoss\_max\_top = 1.261 \times 10^{-8} C$

Qoss_bot := 28nC

$Qoss\_min\_bot = 1.96 \times 10^{-8} C$

$Qoss\_max\_bot = 3.64 \times 10^{-8} C$

Body drain diode forward voltage

Vbody := .8V

Vbody_bol := 25%

Vbody_temphot := 30% At 125C

Vbody_tempcold := 22.5% At -50C

$Vbody\_max = 1.3\,V$

$Vbody\_min = 0.42\,V$

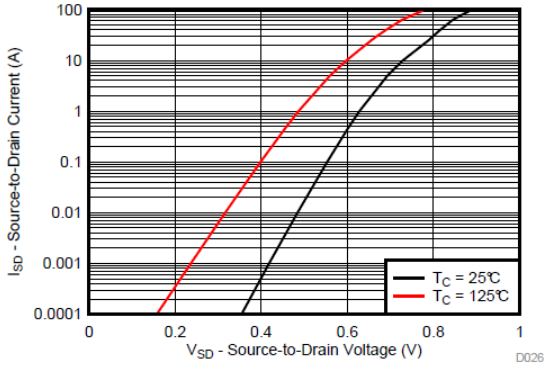


Figure 25. Sync MOSFET Body Diode

Worst case analysis component tolerances

TPS40190 Controller dead time tolerance for body diode PWR calculation

Deadtime_HSoff_LSon := 50ns Deadtime_LSoff_HSon := 25ns DT_bol := 20%

Deadtime_HSoff_LSon_min = 4×10^{-8} s Deadtime_LSoff_HSon_min = 2×10^{-8} s

Deadtime_HSoff_LSon_max = 6×10^{-8} s Deadtime_LSoff_HSon_max = 3×10^{-8} s

Power block delay time tolerance for body diode PWR calculation

Td_FET_bol := 30% Turnon_dly_HS := 7ns Turnon_dly_LS := 8ns Turnoff_dly_HS := 13ns Turnoff_dly_LS := 33ns

Trise_HS := 17ns Trise_LS := 10ns Tfall_HS := 2.3ns Tfall_LS := 4.7ns

Turnon_dly_HSmin = 4.9×10^{-9} s Trise_HSmin = 1.19×10^{-8} s Turnoff_dly_HSmin = 9.1×10^{-9} s Tfall_HSmin = 1.61×10^{-9} s

Turnon_dly_HSmax = 9.1×10^{-9} s Trise_HSmax = 2.21×10^{-8} s Turnoff_dly_HSmax = 1.69×10^{-8} s Tfall_HSmax = 2.99×10^{-9} s

Turnon_dly_LSmin = 5.6×10^{-9} s Trise_LSmin = 7×10^{-9} s Turnoff_dly_LSmin = 2.31×10^{-8} s Tfall_LSmin = 3.29×10^{-9} s

Turnon_dly_LSmax = 1.04×10^{-8} s Trise_LSmax = 1.3×10^{-8} s Turnoff_dly_LSmax = 4.29×10^{-8} s Tfall_LSmax = 6.11×10^{-9} s

Worst case analysis MOSFET power dissipation example

1) First calculate conducted loss

$Irms\_top\_fet = 10.462\,A$

$Pfet\_cond\_topmax := Irms\_top\_fet^2 \cdot Rdsmax\_top$ $\quad Pfet\_cond\_topmax = 1.07 \cdot W$ (Cond losses)

$Pfet\_cond\_topmin := Irms\_top\_fet^2 \cdot Rdsmin\_top$ $\quad Pfet\_cond\_topmin = 0.263 \cdot W$ (Cond losses)

$Irms\_bot\_fet = 38.677\,A$

$Pfet\_cond\_botmax := Irms\_bot\_fet^2 \cdot Rdsmax\_bot$ $\quad Pfet\_cond\_botmax = 3.511\,W$ (Cond losses)

$Pfet\_cond\_botmin := Irms\_bot\_fet^2 \cdot Rdsmin\_bot$ $\quad Pfet\_cond\_botmin = 0.862\,W$ (Cond losses)

2) Calculate top FET switching loss

$Ig := 1A$

$$Psw\_fet\_top := Vinmax \cdot fmax \cdot \left[\frac{Ipfet\_top \cdot (Qgd\_max\_top + Qgs\_max\_top)}{Ig} + \frac{Qoss\_max\_top + Qoss\_max\_bot}{2} \right]$$ $Psw\_fet\_top = 1.502\,W$ (Switching losses)

$Tsw := 18 \cdot ns$

$$Pd\_SW\_FET := 2 \cdot \left[\frac{1}{Tmin} \cdot \int_0^{Tsw} \left(Vinmax \cdot \frac{t}{Tsw} \right) \cdot \left[Ipfet\_top \cdot \left(1 - \frac{t}{Tsw} \right) \right] dt \right]$$ $Pd\_SW\_FET = 1.517 \cdot W$ (Switching losses)

Bottom FET has body diode voltage across it at turn on/off therefore loss is in the body diode

Worst case analysis MOSFET power dissipation example

3) calculate gate drive losses

PARAMETER		TEST CONDITIONS	Q1 CONTROL FET			Q2 SYNC FET			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
R_G	Series gate resistance			1.3	3		0.8	2	Ω

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT DRIVERS						
R_{HDHI}	High-side driver pull-up resistance	V_{BOOT} - V_{SW} = 4.5 V, I_{HDRV} = -100 mA		3	6	Ω
R_{HDLO}	High-side driver pull-down resistance	V_{BOOT} - V_{SW} = 4.5 V, I_{HDRV} = 100 mA		1.5	3	Ω
R_{LDHI}	Low-side driver pull-up resistance	I_{LDRV} = -100 mA		2.5	5	Ω
R_{LDLO}	Low-side driver pull-down resistance	I_{LDRV} = 100 mA		0.8	1.5	Ω

$Vgate := 8V$

$Pg\_dr\_top := f \cdot qtotal\_max\_top \cdot Vgate$ $\quad Pg\_dr\_top = 0.028\,W$ (Gate losses)

$Act\_gate\_drive\_pwr\_top := \frac{1.3}{3} \cdot Pg\_dr\_top$ $\quad Act\_gate\_drive\_pwr\_top = 0.012\,W$

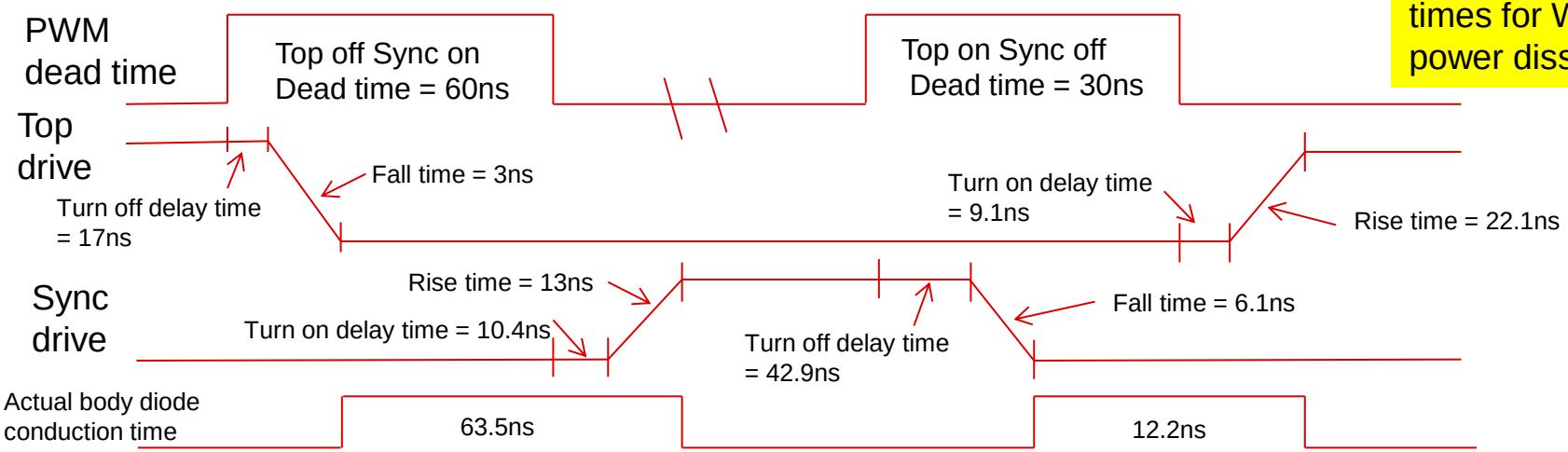
$Pg\_dr\_bot := f \cdot qtotal\_max\_bot \cdot Vgate$ $\quad Pg\_dr\_bot = 0.068\,W$ (Gate losses)

$Act\_gate\_drive\_pwr\_LS := \frac{.8}{2.5} \cdot Pg\_dr\_bot$ $\quad Act\_gate\_drive\_pwr\_LS = 0.022\,W$

Worst case analysis MOSFET power dissipation example

3) Calculate body diode losses

Used maximum times for WC power dissipation



$$Tdelay1 := Deadtime\_HSoff\_LSon\_max - Turnoff\_dly\_HSmax - Tfall\_HSmax + Turnon\_dly\_LSmax + Trise\_LSmax \qquad Tdelay1 = 6.351 \times 10^{-8}\,s$$

$$Tdelay2 := Deadtime\_LSoff\_HSon\_max - Turnoff\_dly\_LSmax - Tfall\_LSmax + Turnon\_dly\_HSmax + Trise\_HSmax \qquad Tdelay2 = 1.219 \times 10^{-8}\,s$$

$$Pbody\_diode\_max := Vbody\_min \cdot Iomax \cdot \frac{Tdelay1 + Tdelay2}{Tmin} \qquad Pbody\_diode\_max = 0.475\,W$$

Worst case analysis MOSFET power dissipation example

4) Add up all the top and bottom FET losses

$$Pfet\_tot\_top\_min := Pfet\_cond\_topmin + Psw\_fet\_top + Act\_gate\_drive\_pwr\_top$$

$$Pfet\_tot\_top\_min = 1.777\,W$$ (Total top FET losses Cond min)

$$Pfet\_tot\_top\_max := Pfet\_cond\_topmax + Psw\_fet\_top + Act\_gate\_drive\_pwr\_top$$

$$Pfet\_tot\_top\_max = 2.584\,W$$ (Total top FET losses max)

$$Pfet\_tot\_bot\_min := Pfet\_cond\_botmin + Act\_gate\_drive\_pwr\_LS + Pbody\_diode\_max$$

$$Pfet\_tot\_bot\_min = 1.359\,W$$ (Total bottom FET losses cond min)

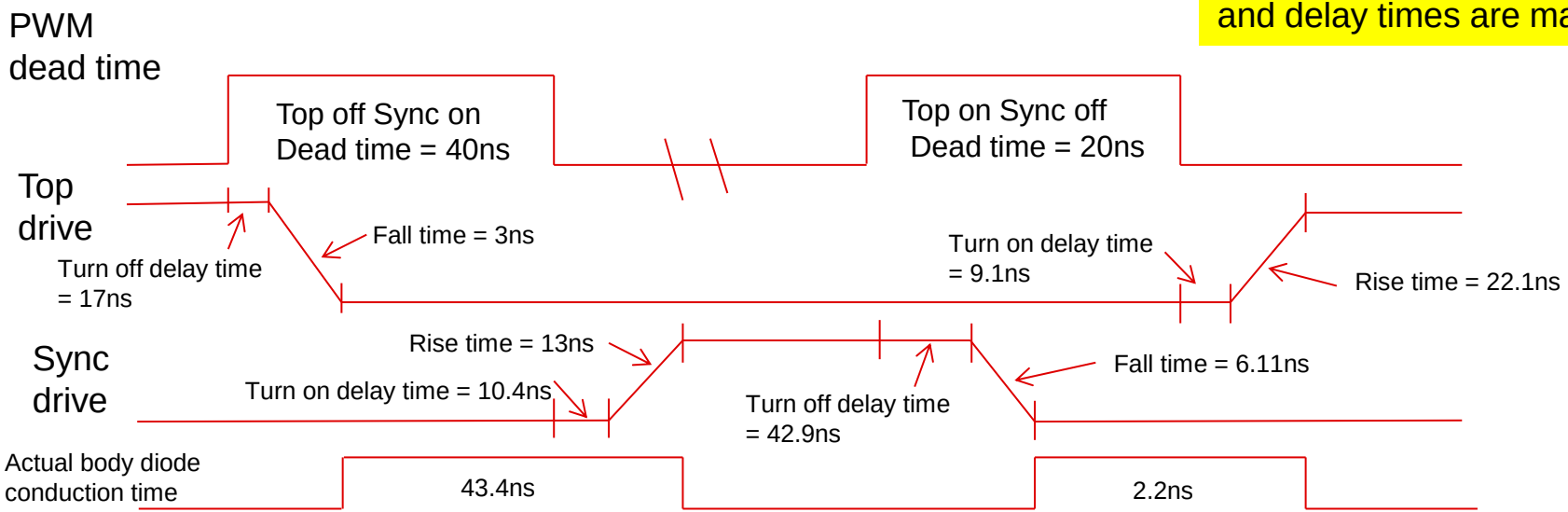
$$Pfet\_tot\_bot\_max := Pfet\_cond\_botmax + Act\_gate\_drive\_pwr\_LS + Pbody\_diode\_max$$

$$Pfet\_tot\_bot\_max = 4.008\,W$$ (Total bottom FET losses max)

Worst case analysis MOSFET

Cross conduction and Timing issues

Look at what happens
when dead time is minimum
and delay times are maximum



Worst case analysis BJT transistor example

Problem statement

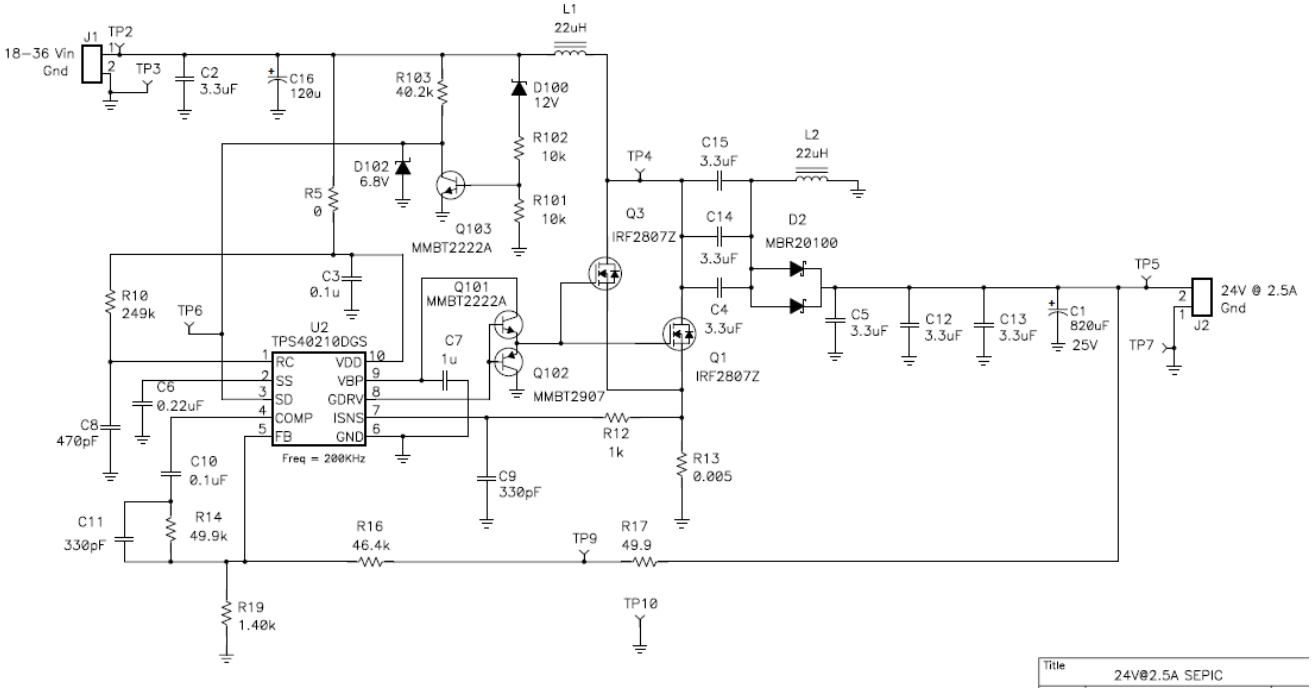
- My PS wont turn on at cold temperature

Possible causes

- Not enough start up voltage/current
- Enable circuit
- Not enough gate drive

Solution

- WCA Enable circuit



Worst case analysis BJT transistor example

Procedure

- Calculate base current
- Calculate collector current
- Calculate necessary Beta to maintain transistor in on state

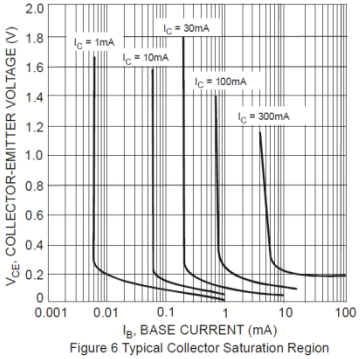


Figure 6 Typical Collector Saturation Region

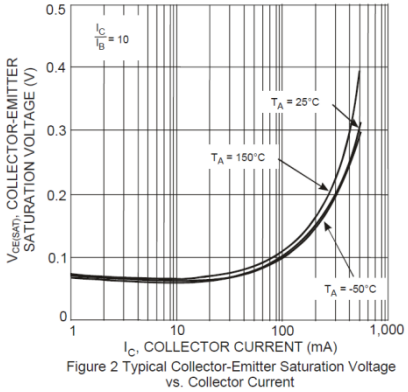


Figure 2 Typical Collector-Emitter Saturation Voltage vs. Collector Current

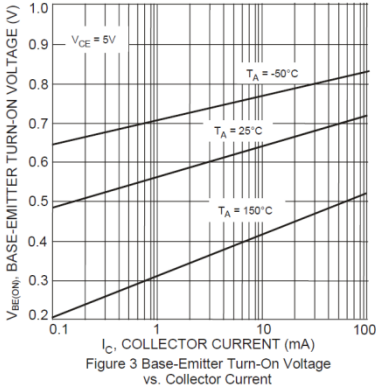


Figure 3 Base-Emitter Turn-On Voltage vs. Collector Current

Resistor Variations

$tol\_res\_bol := 1 \cdot \%$ $tol\_res\_eol := 0.5 \cdot \%$ $tol\_res\_temp := 100 \cdot 10^{-6} \cdot delT$

$R101 := 10 \cdot K\Omega$ $R102 := 10 \cdot K\Omega$ $R103 := 40.2 \cdot K\Omega$

$R101min = 9.8 \times 10^{3}\,\Omega$ $R102min = 9.8 \times 10^{3}\,\Omega$ $R103min = 3.94 \times 10^{4}\,\Omega$

$R101max = 1.02 \times 10^{4}\,\Omega$ $R102max = 1.02 \times 10^{4}\,\Omega$ $R103max = 4.1 \times 10^{4}\,\Omega$

Voltage tolorances

$Vinmin2 := 18V$ $Vinmax2 := 36V$ $Vbesatmin := .6V$ $Vbesatmax := 1.2V$

$Vcesatmax := .3V$ $VD100max := 12.6V$

$$Ibmin := \frac{Vinmin2 - VD100max - Vbesatmax}{R102max}$$

$Ibmin = 4.118 \times 10^{-4}\,A$

$$ICmax := \frac{Vinmin2 - Vcesatmax}{R103min}$$

$ICmax = 4.493 \times 10^{-4}\,A$

Worst case analysis BJT transistor example

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Max	Unit	Test Condition
ON CHARACTERISTICS (Note 10)					
DC Current Gain	h_{FE}	35 50 75 100 40 50 35	— — — 300 — — —	—	I_C = 100µA, V_{CE} = 10V I_C = 1.0mA, V_{CE} = 10V I_C = 10mA, V_{CE} = 10V I_C = 150mA, V_{CE} = 10V I_C = 500mA, V_{CE} = 10V I_C = 10mA, V_{CE} = 10V, T_A = -55°C I_C = 150mA, V_{CE} = 1.0V
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	—	0.3 1.0	V	I_C = 150mA, I_B = 15mA I_C = 500mA, I_B = 50mA
Base-Emitter Saturation Voltage	$V_{BE(SAT)}$	0.6 —	1.2 2.0	V	I_C = 150mA, I_B = 15mA I_C = 500mA, I_B = 50mA

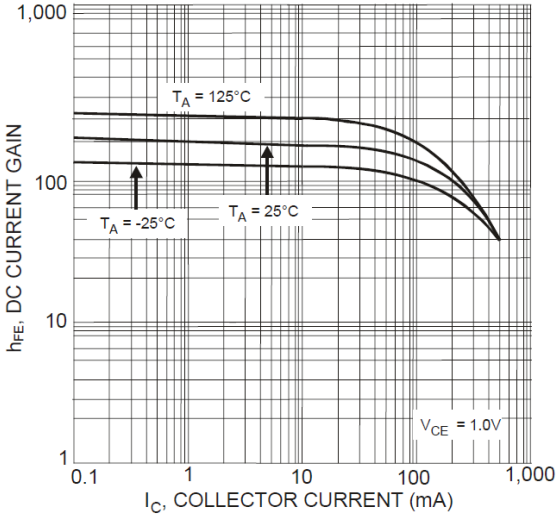


Figure 1 Typical DC Current Gain vs. Collector Current

$$B := \frac{ICmax}{Ibmin} \qquad B = 1.091$$

Summary

- Analyze the circuit to determine potential issues in the design
- Decide what type of analysis needs to be performed - EV, RSS, Monte Carlo
- Write an equation for the potential issues you found
- Determine the variables in each equation
- Determine the BOL, EOL, and temp tolerances for each variable from the manufactures DS or company APL
- Calculate the tolerances for each
- Calculate the behavioral equations using the variable tolerances to determine the worst case parameters for your design

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