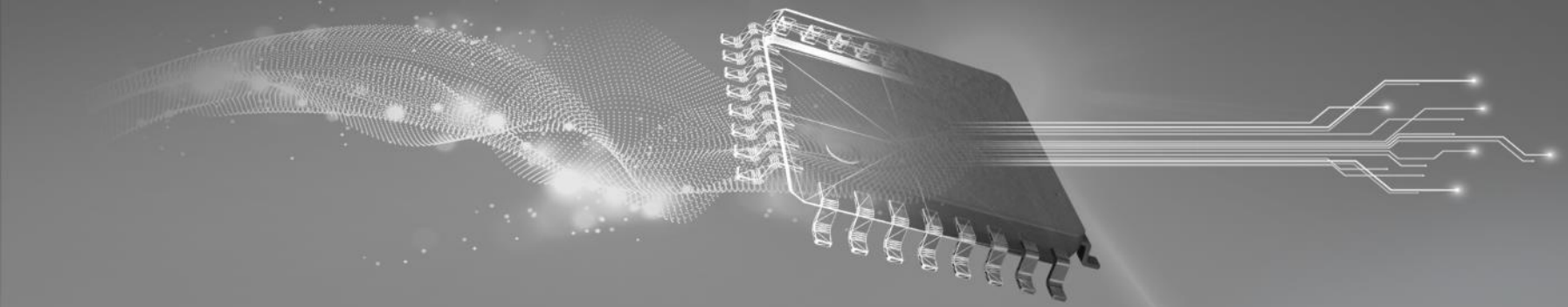
TI TECH DAYS



How to resolve op-amp stability issues using SPICE simulations

Presented by Marek Lis

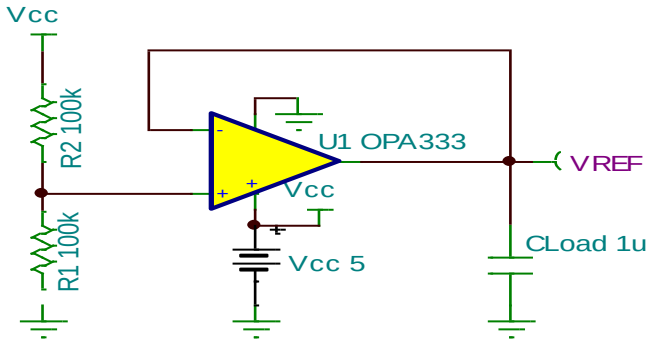
High Precision Products

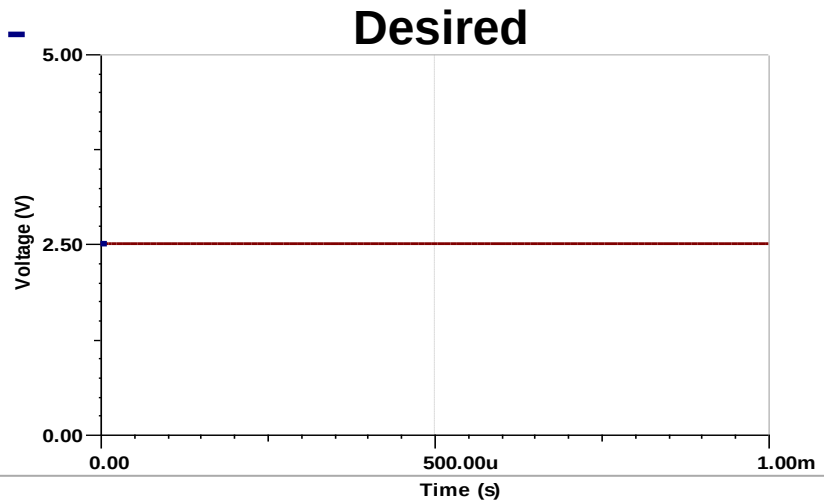
Speaker: Marek Lis

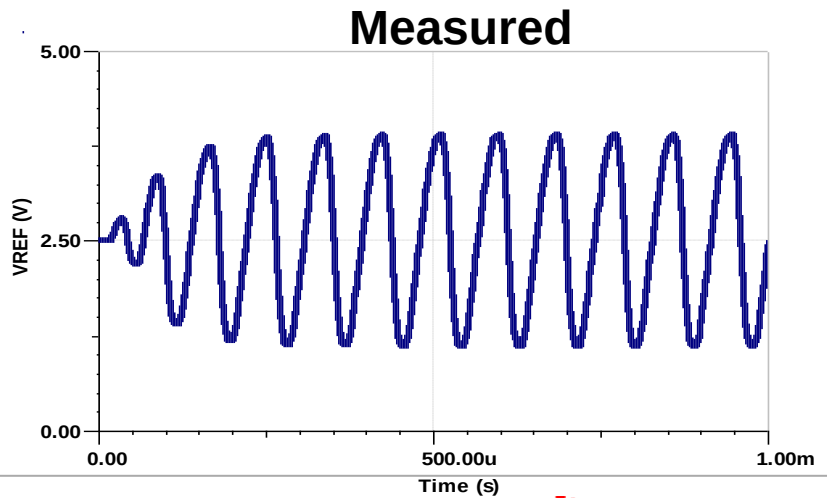
- Senior analog applications engineer on PA team
- Supports:
  - Operational amplifiers
  - Voltage references
  - Macro-models
  - Long-term stability
  - Statistical guarantee of specs

- Worked for ten years at Burr-Brown Corporation as an analog IC design engineer
- Designed over 20 new products from op amps to voltage LDO regulators
- Managed development of series voltage references and instrumentation amplifiers
- Co-invented Green-Lis op amp macro-model; state-of-the-art PSpice-based architecture
- Studied electrical engineering at the University of Michigan and the University of Arizona

Op amp stability issue

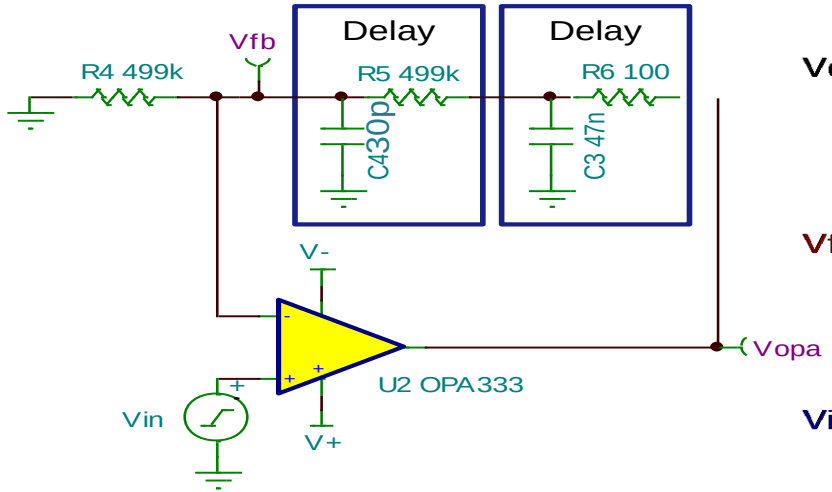


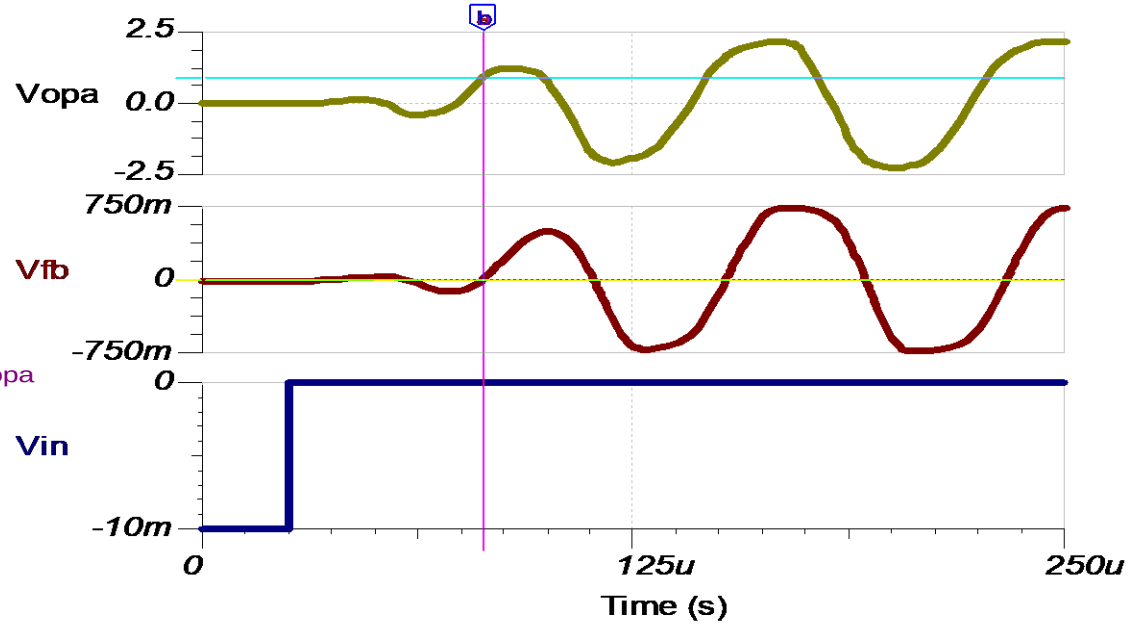




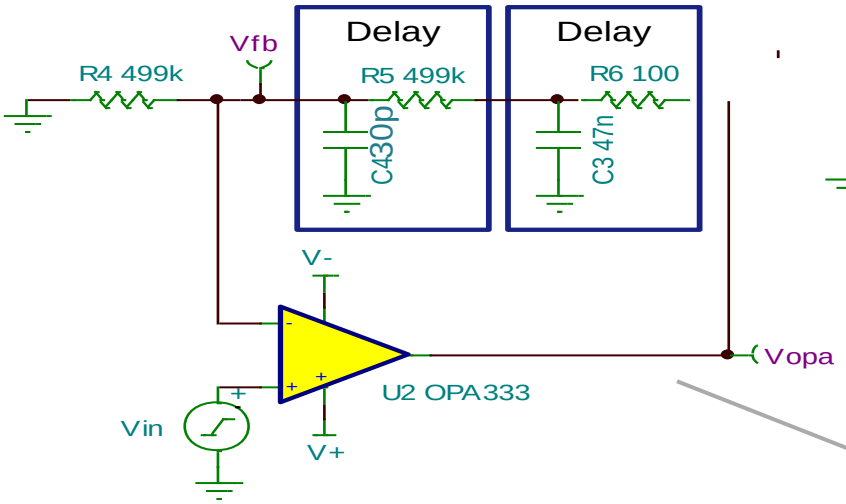
Simplified cause of op amp stability issues

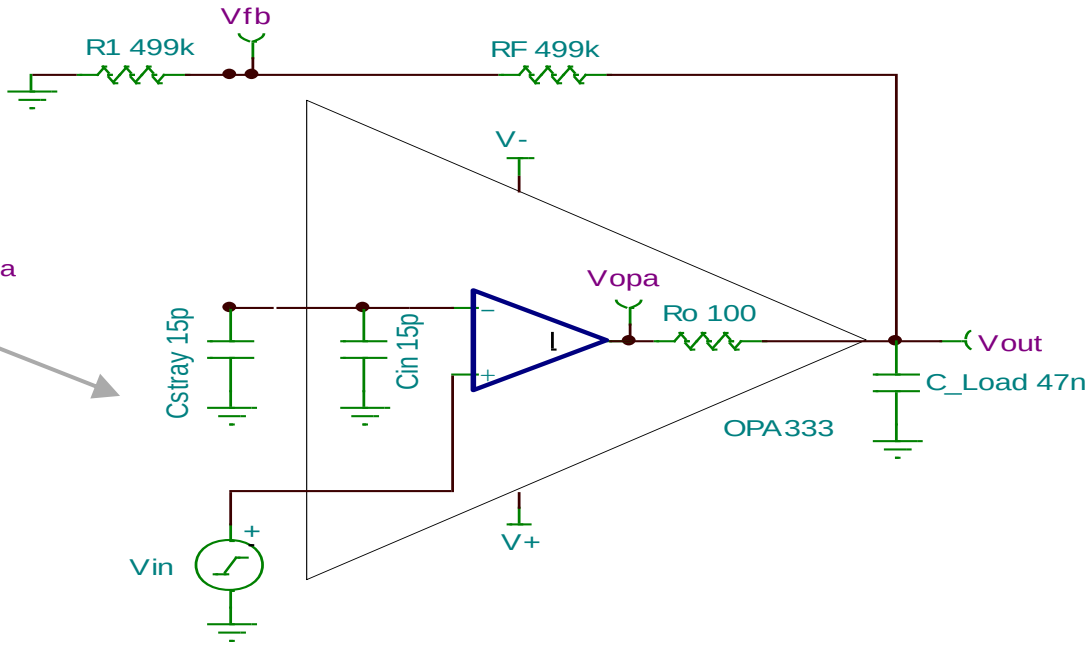
Issues happen because of too much delay from output to feedback!





Delay happens in many circuits

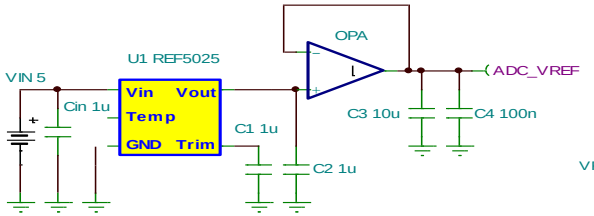




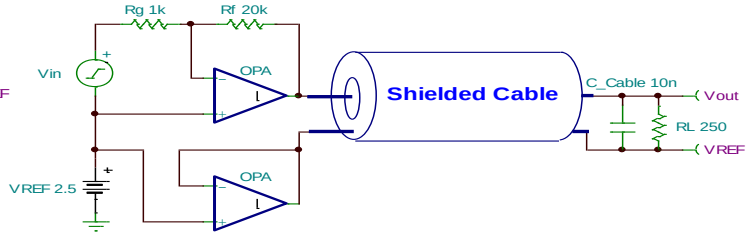
Circuits with possible stability issues

Output capacitive loads

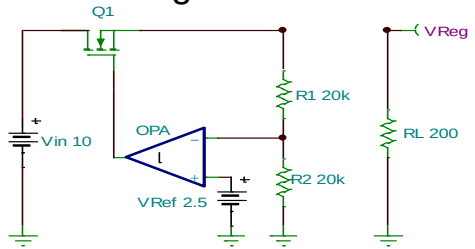
Reference buffers



Cable/shield drive

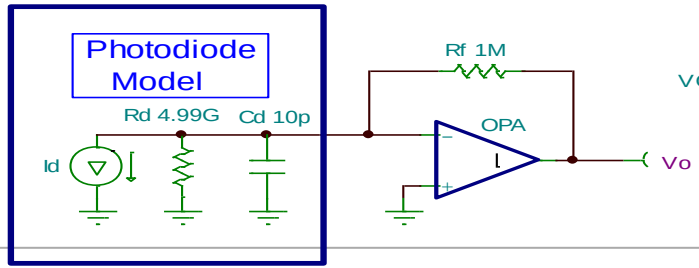


MOSFET gate drive

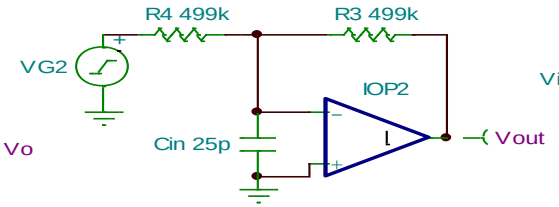


Input capacitance and large value resistors

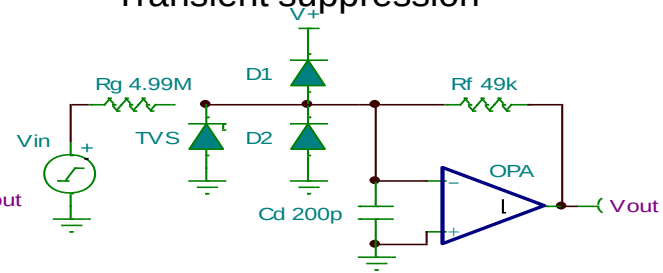
Transimpedance amplifiers



Large value resistors for low-power circuits



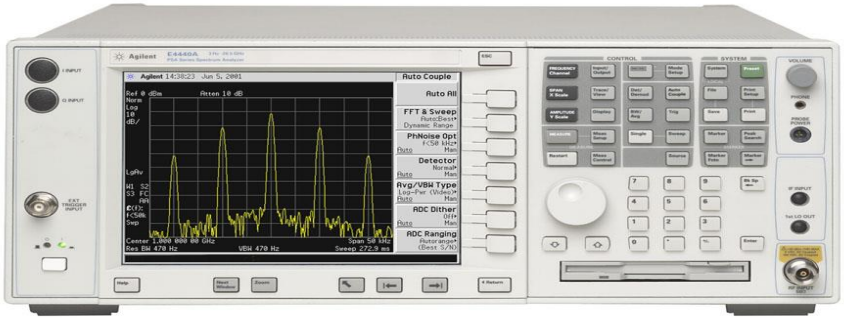
Transient suppression



Identify stability issues in the lab

- Suggested tools:
  - Oscilloscope
  - Signal generator

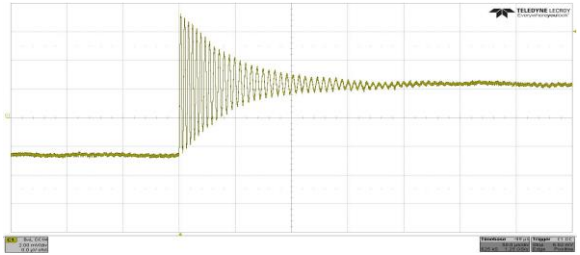
- Other useful tools:
  - Gain / phase analyzer



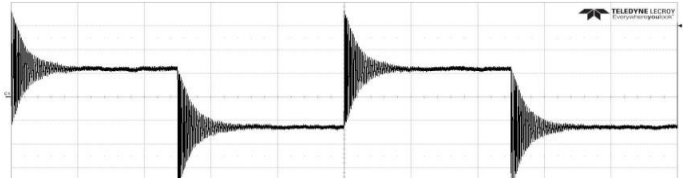
Identify stability issues in the lab

- Oscilloscope – time domain analysis:
  - Oscillations
  - Overshoot and ringing
  - Unstable DC voltages
  - High distortion

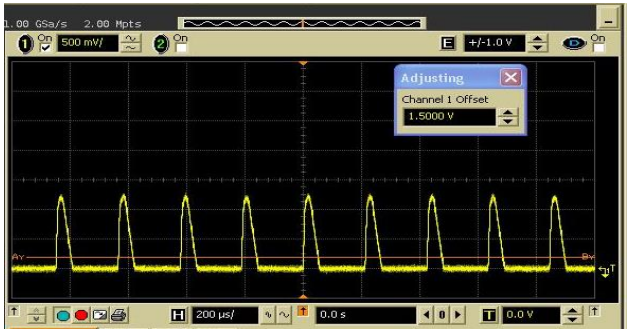
Output response to step input

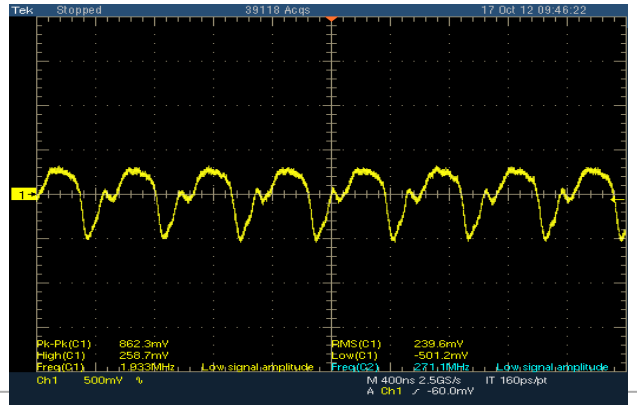


Output response to square wave input



Sustained output oscillation with DC input



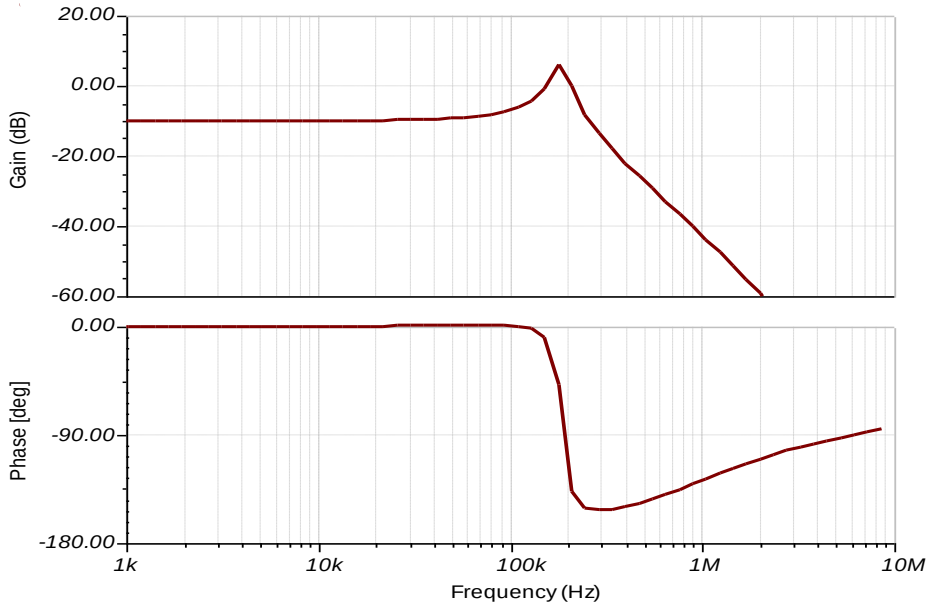


Identify stability issues in the lab

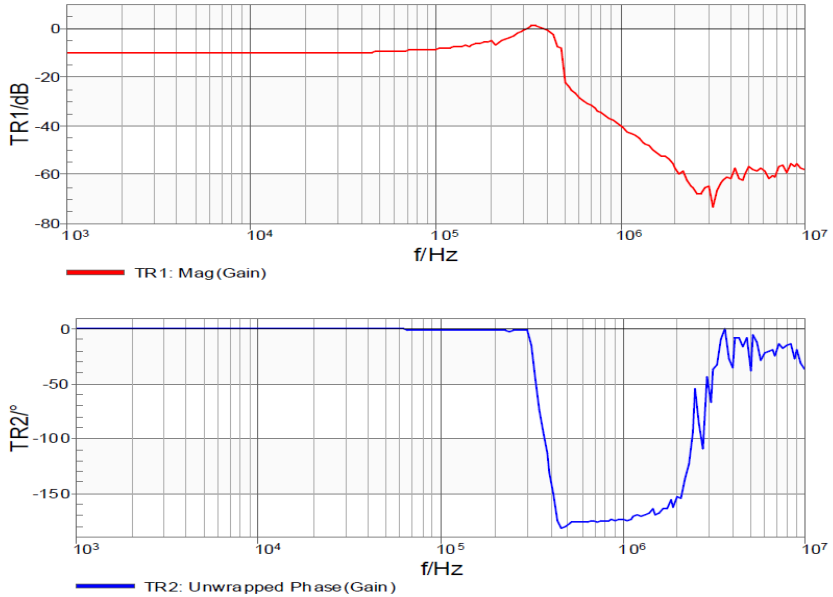
- Gain / phase analyzer – frequency domain:

  - Peaking, unexpected gains, rapid phase shifts

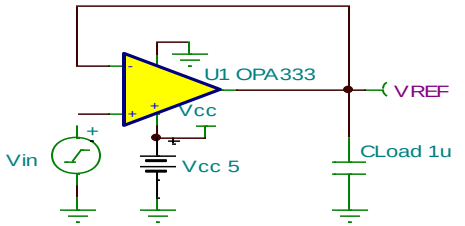
Simulated

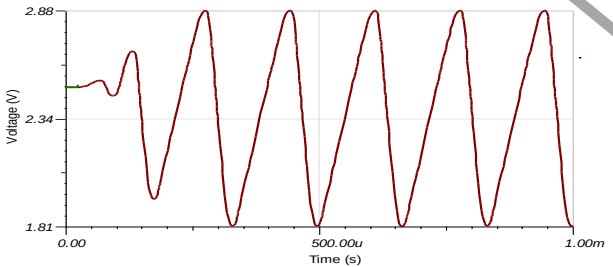


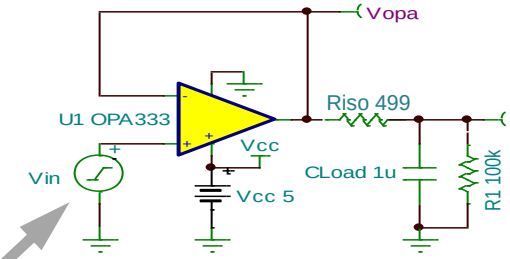
Measured

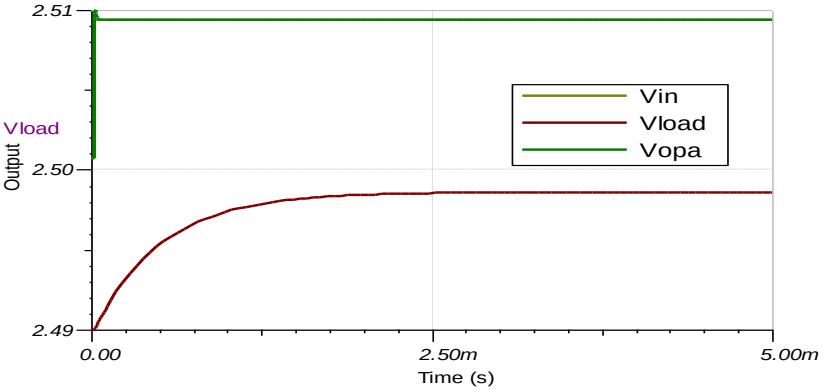


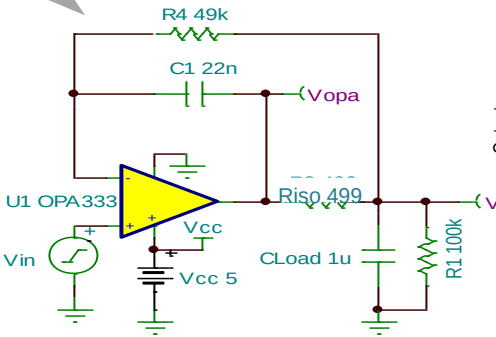
Solving op amp stability issues

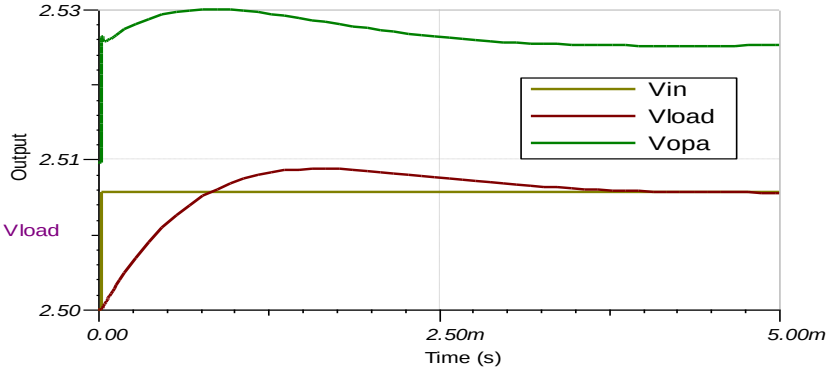




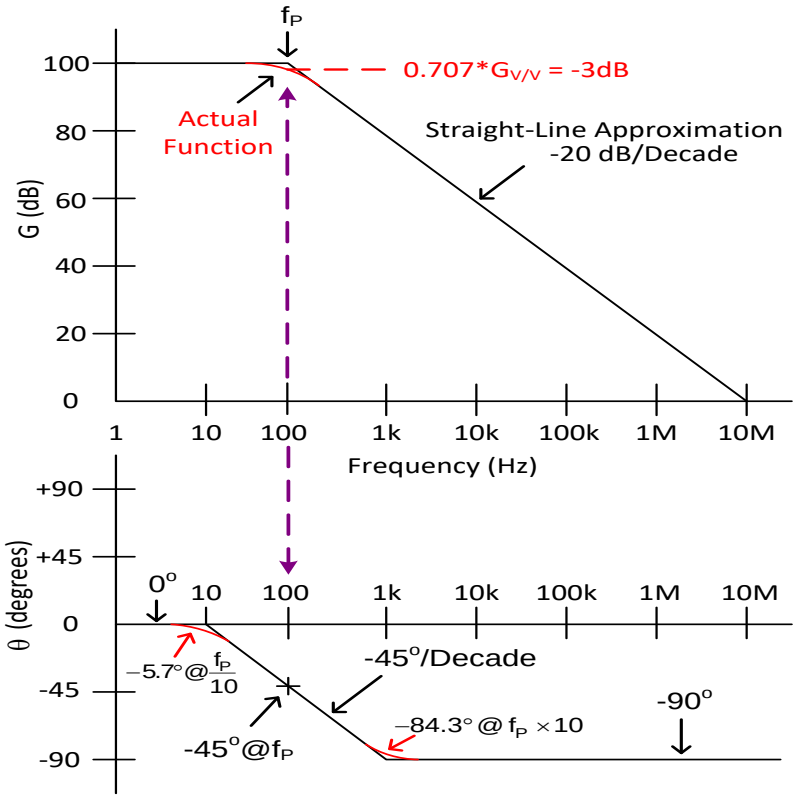








Bode plots – pole



$$G_{v/v} = \frac{V_{out}}{V_{in}} = \frac{G_{dc}}{i\left(\frac{f}{f_P}\right) + 1}$$ As a complex number

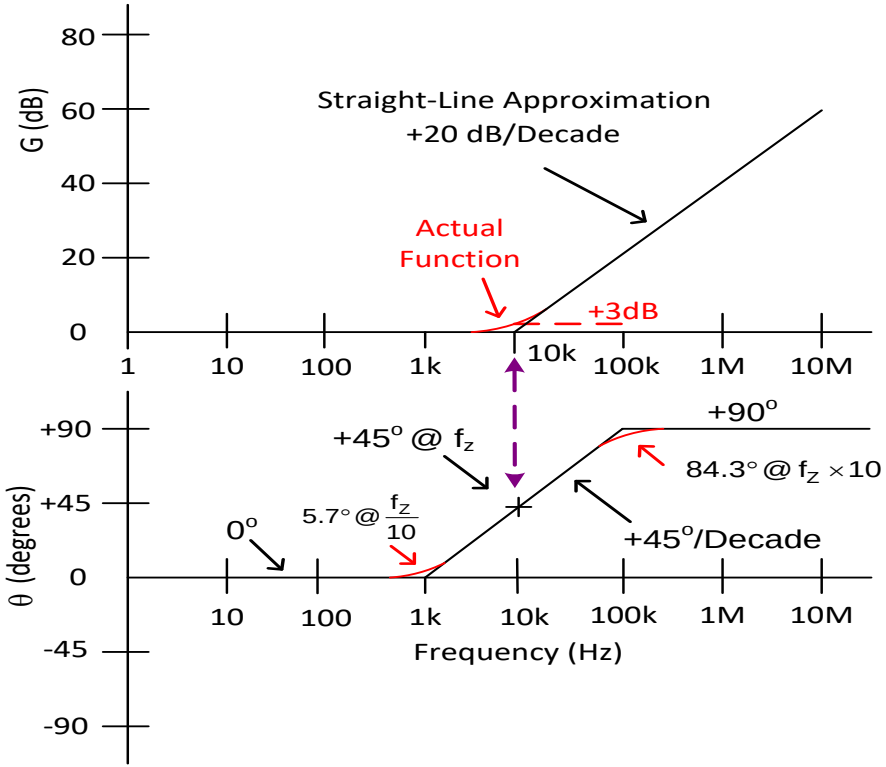
$$G_{v/v} = \frac{V_{out}}{V_{in}} = \frac{G_{dc}}{\sqrt{\left(\frac{f}{f_P}\right)^2 + 1}}$$ Magnitude

$$\Theta = -\tan^{-1}\left(\frac{f}{f_P}\right)$$ Phase

$$G_{dB} = 20\mathrm{Log}(G_{v/v})$$ Magnitude in dB

- Pole Location = f_P (Cutoff Freq)
- Magnitude ($f < f_P$) = G_{dc} (e.g. 100dB)
- Magnitude ($f = f_P$) = -3dB
- Magnitude ($f > f_P$) = -20dB/Decade
- Phase ($f = f_P$) = -45°
- Phase ($0.1f_P < f < 10f_P$) = -45°/Decade
- Phase ($f > 10f_P$) = -90°
- Phase ($f < 0.1f_P$) = 0°

Bode plots – zero



$$G_{v/v} = \frac{V_{out}}{V_{in}} = G_{dc}\left[i\left(\frac{f}{f_Z}\right) + 1\right]$$ As a complex number

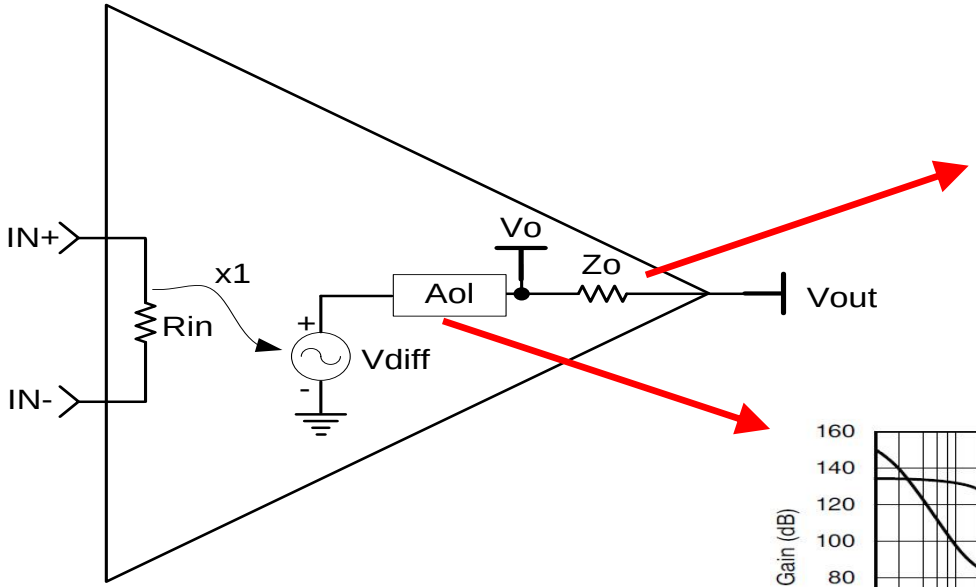
$$G_{v/v} = \frac{V_{out}}{V_{in}} = G_{dc}\sqrt{\left(\frac{f}{f_Z}\right)^2 + 1}$$ Magnitude

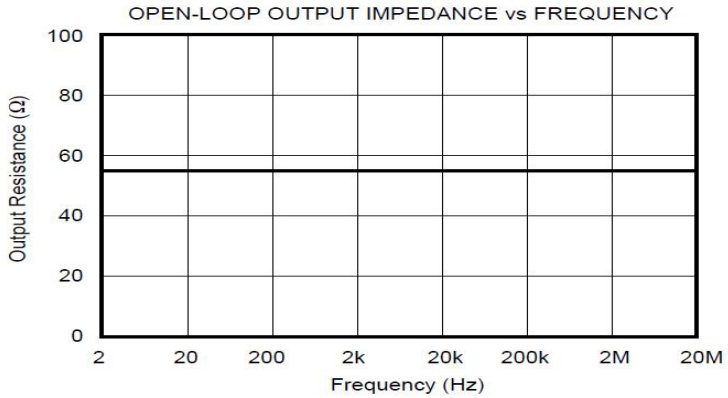
$$\Theta = \tan^{-1}\left(\frac{f}{f_Z}\right)$$ Phase

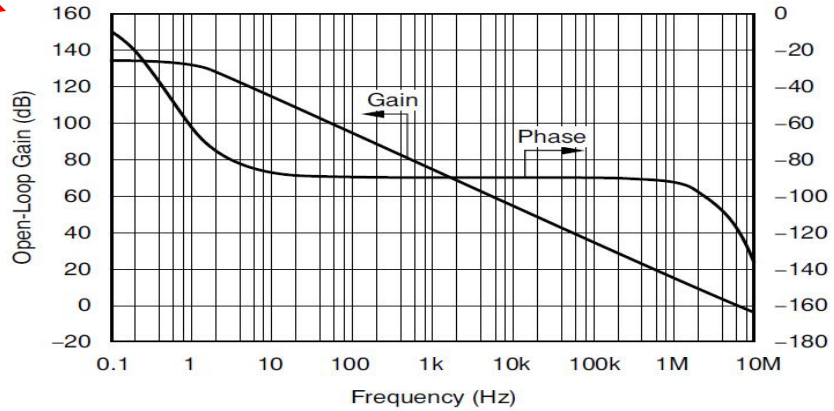
$$G_{dB} = 20\mathrm{Log}(G_{v/v})$$ Magnitude in dB

- Zero Location = f_Z
- Magnitude ($f < f_Z$) = 0dB
- Magnitude ($f = f_Z$) = +3dB
- Magnitude ($f > f_Z$) = +20dB/Decade
- Phase ($f = f_Z$) = +45°
- Phase ($0.1f_Z < f < 10f_Z$) = +45°/Decade
- Phase ($f > 10f_Z$) = +90°
- Phase ($f < 0.1f_Z$) = 0°

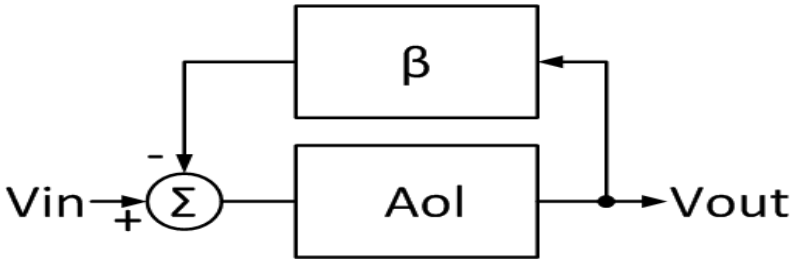
Op amp open loop model

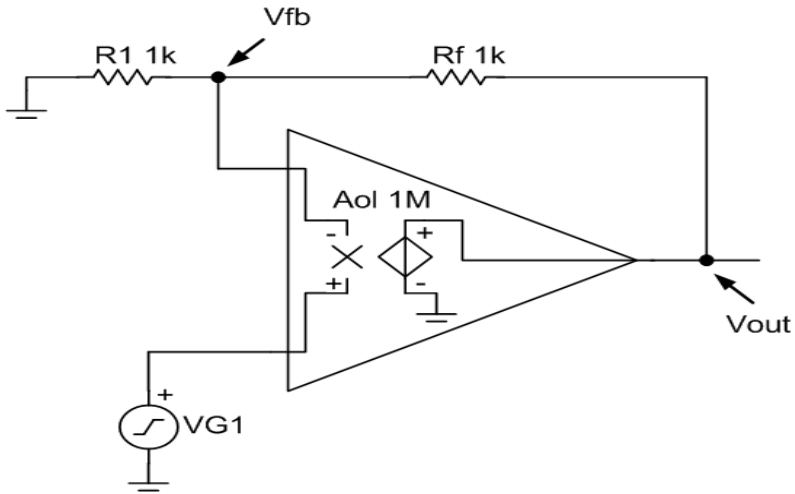






Op amp closed loop model





A_{ol} = Open loop Gain

β = Feedback Factor = $\frac{V_{fb}}{V_{out}} = \frac{R_1}{R_1 + R_f}$

A_{cl} = Closed Loop Gain = $\frac{A_{ol}}{1 + A_{ol}\beta}$

$A_{ol}\beta$ = Loop Gain

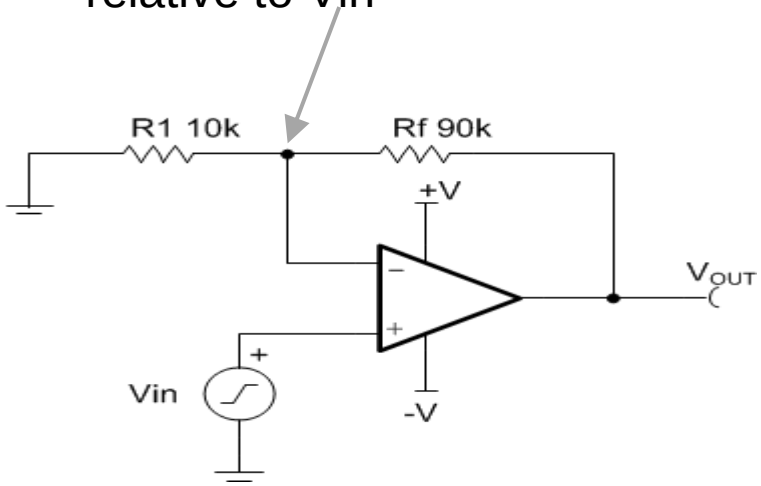
$$A_{cl} = \lim_{A_{ol}\beta \to \infty} \left(\frac{A_{ol}}{1 + A_{ol}\beta}\right) = \frac{1}{\beta} = 1 + \frac{R_f}{R_1}$$

When is an amplifier unstable?

$$\mathbf{A_{CL}} = \frac{\mathbf{A_{OL}}}{\mathbf{1} + \mathbf{A_{OL}\beta}}$$

- A circuit is unstable when $A_{OL}\beta = -1$
- $A_{OL}\beta = -1$ sets the denominator of $A_{CL} = 0$
- $A_{OL}\beta = -1$ when $A_{OL}\beta(dB) = 0dB$ and phase shift($A_{OL}\beta$) = 180°
  - Phase shift is relative to the DC phase

$A_{OL}\beta = -1$ when the phase at V_{FB} has shifted 180º relative to Vin

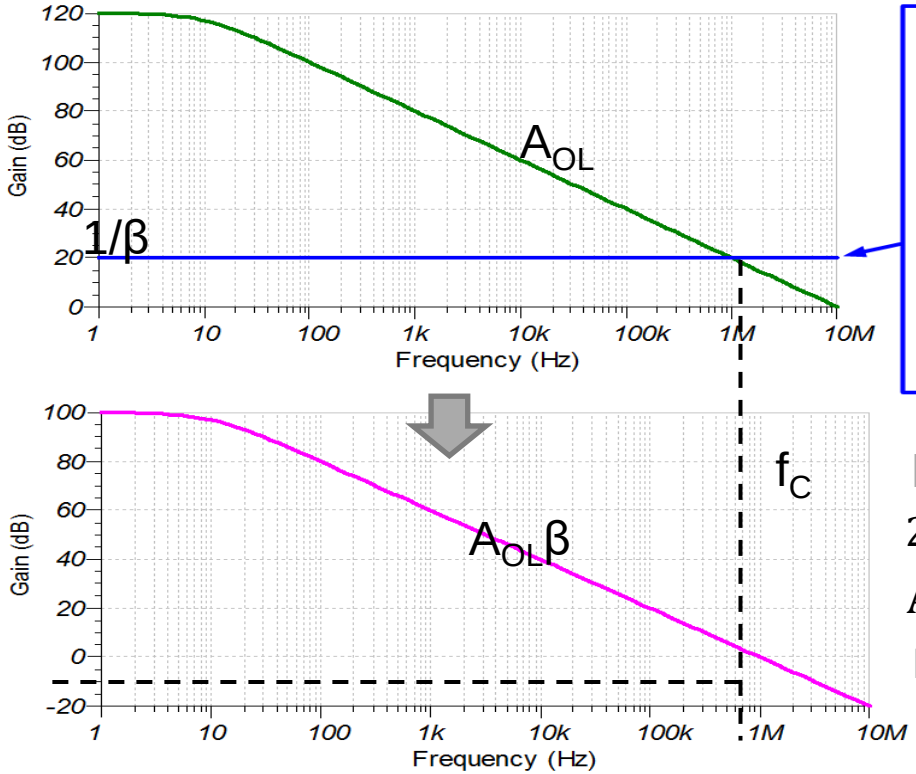


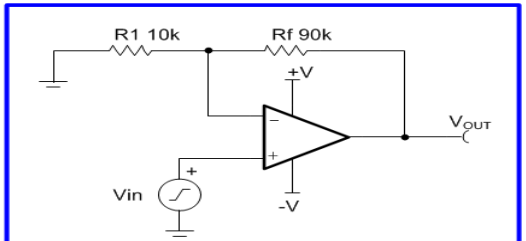
Phase margin (PM)

How close the system is to a 180° phase shift in $A_{OL}\beta$

- PM = Phase($A_{OL}\beta$) when Gain($A_{OL}\beta$) = 0dB
- Ex: 10° phase margin = 170° phase shift in $A_{OL}\beta$

Loop gain magnitude – $A_{OL}\beta$





$$\frac{1}{\beta} = \frac{V_{OUT}}{V_{FB}} = \frac{R_F}{R_1} + 1 = 10\,V/V$$

$$\frac{1}{\beta}(dB) = 20\log(10) = 20dB$$

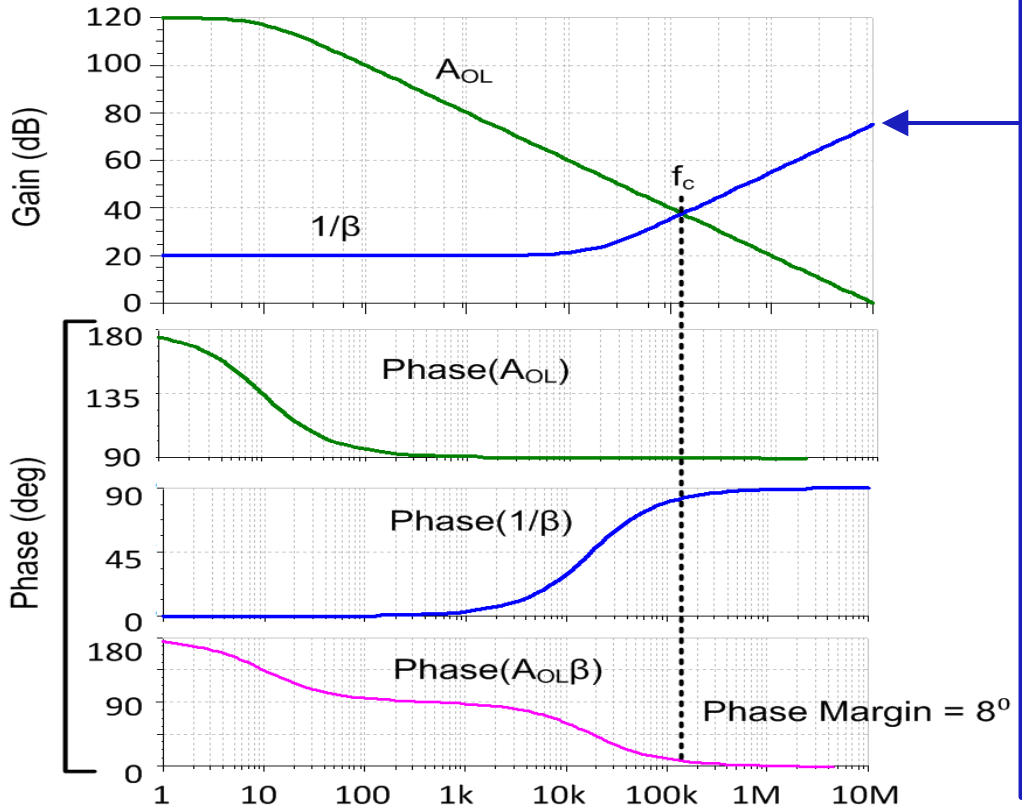
Loop gain in dB:

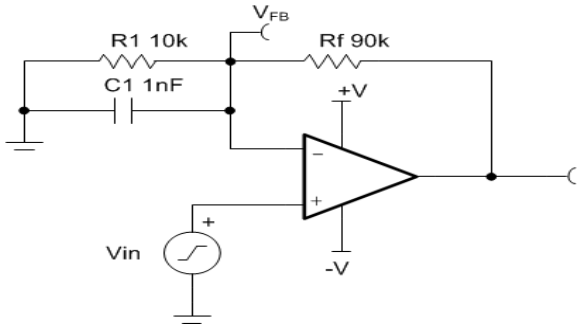
$$20\log(A_{OL}\beta) = 20\log(A_{OL}) - 20\log\left(\frac{1}{\beta}\right)$$

$$A_{OL}\beta(dB) = A_{OL}(dB) - \frac{1}{\beta}(dB)$$

Note: $A_{OL}\beta(dB) = 0dB$ when A_{OL} and $\frac{1}{\beta}$ intersect

Loop gain phase – phase($A_{OL}\beta$)



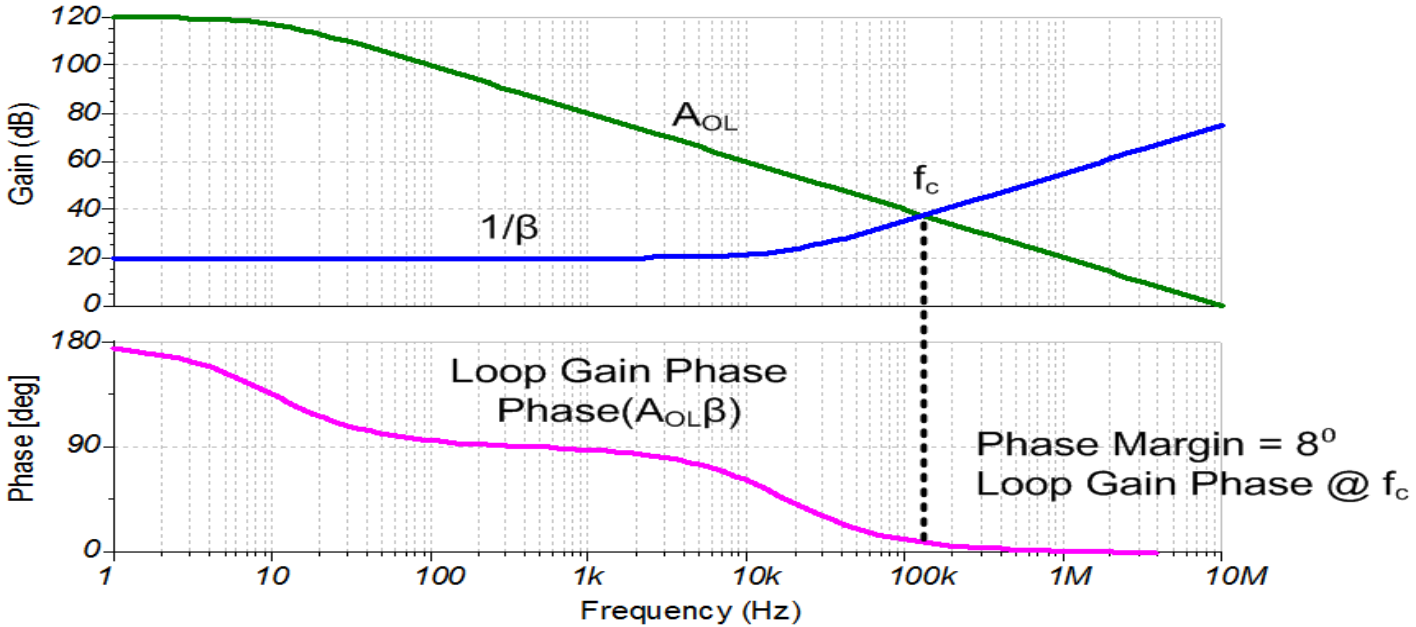


C1 introduces a zero in $\frac{1}{\beta}$

$$\frac{1}{\beta} = \frac{Z_f}{Z_1} + 1$$

At DC the capacitor is open, so gain = 10V/V. At high frequency the capacitor causes Z_1 to decrease, so gain increases by +20dB/decade

Phase margin



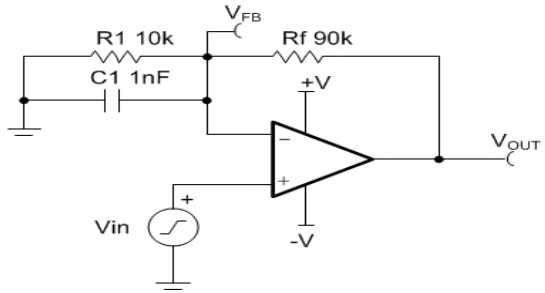
Rule of thumb:

Phase margin > 45° is required for optimal stability!

Phase margin < 45° is considered “marginally stable.”

This does not ensure a robust design over process variation.

Rate of closure – unstable example

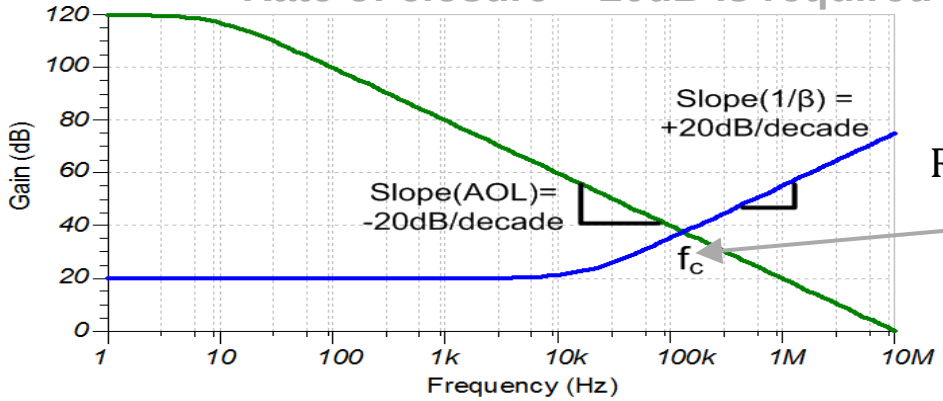


$$\frac{1}{\beta} = \frac{V_{OUT}}{V_{FB}} = 10\left(\frac{f}{f_C} + 1\right)$$

1/β(dB) = 20dB at DC, then increases by +20dB/decade after the zero frequency

Rule of thumb:

Rate of closure = 20dB is required for optimal stability!

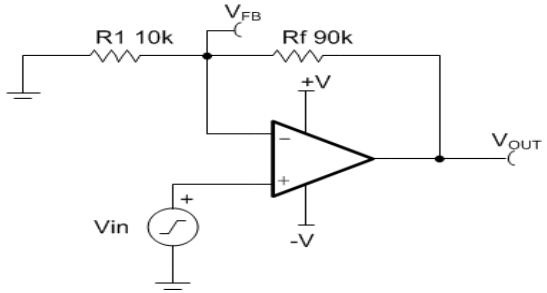


$$\text{Rate of Closure} = \left|\text{Slope}(A_{OL}) - \text{Slope}\left(\frac{1}{\beta}\right)\right|$$

$$\text{Rate of Closure} = |-20\text{dB} - (+20\text{dB})| = 40\text{dB}$$

Unstable because rate of closure > 20dB!

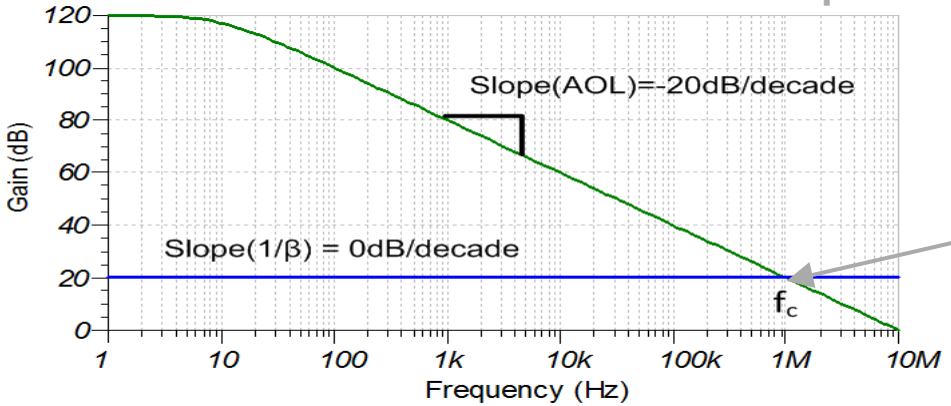
Rate of closure – stable example



$$\frac{1}{\beta} = \frac{V_{OUT}}{V_{FB}} = \frac{R_F}{R_1} + 1 = 10\,V/V$$

$$\frac{1}{\beta}(dB) = 20\log(10) = 20dB$$

Rule of thumb:
Rate of closure = 20dB is required for optimal stability!

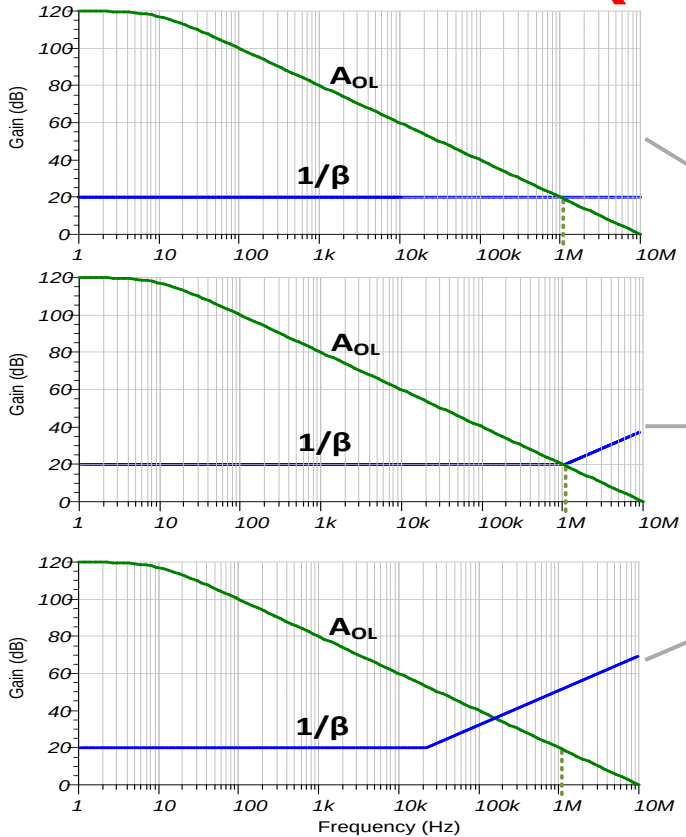


$$\text{Rate of Closure} = \left|\text{Slope}(A_{OL}) - \text{Slope}\left(\frac{1}{\beta}\right)\right|$$

$$\text{Rate of Closure} = |-20dB - 0dB| = 20dB$$

Stable because rate of closure = 20dB!

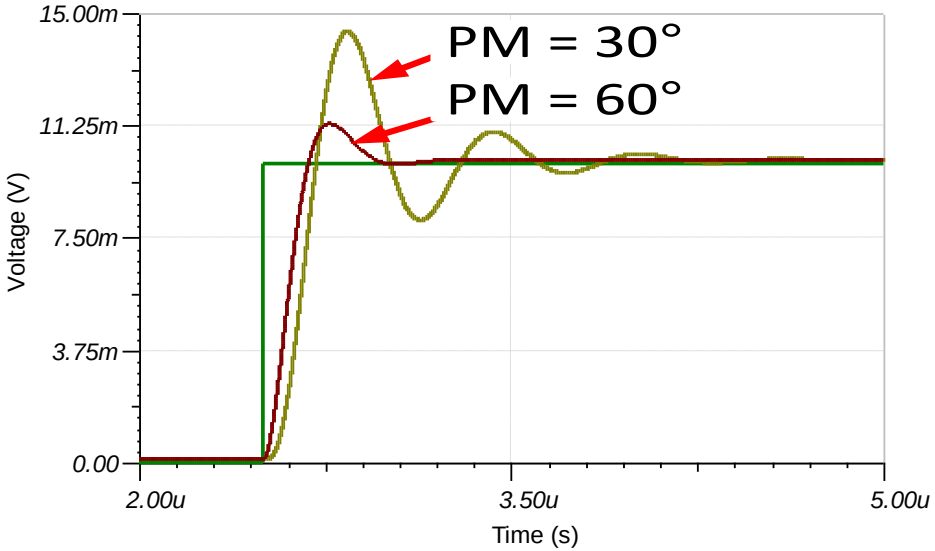
Rate of closure (ROC) and phase margin

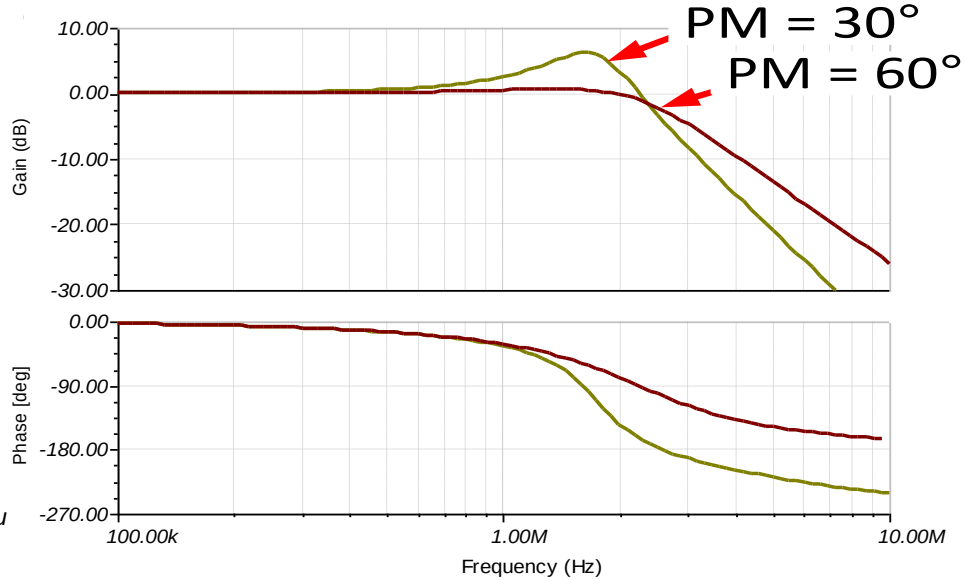


ROC (dB/decade)	Phase margin (°)
20	45 < PM < 90
20 < ROC < 40	45
40	0 < PM < 45

Indirect phase margin measurements

Phase margin can be measured indirectly on closed-loop circuits!

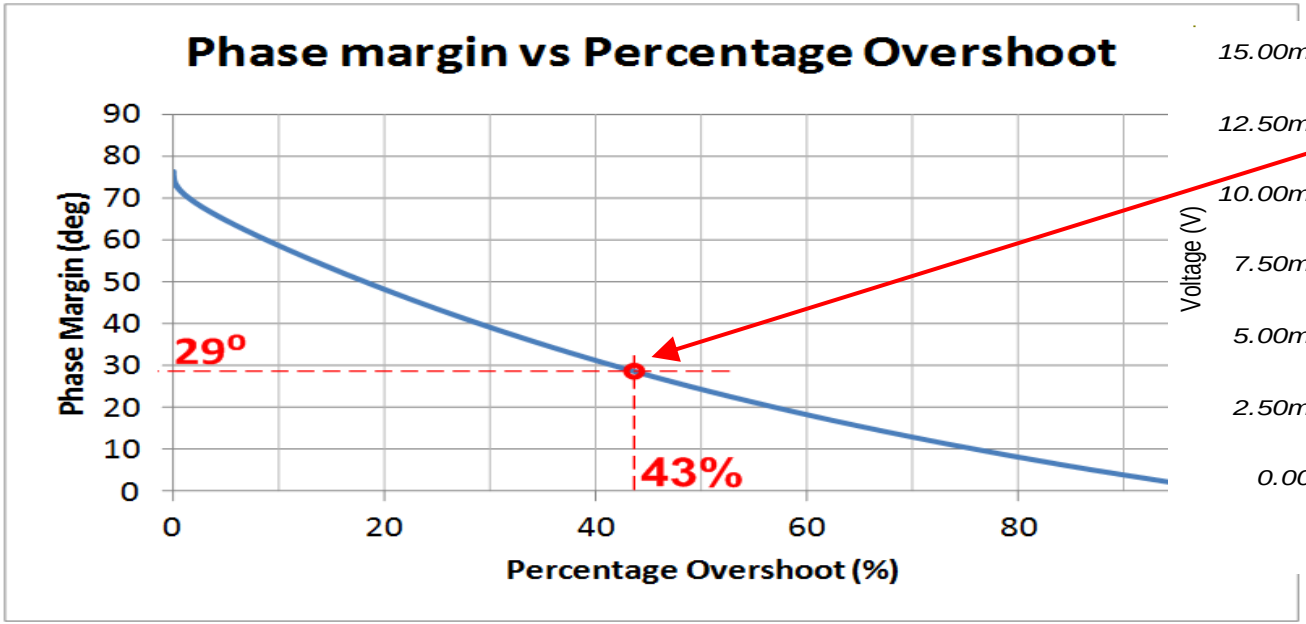


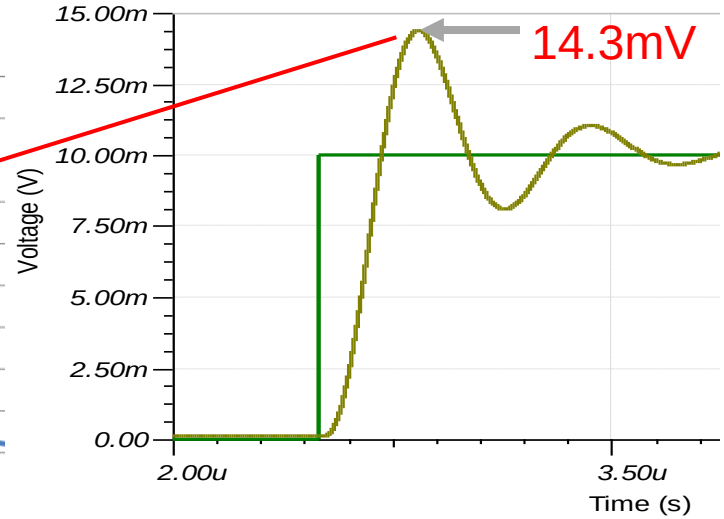


Time domain → percent overshoot

AC gain/phase → AC peaking

Indirect phase margin measurements

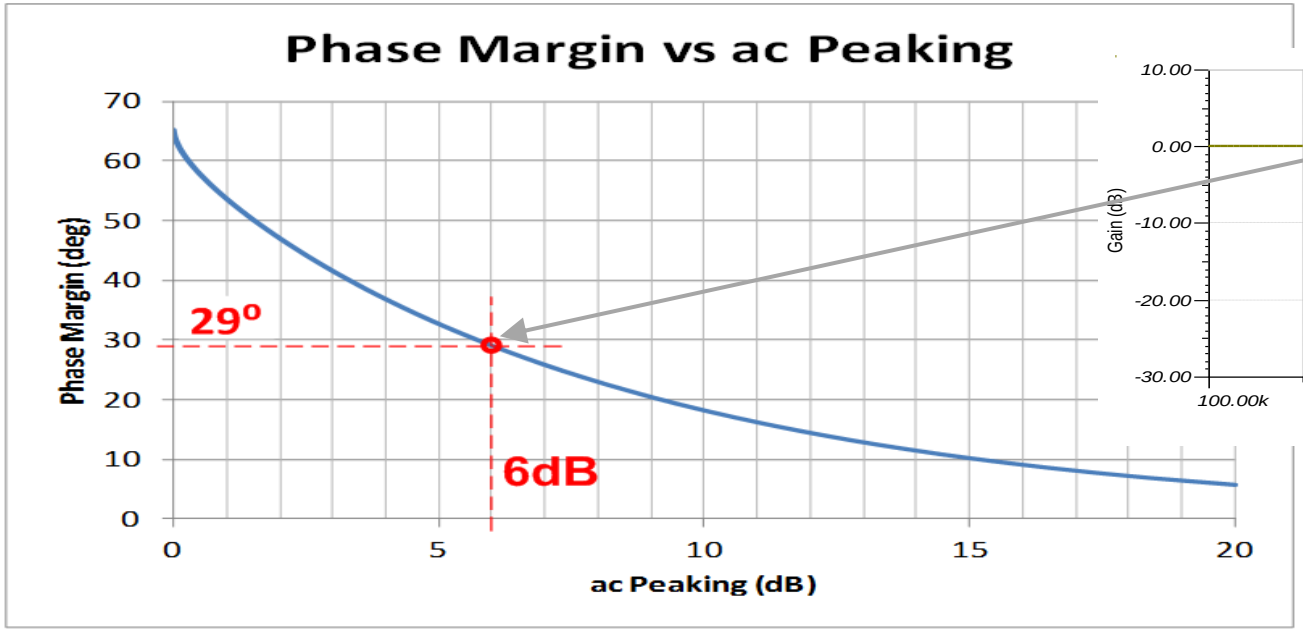


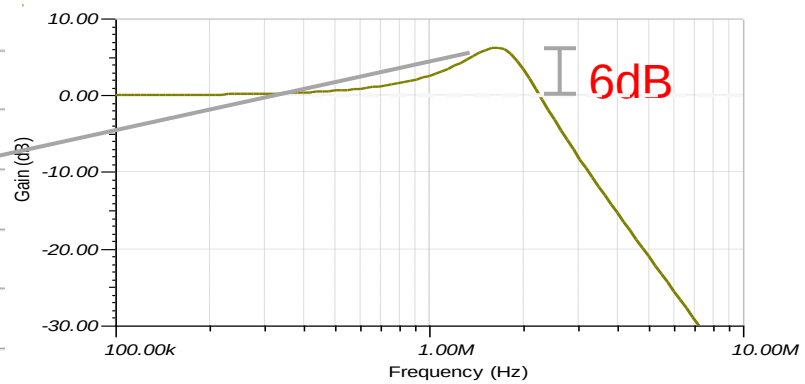


$$\%\text{Overshoot} = \left(\frac{14.3\text{mV} - 10\text{mV}}{10\text{mV}}\right) * 100\% = \mathbf{43}\%$$

43% overshoot → **29° phase margin**

Indirect phase margin measurements



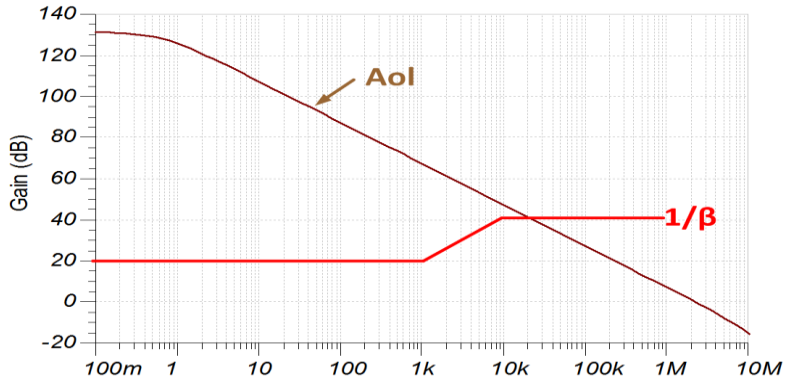


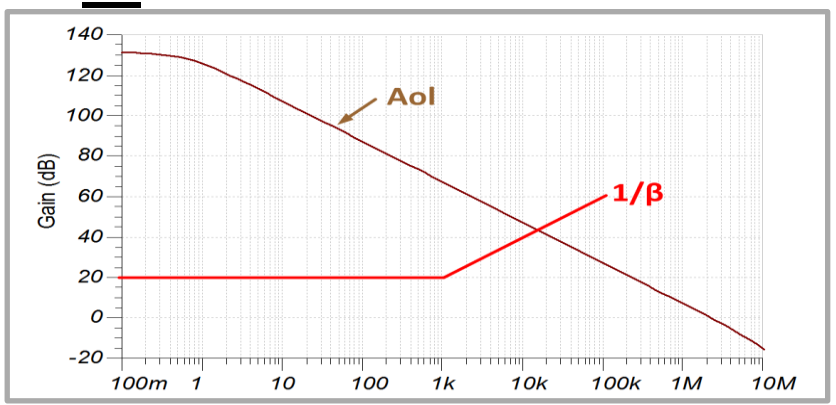
$$\text{AC peaking} = 6\text{dB} - 0\text{dB} = 6\text{dB}$$

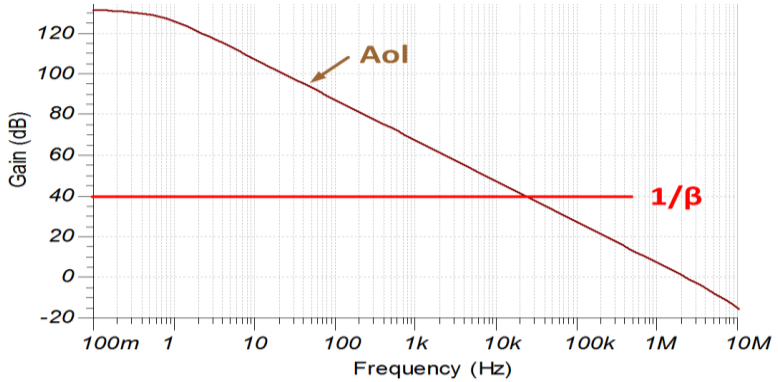
6dB AC peaking → **29° phase margin**

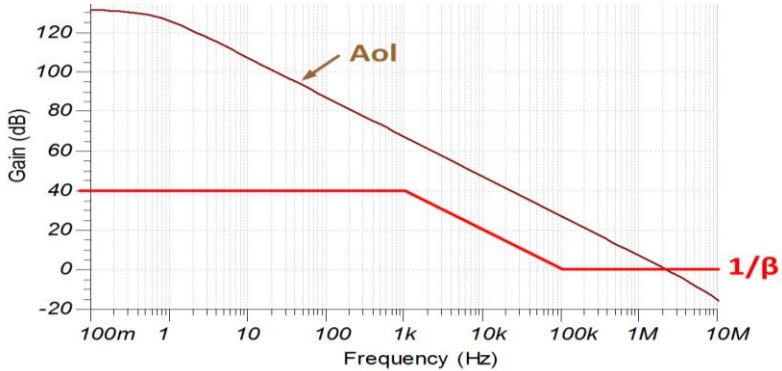
Quiz

- Which **one** of these A_{OL} and 1/β curves is **unstable**?



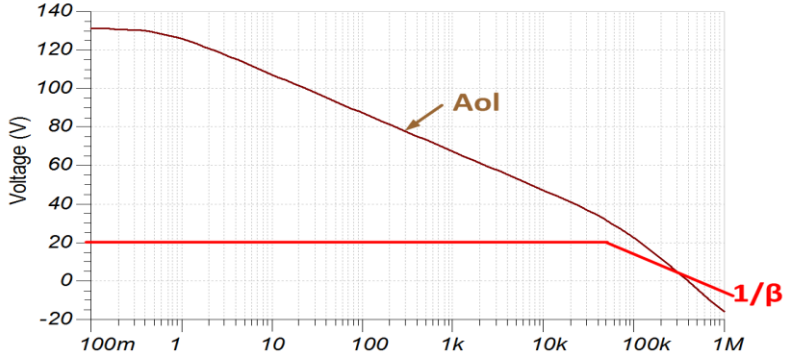


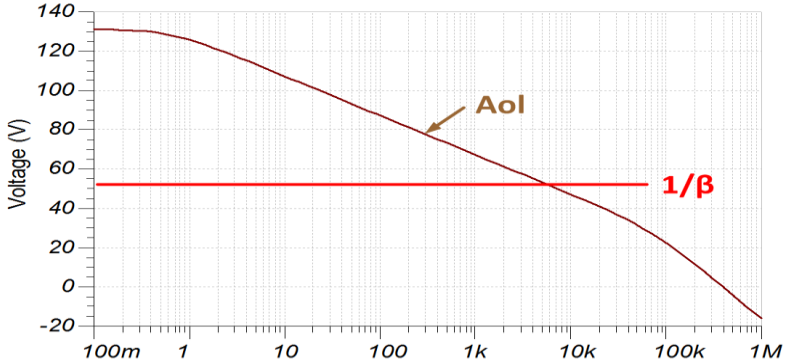


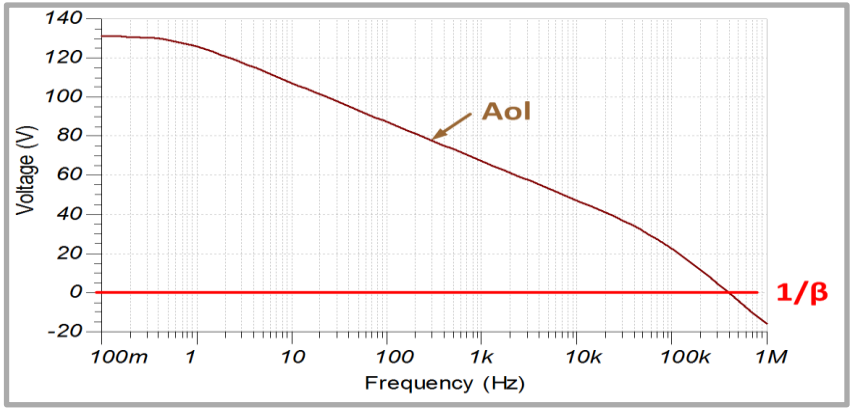


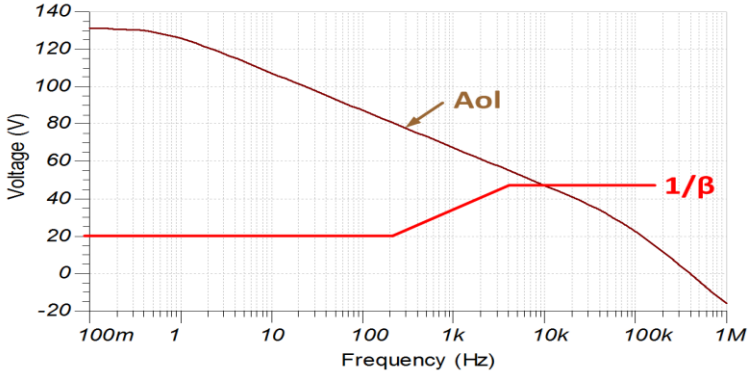
Quiz

- Which **one** of these A_{OL} and 1/β curves is **un**stable?



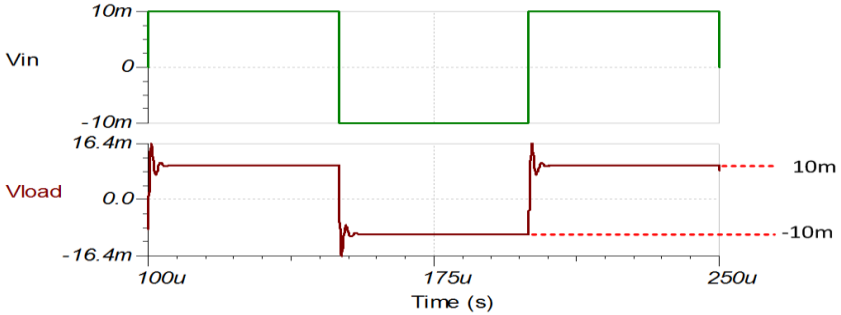




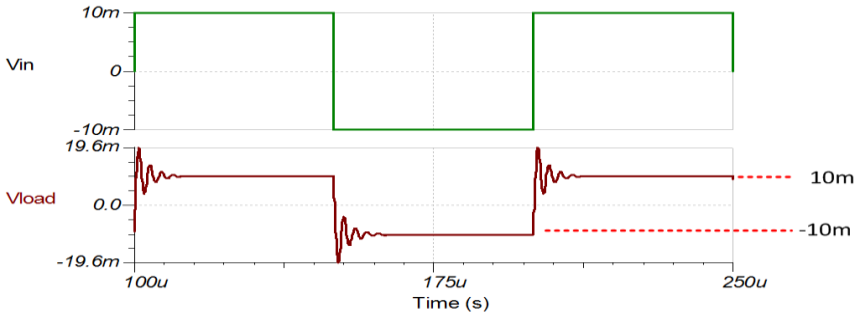


Quiz

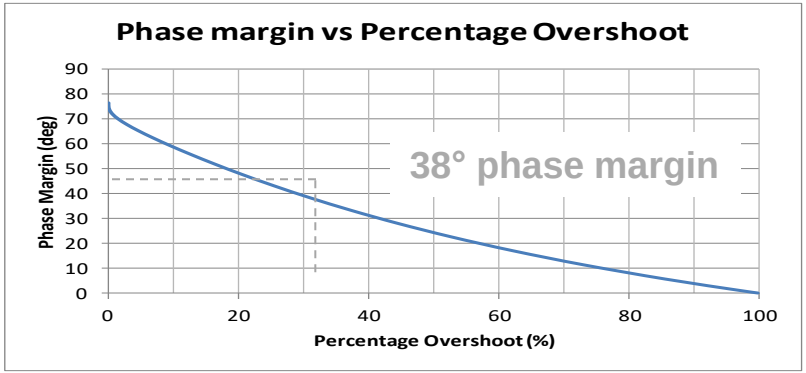
- Find the phase margin of each system according to the % overshoot.

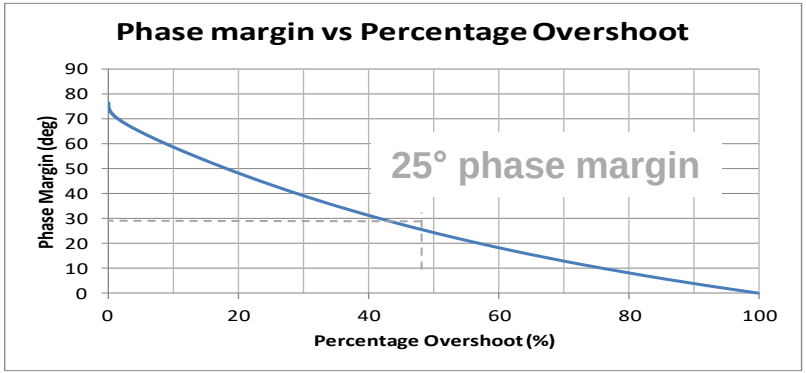


$$\%\text{Overshoot} = \left(\frac{16.4\text{mV} - 10\text{mV}}{20\text{mV}}\right) * 100\% = \mathbf{32}\%$$



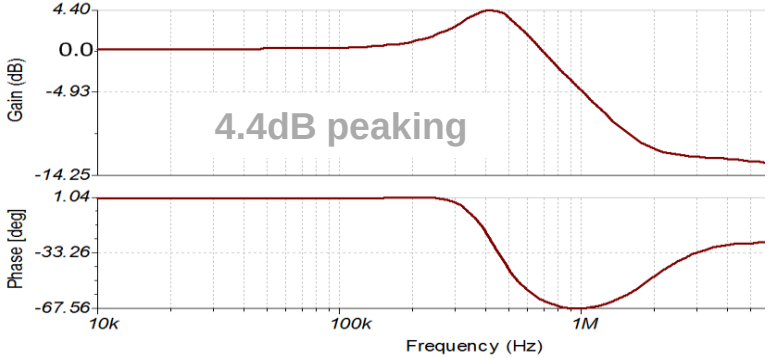
$$\%\text{Overshoot} = \left(\frac{19.6\text{mV} - 10\text{mV}}{20\text{mV}}\right) * 100\% = \mathbf{48}\%$$

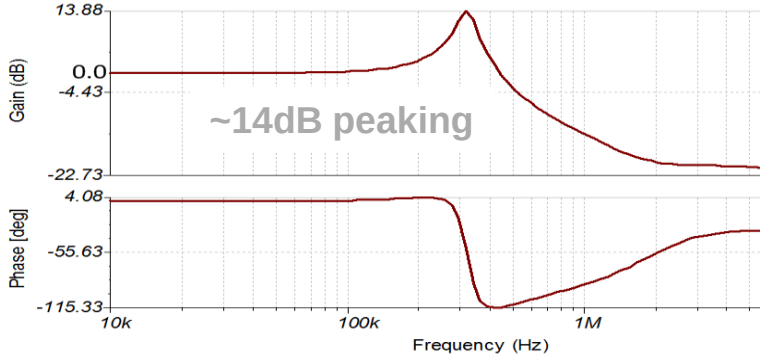


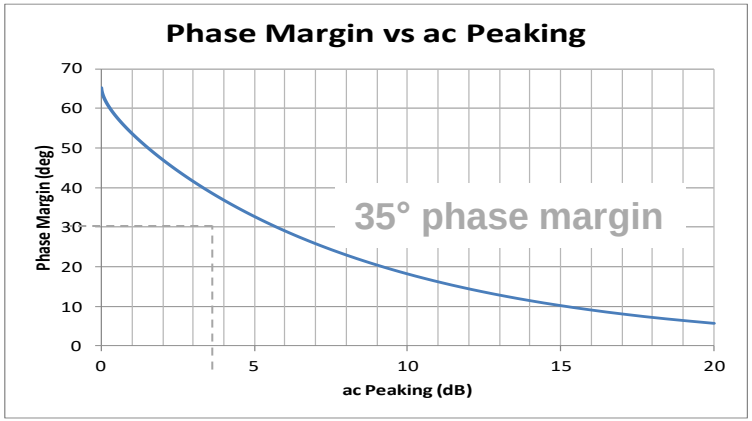


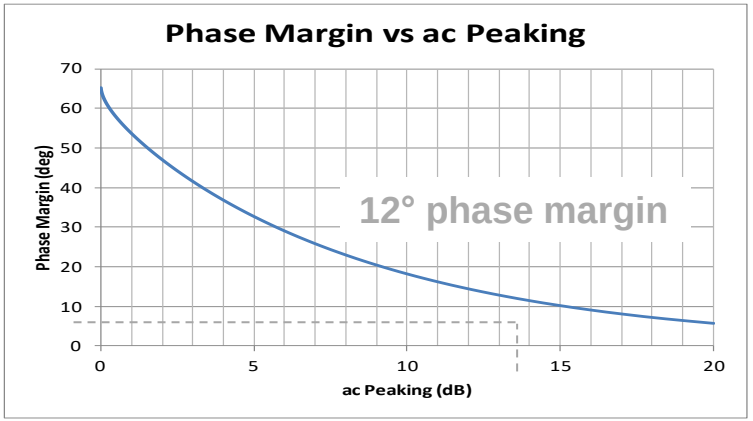
Quiz

- Find the phase margin of each system according to the AC peaking.



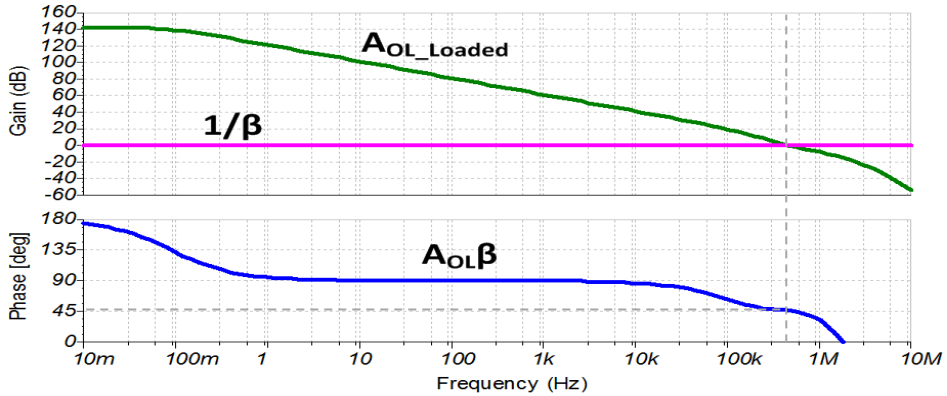




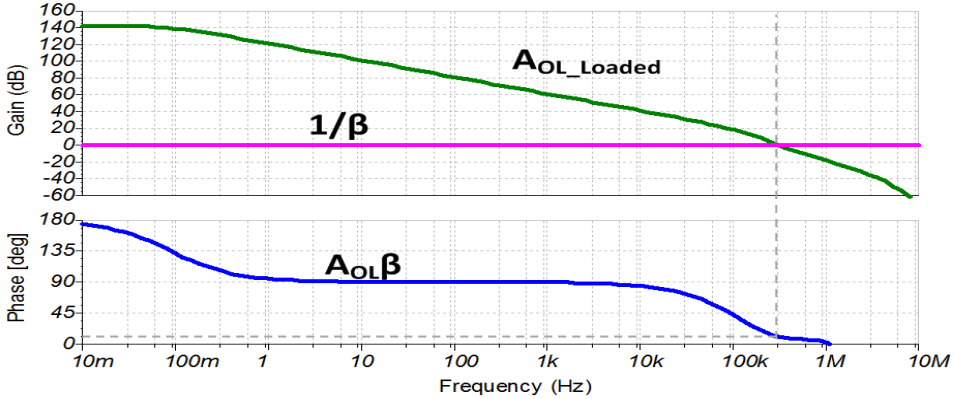


Quiz

- Find the phase margin of each system according to the Bode plot.



45° phase margin



~15° phase margin

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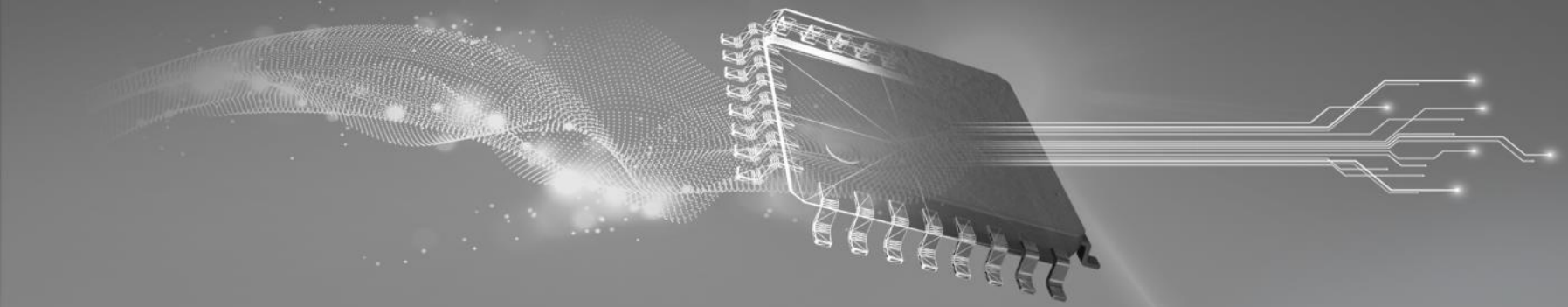


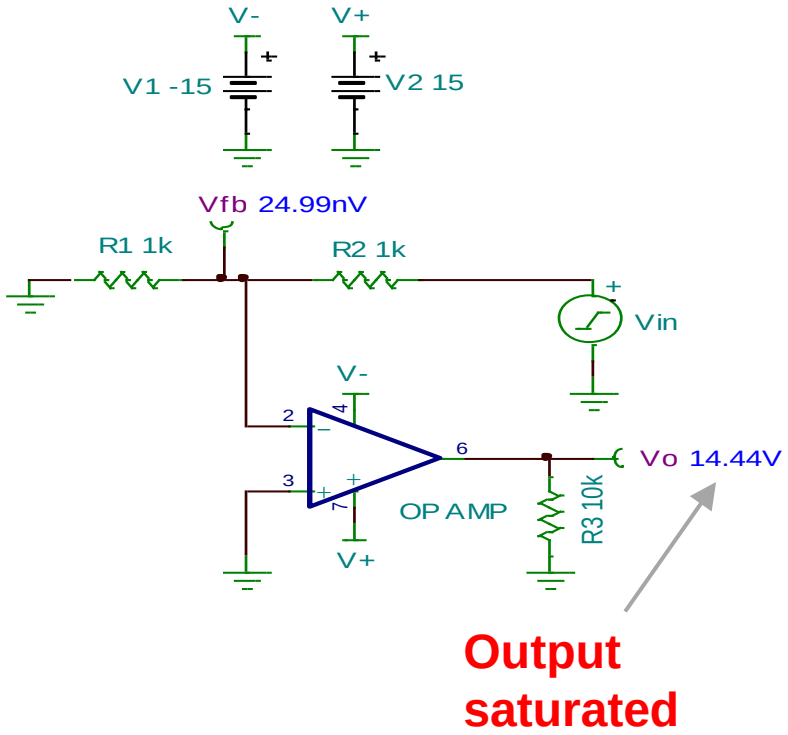
How to resolve op-amp stability issues using SPICE simulations – Part 2

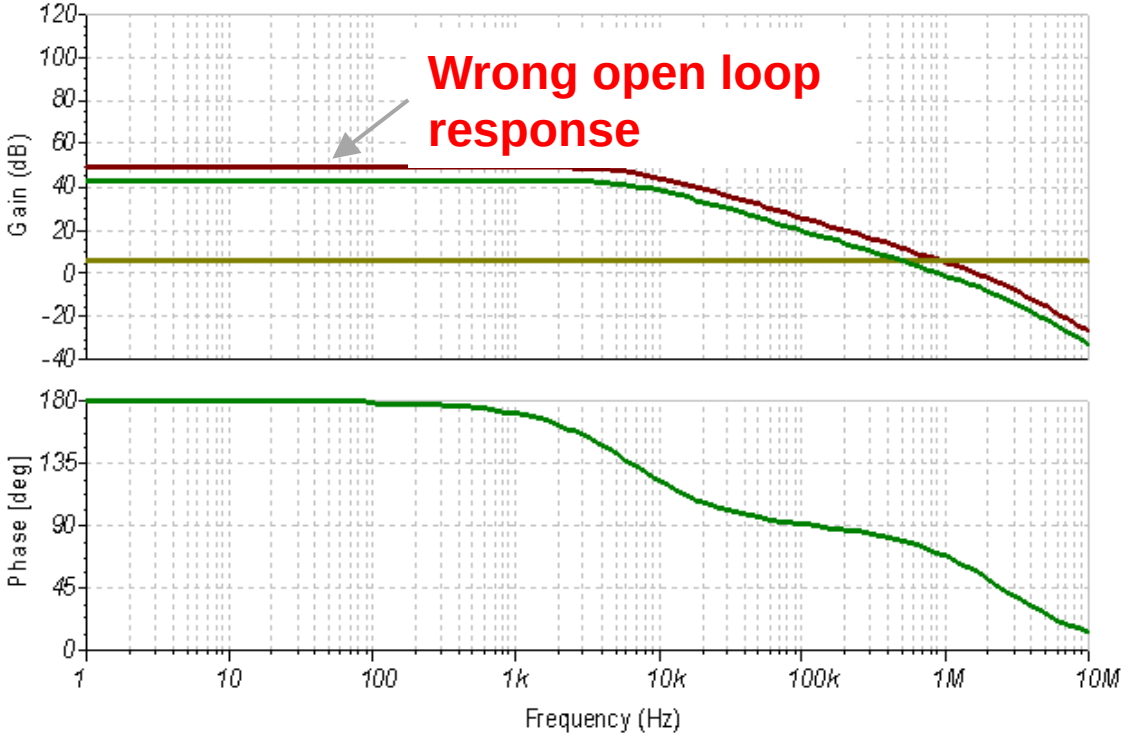
Presented by Marek Lis

High Precision Products

Simulating open-loop circuits

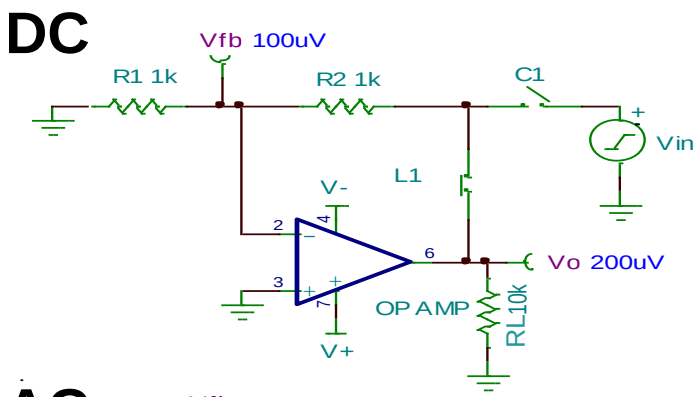
No DC biasing produces erroneous results!

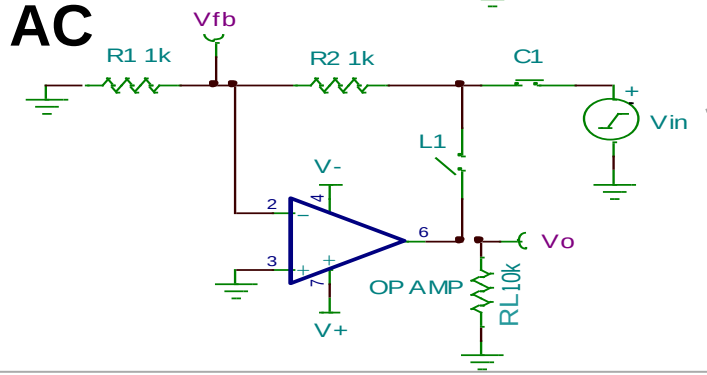


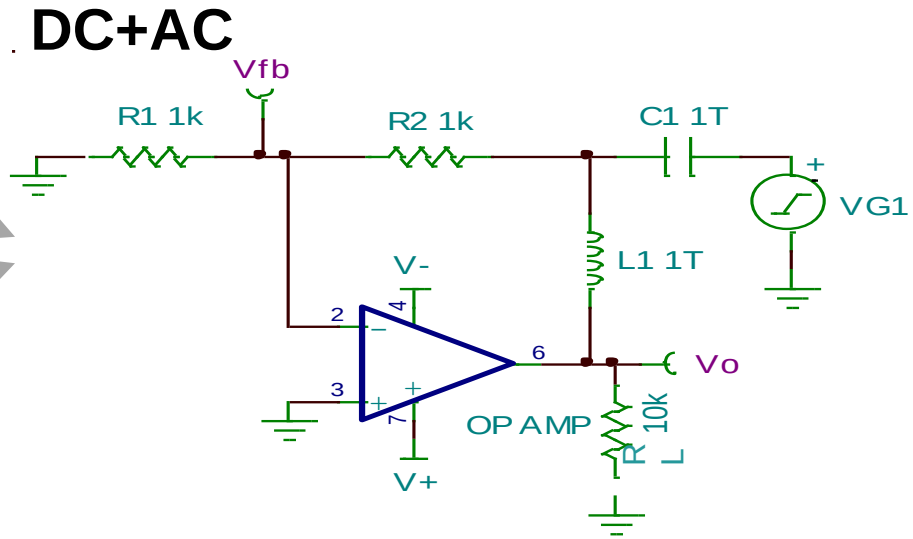


Simulating open-loop circuits

DC: closed loop needed for SPICE operation
AC: open loop needed for stability analysis

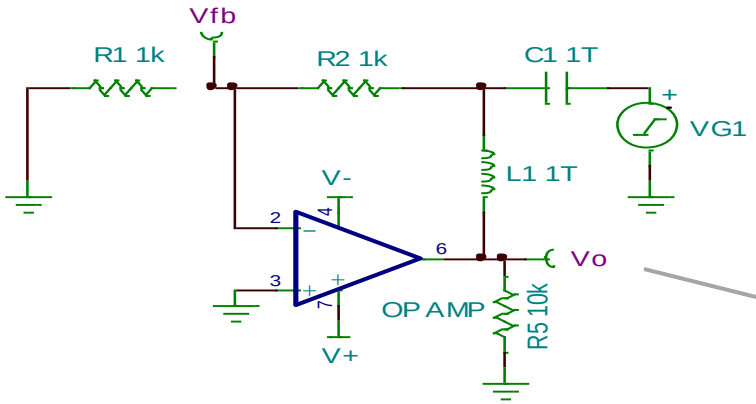


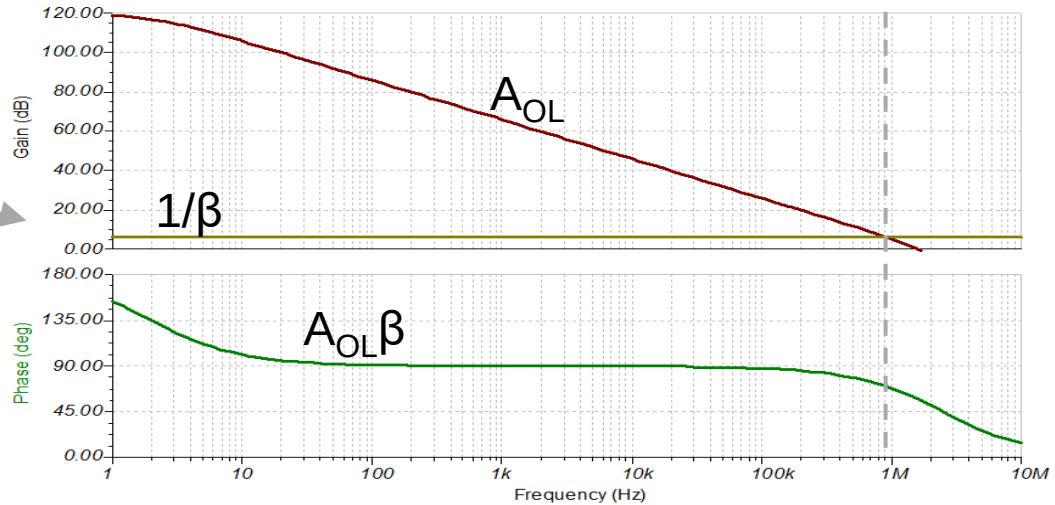




Standard open-loop SPICE configuration

We need an open-loop circuit (no feedback) to generate open-loop gain (A_{OL}), **1/β**, and loop gain ($A_{OL}\beta$) curves





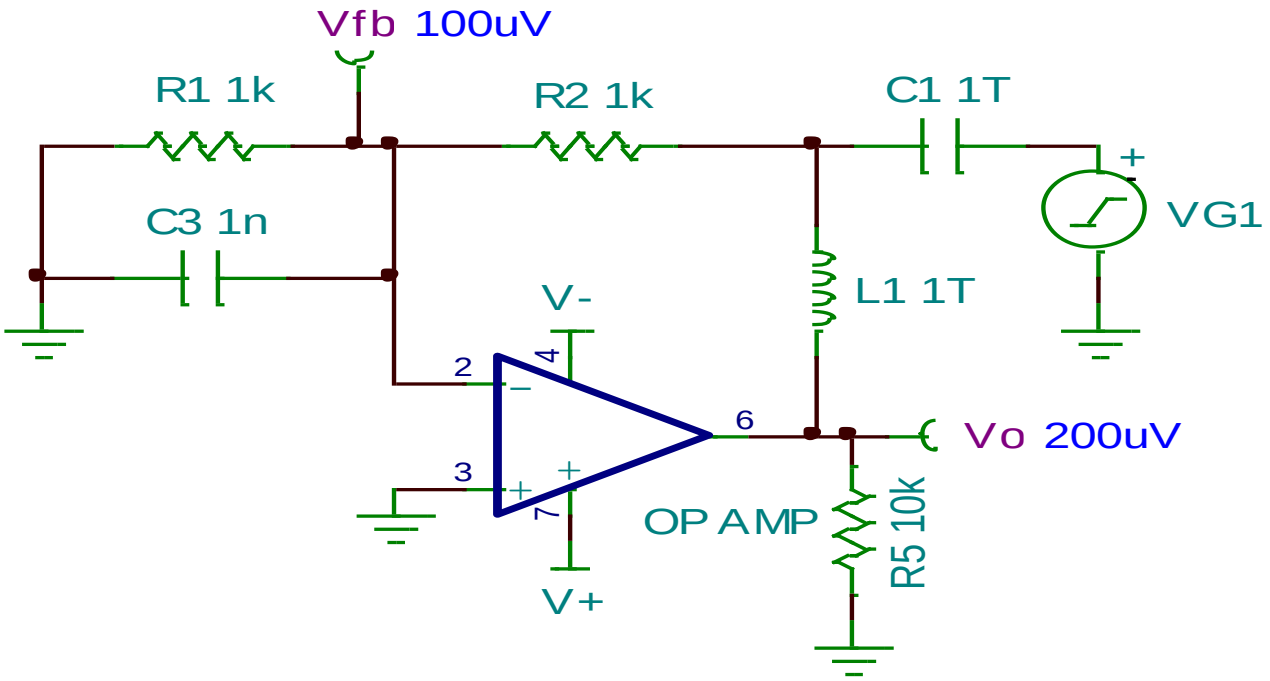
$$A_{OL\_LOADED} = Vo / Vfb$$

$$1/\beta = 1 / Vfb$$

$$A_{OL}\beta = Vo$$

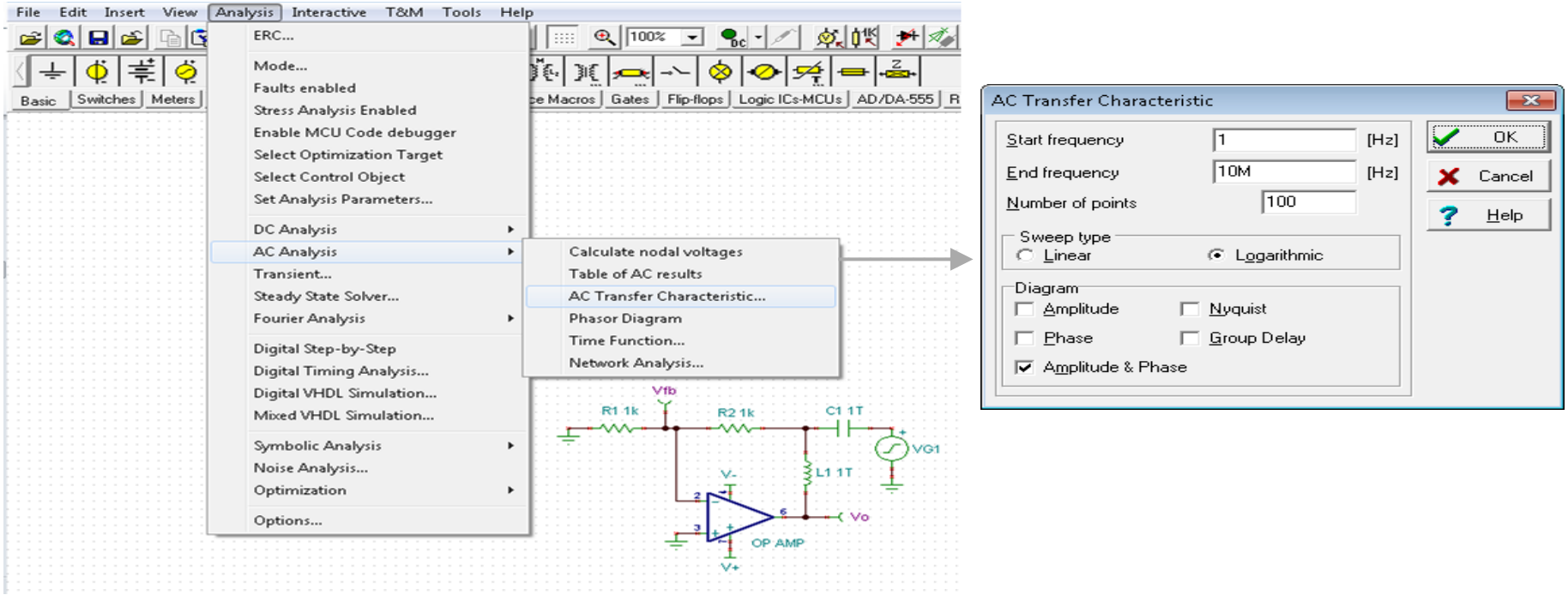
Check DC operating point

Click **Analysis → DC Analysis → Calculate Nodal Voltages**



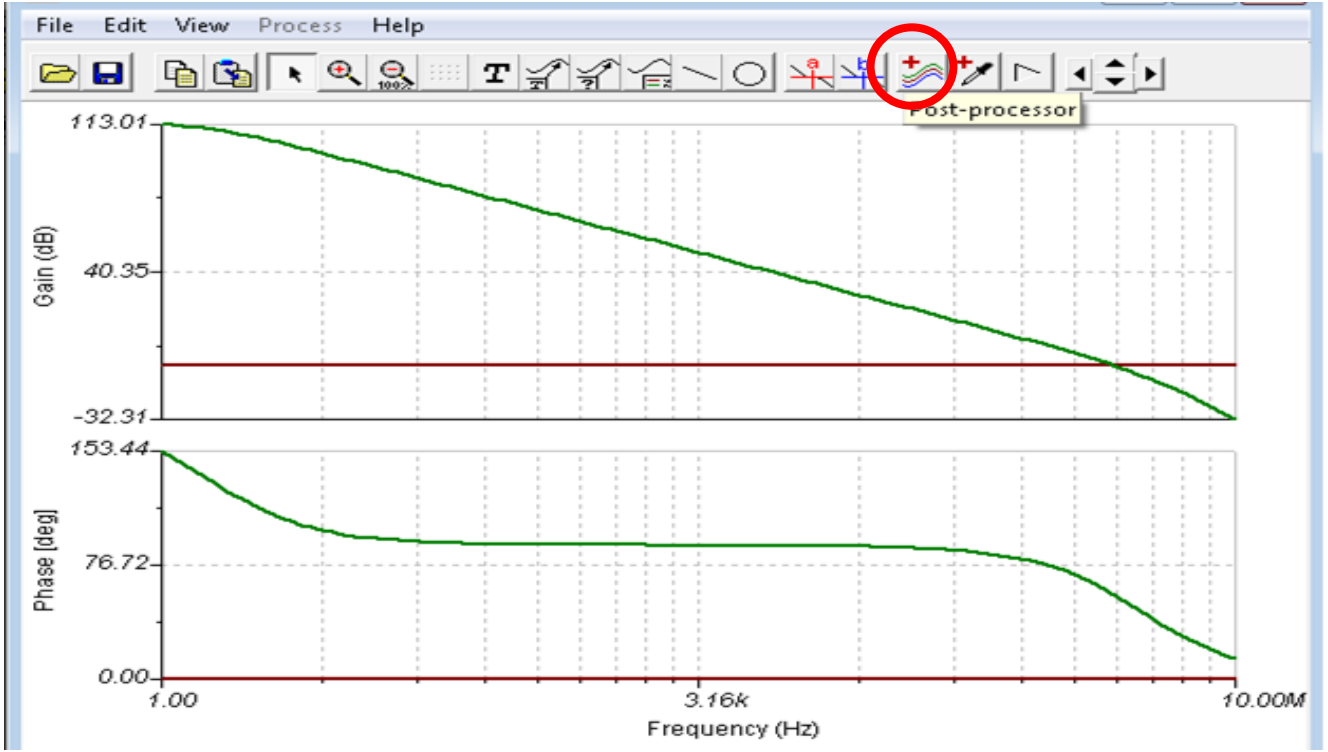
Generating open-loop curves

Run an AC transfer characteristic analysis over the appropriate frequency range:
Click **Analysis → AC Analysis → AC Transfer Characteristic**



Generating open-loop curves

Click the “Post-Processor” button to add the desired curves



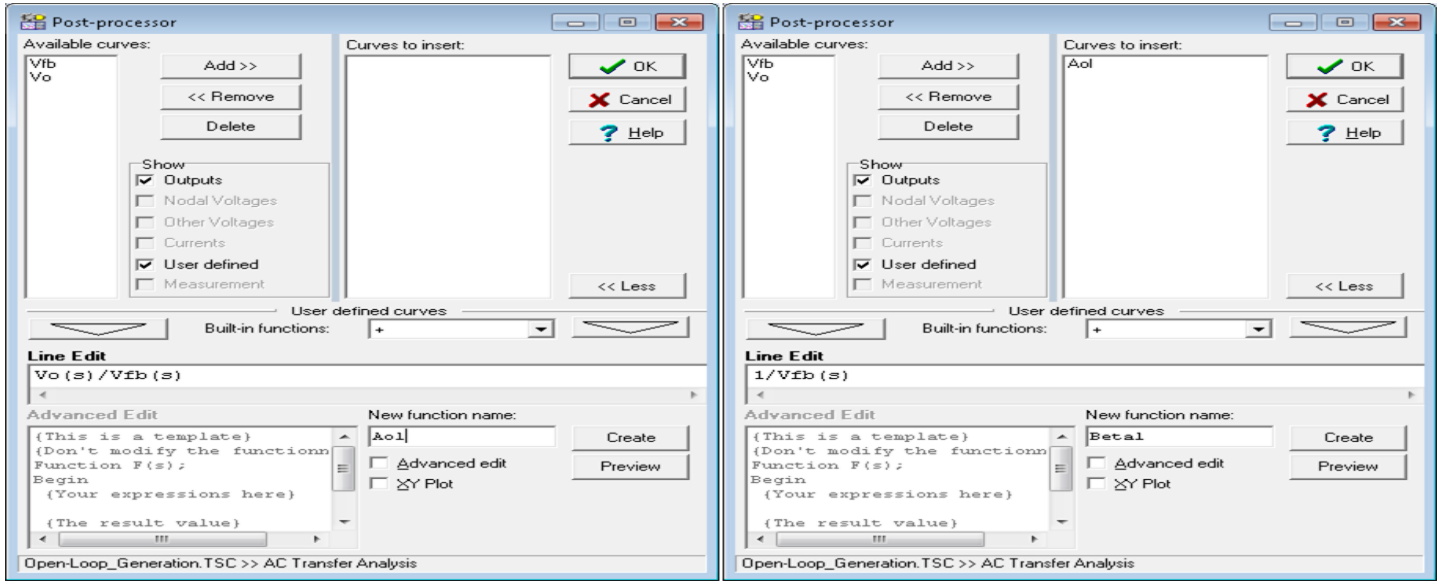
Generating open-loop curves

Perform math on the existing curves to create the new curves:

$$A_{OL} = Vo / Vfb$$

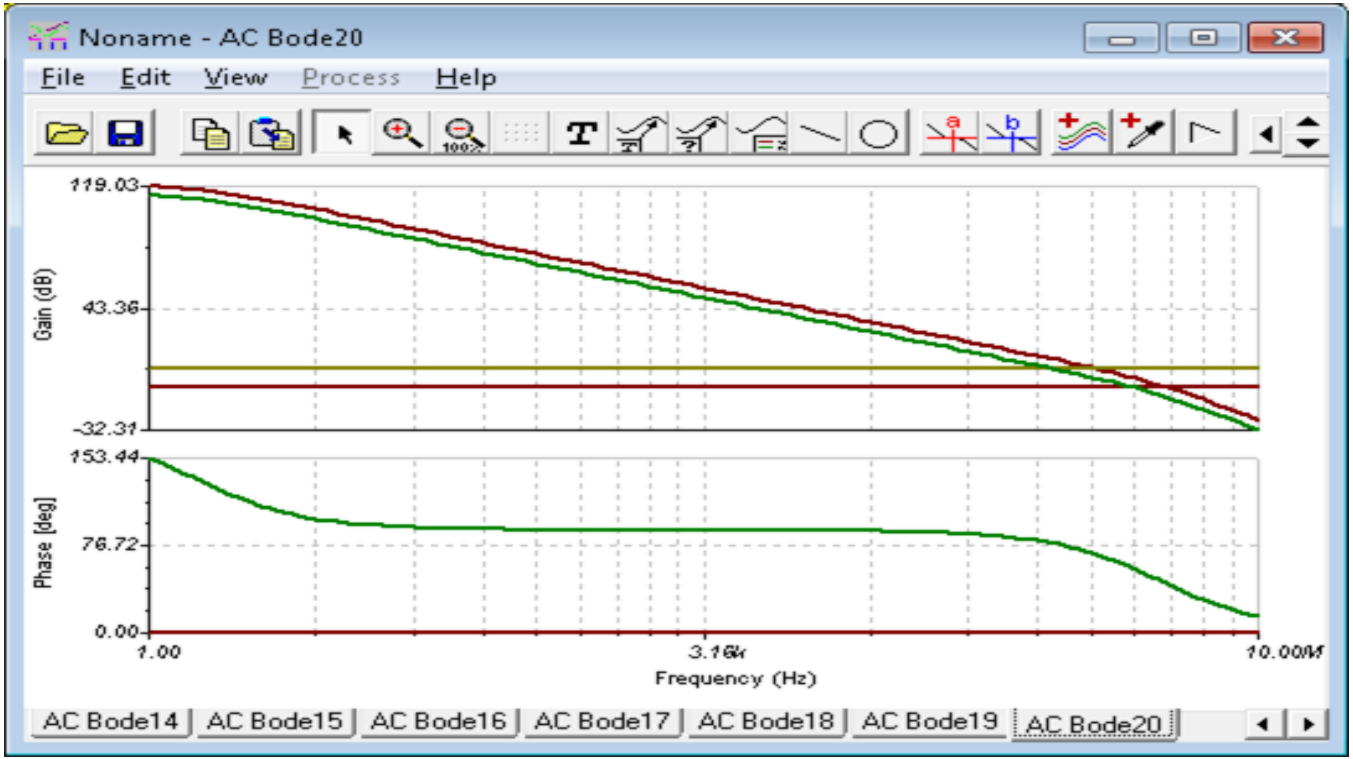
$$1/\beta = 1/Vfb$$

$$A_{OL}\beta = Vo$$



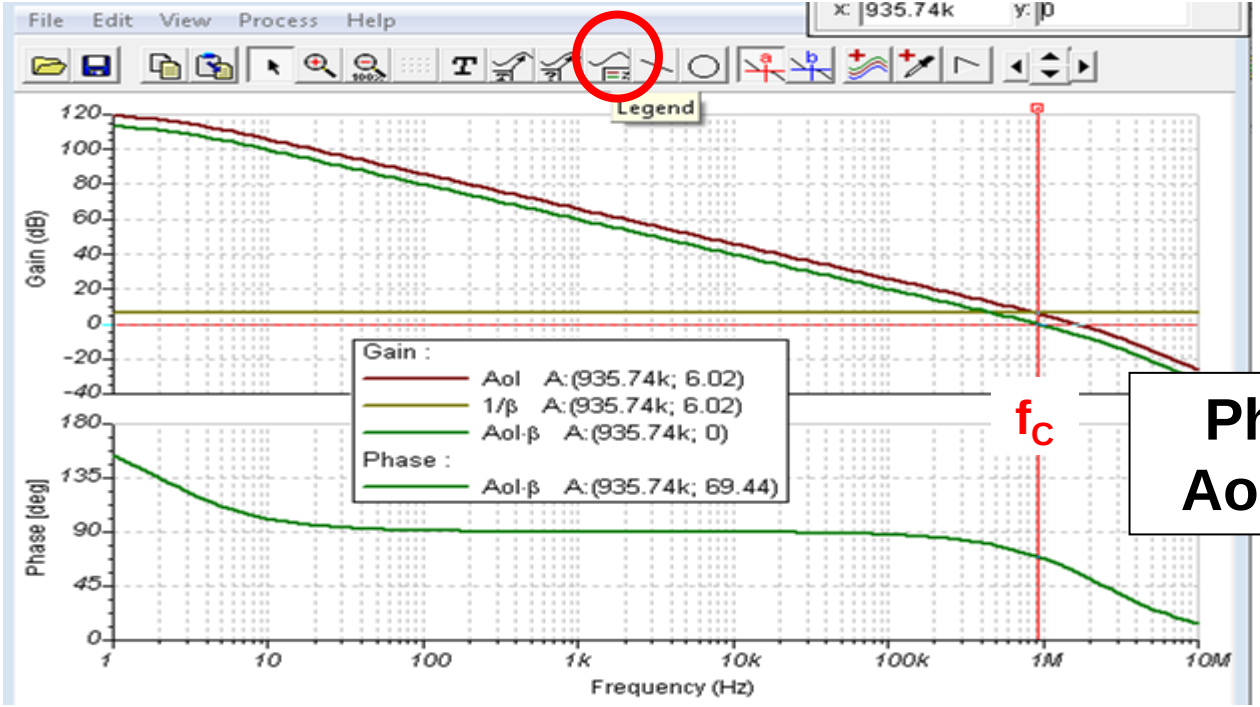
Generating open-loop curves

Unformatted results with all curves:



Generating open-loop curves

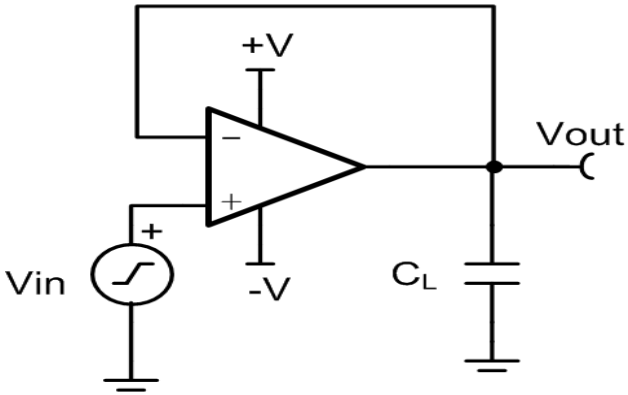
Use a cursor to determine the frequency where Aolβ = 0dB, f_C, and place legend to show corresponding magnitudes and phases

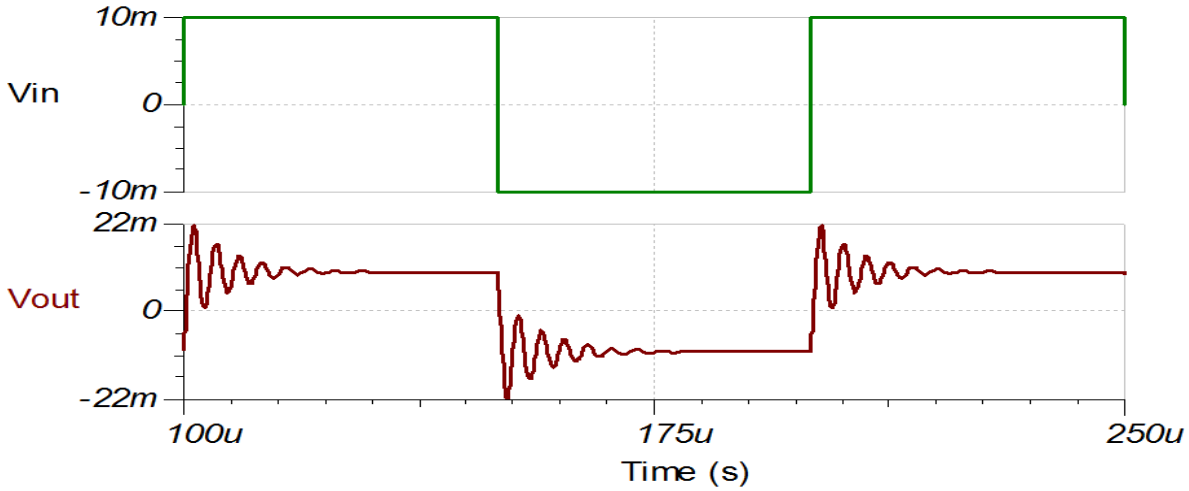


f_C

Phase Margin = Aol*β Phase @ f_C

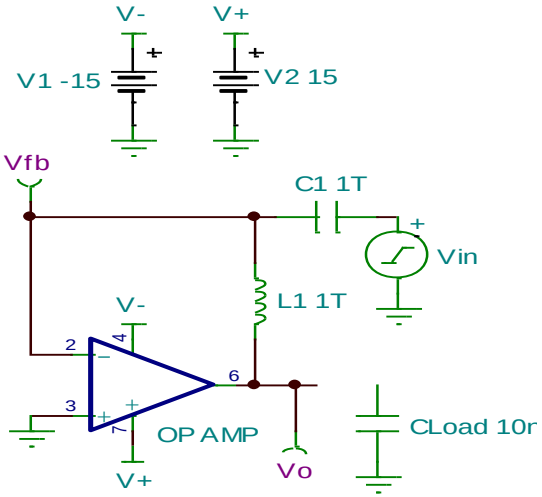
Why do capacitive loads cause instability?

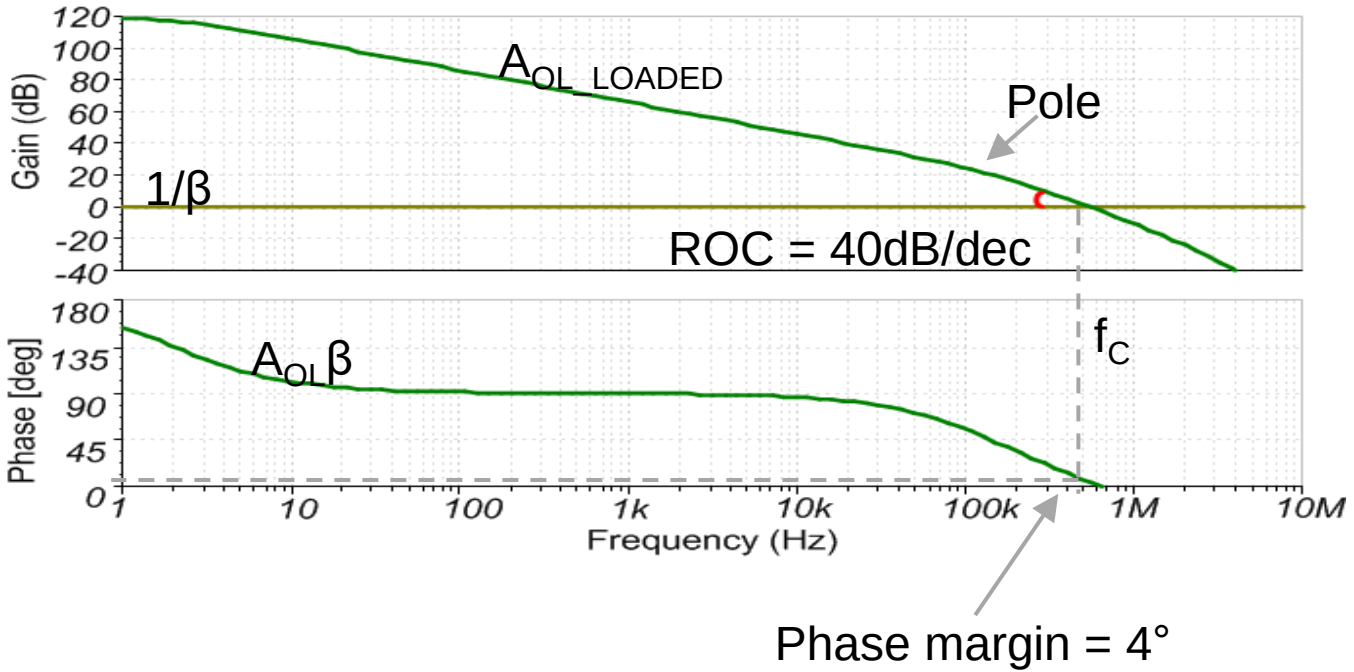




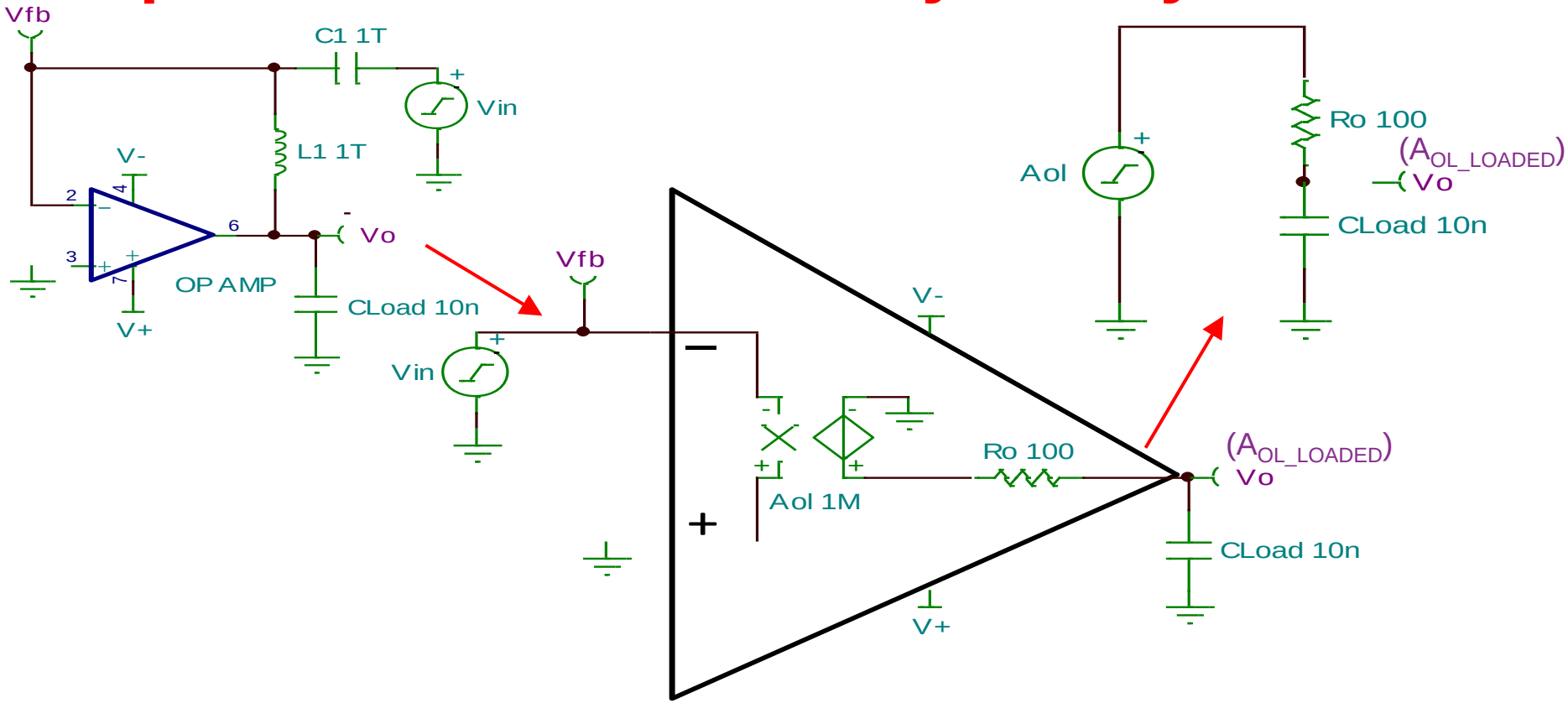
Simulate the effects of output capacitance

Run open-loop analysis on buffer circuit with capacitive load

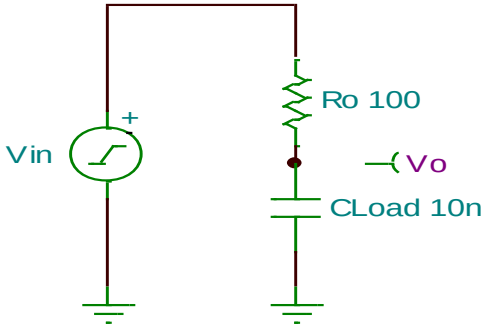


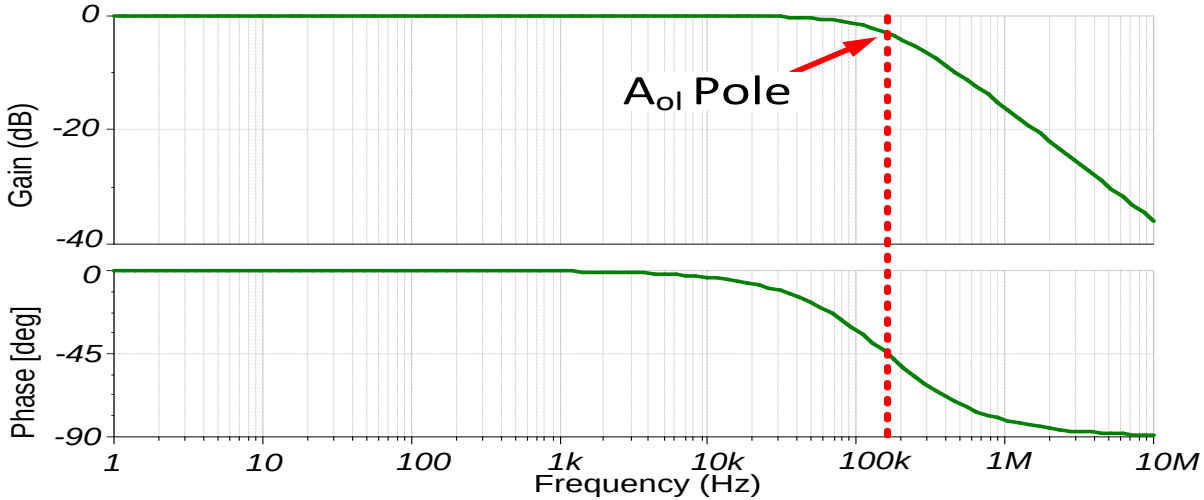


Capacitive loads – stability theory



Capacitive loads – stability theory



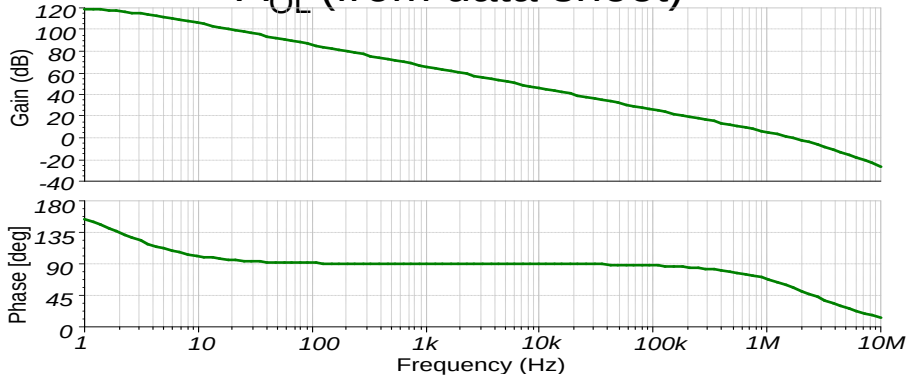


Transfer function: $$\frac{V_o}{V_{in}}(s) = \frac{1}{1 + s * Ro * C_{LOAD}}$$

Pole equation: $$f_{POLE} = \frac{1}{2 * \pi * Ro * C_{LOAD}}$$

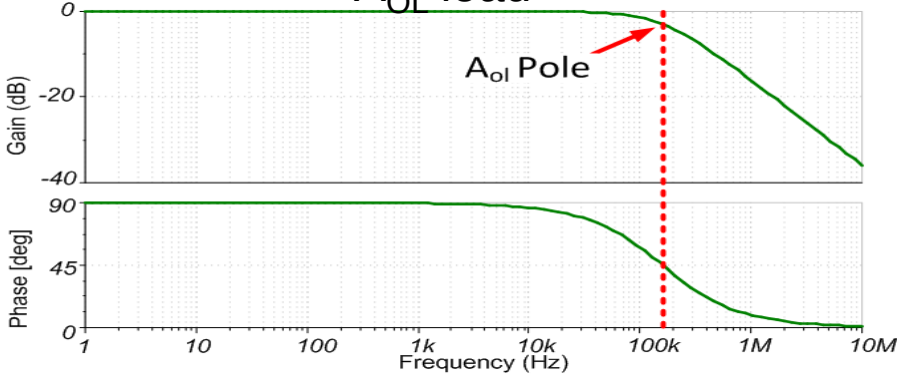
Capacitive loads – stability theory

A_{OL} (from data sheet)

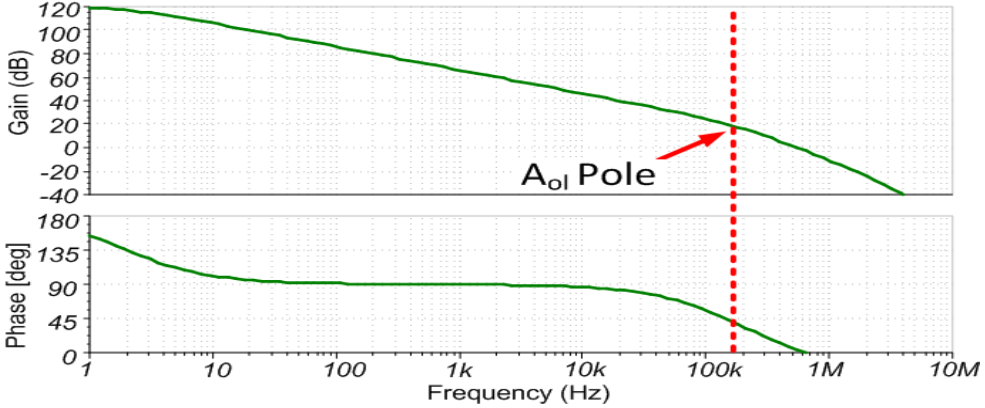


X

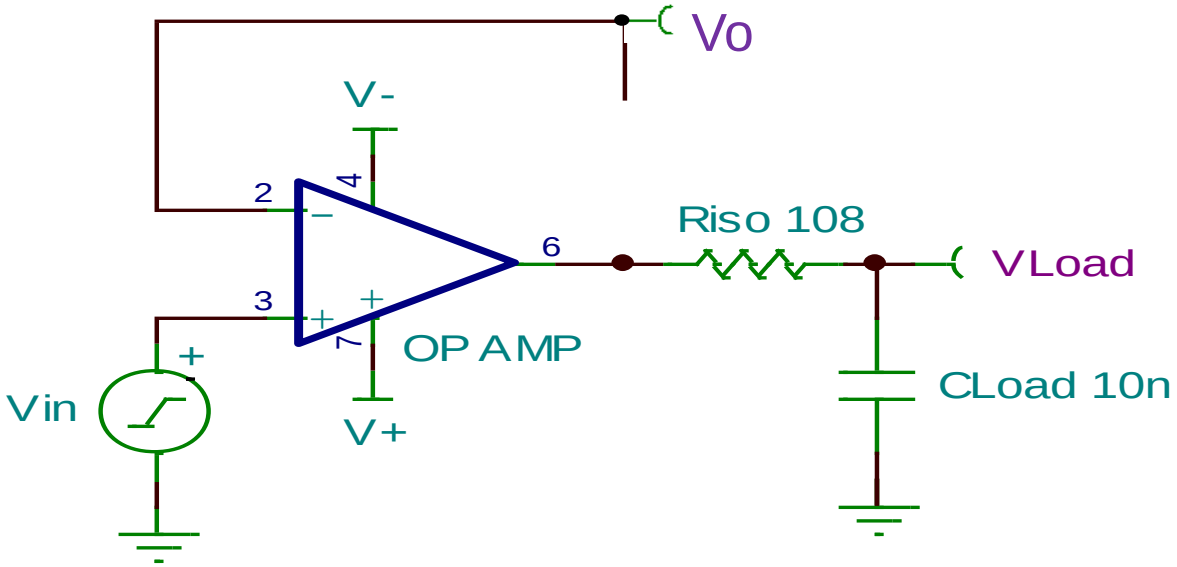
A_{OL} load



Loaded A_{OL} =

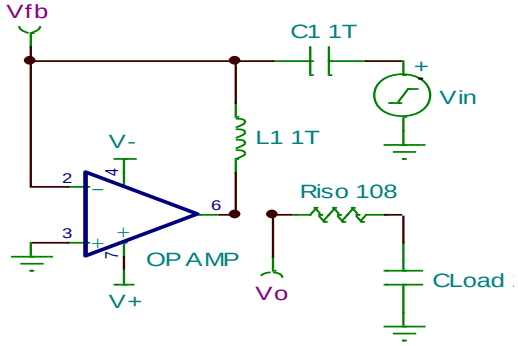


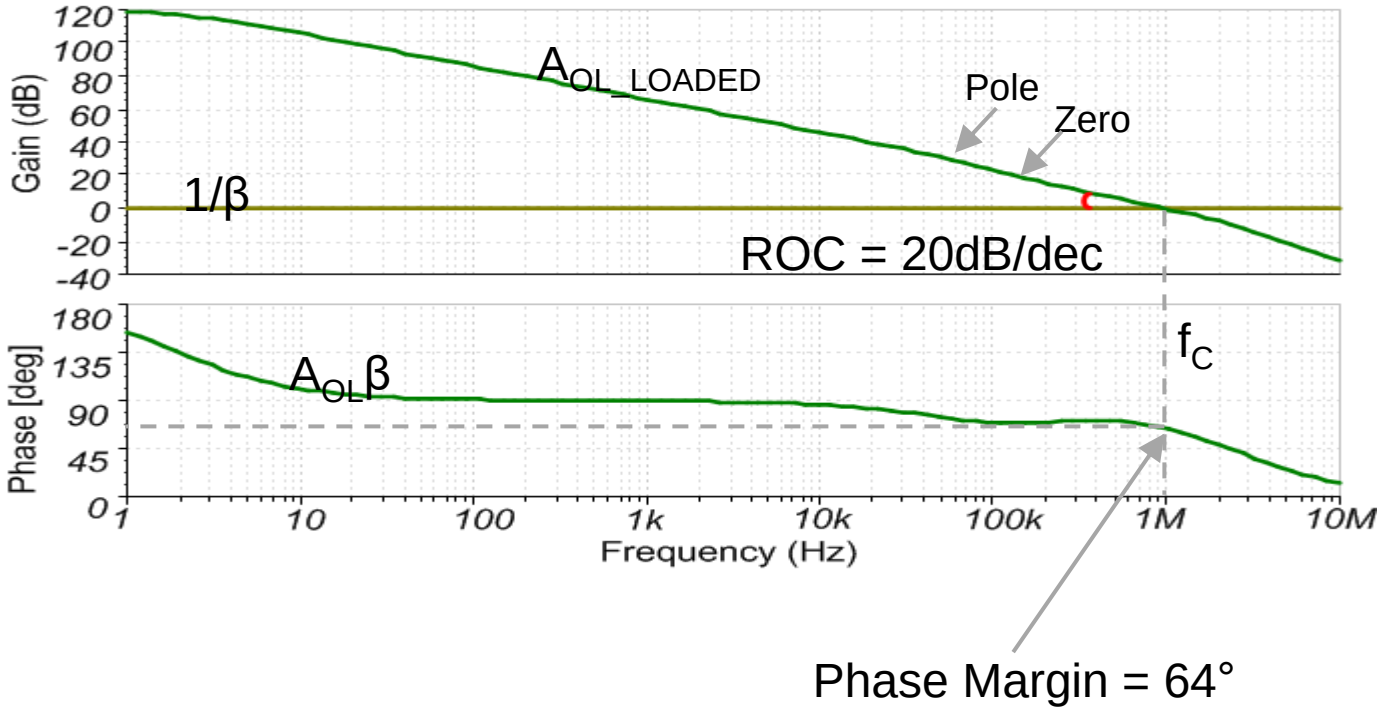
Compensation method 1: R_{ISO}



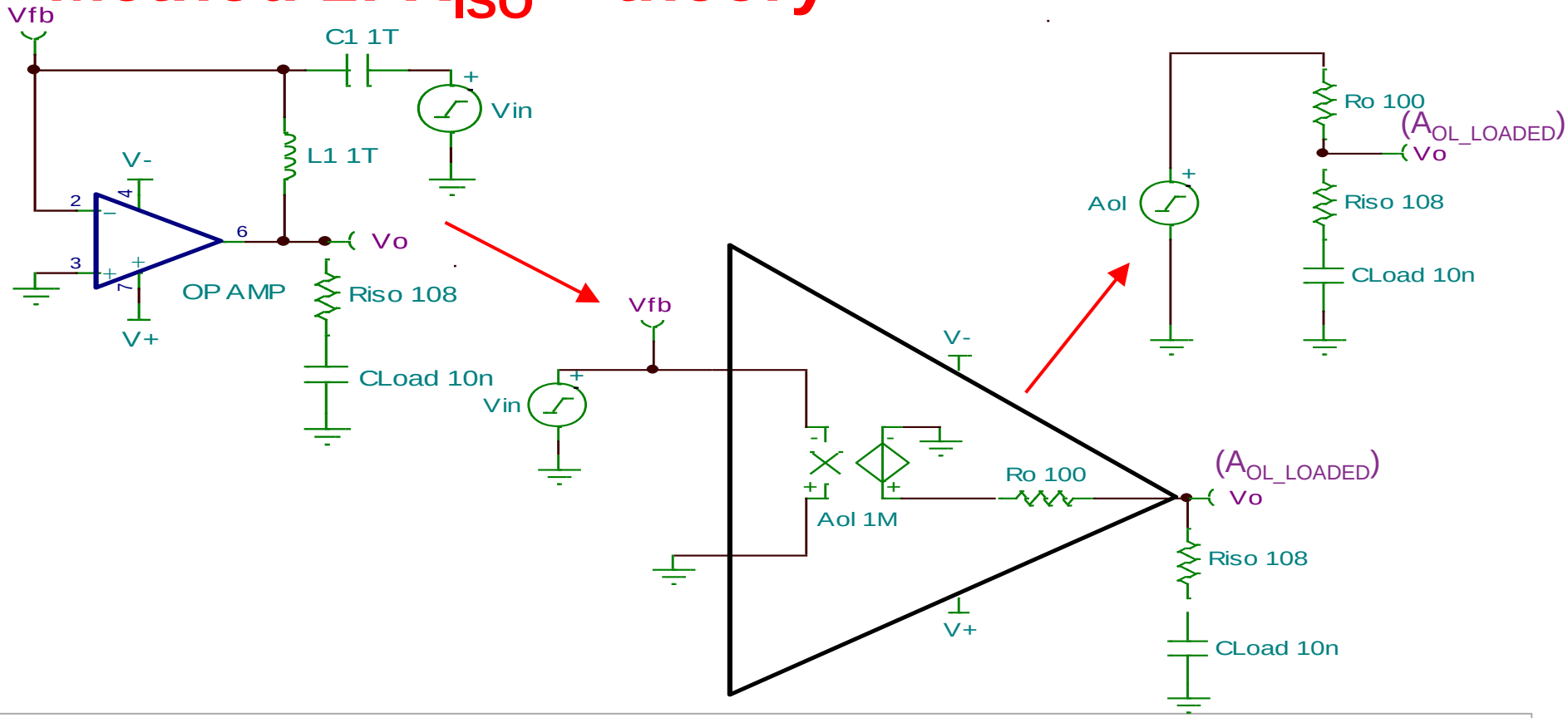
Method 1: R_{ISO} – results

Theory: Adds a zero to cancel the pole in loaded A_{OL}

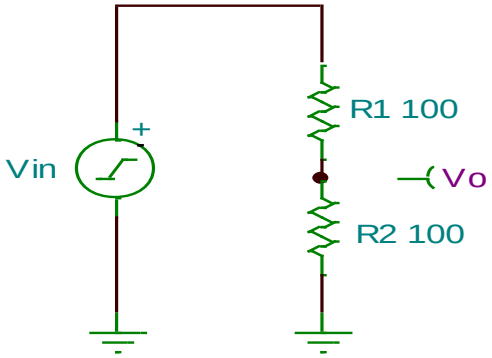




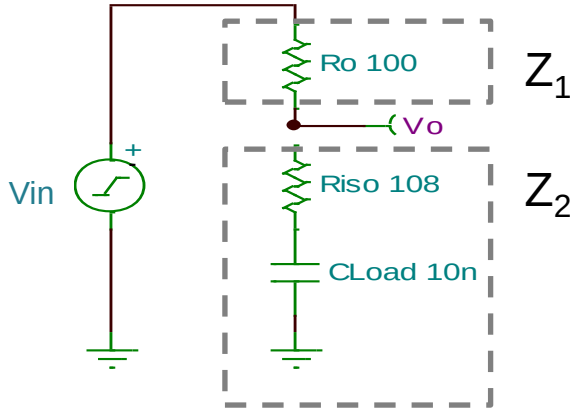
Method 1: R_{ISO} – theory



Resistor divider analogy



$$\frac{V_O}{V_{IN}} = \frac{R_2}{R_2 + R_1}$$



$$\frac{V_O}{V_{IN}} = \frac{Z_2}{Z_2 + Z_1}$$

$$\frac{V_O}{V_{IN}} = \frac{R_{ISO} + \frac{1}{s * C_{LOAD}}}{\left(R_{ISO} + \frac{1}{s * C_{LOAD}}\right) + R_O}$$

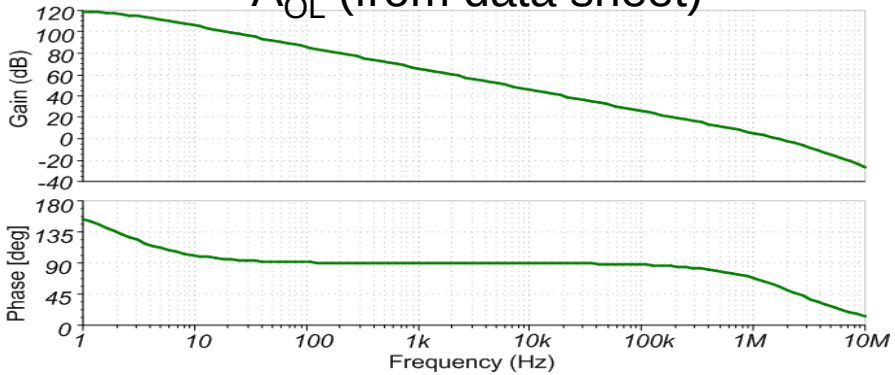
$$\frac{V_O}{V_{IN}} = \frac{1 + s * R_{ISO} * C_{LOAD}}{1 + s * (R_{ISO} + R_O) * C_{LOAD}}$$

Zero: R_{ISO} & C_{LOAD}

Pole: R_O, R_{ISO}, and C_{LOAD}

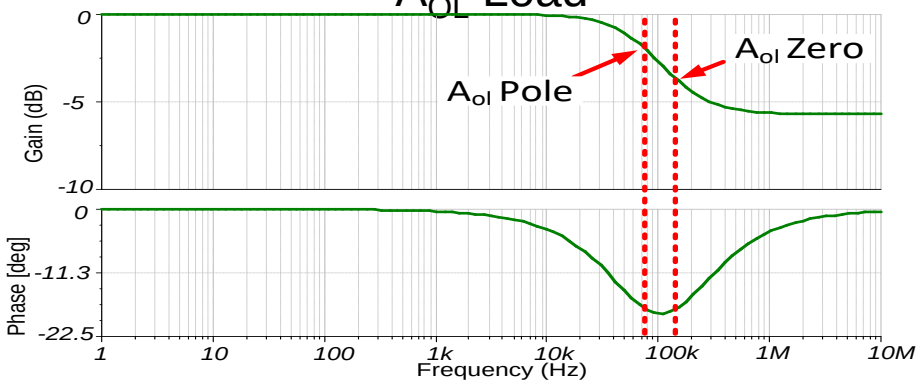
Method 1: R_{ISO} – theory

A_{OL} (from data sheet)

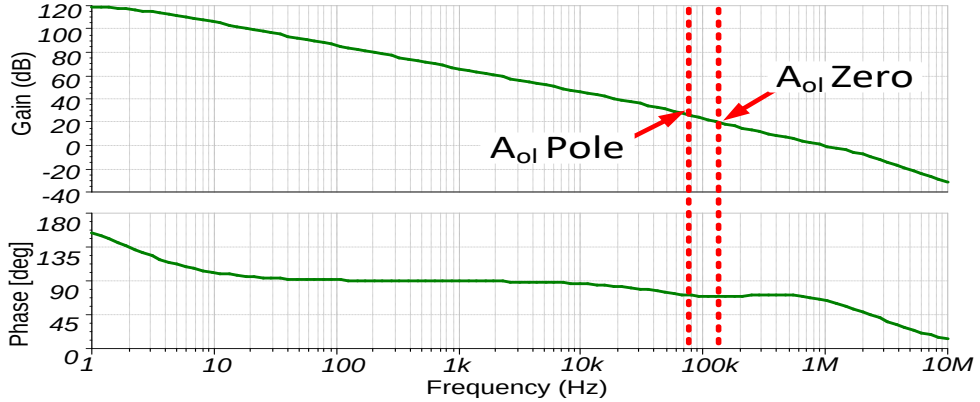


X

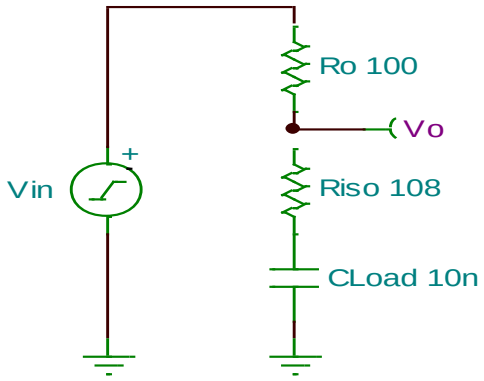
A_{OL} Load

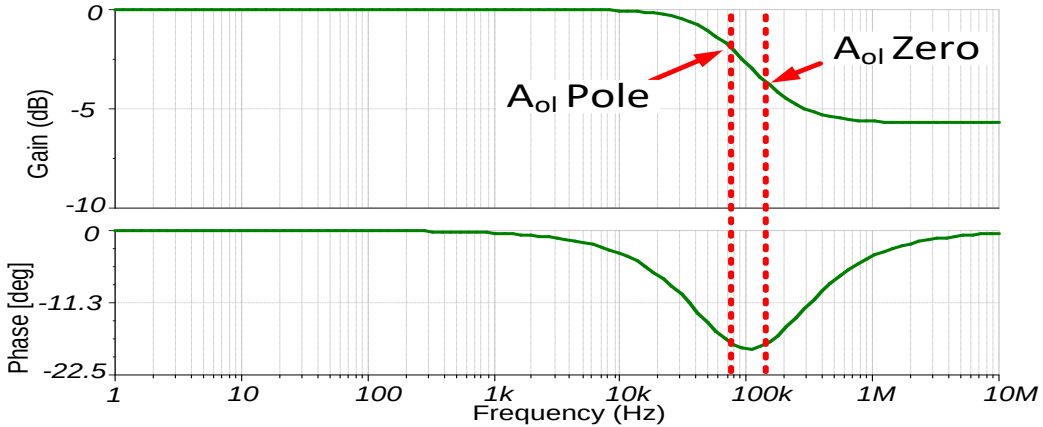


Loaded A_{OL} =



Method 1: R_{ISO} – theory





Transfer function:

$$\frac{V_o}{V_{in}}(s) = \frac{1 + s * R_{ISO} * C_{LOAD}}{1 + s * (R_O + R_{ISO}) * C_{LOAD}}$$

Zero equation:

$$f_{ZERO} = \frac{1}{2 * \pi * R_{ISO} * C_{LOAD}}$$

Pole equation:

$$f_{POLE} = \frac{1}{2 * \pi * (R_O + R_{ISO}) * C_{LOAD}}$$

Method 1: R_{ISO} – design

Design steps:

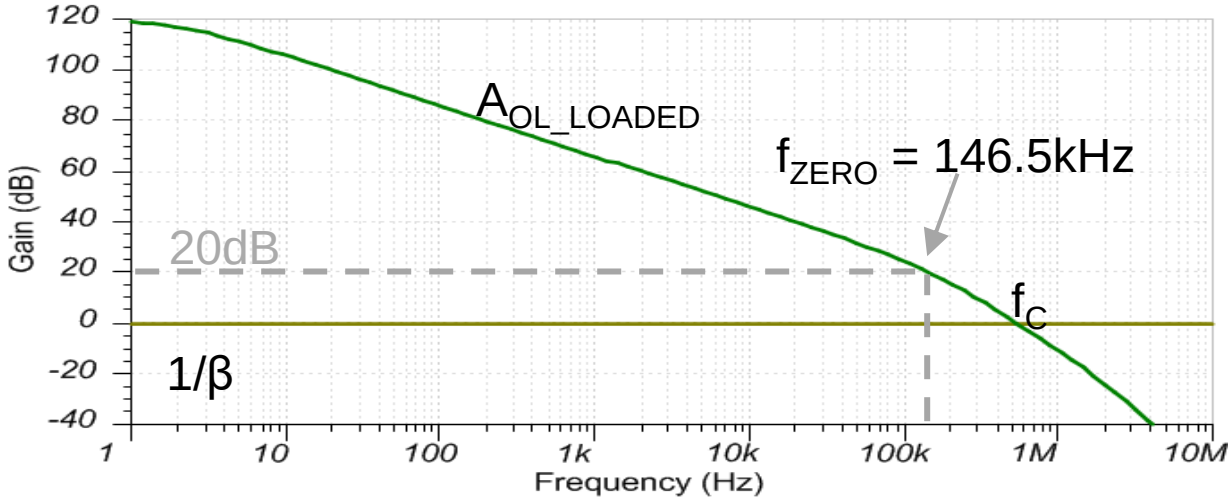
1.) Find the zero frequency, f_{ZERO}, where A_{OL_Loaded} = 20 dB
2.) Calculate Riso to set the zero at f_{ZERO}
This will yield between 60° and 90° degrees of phase margin

R_{ISO} equation:

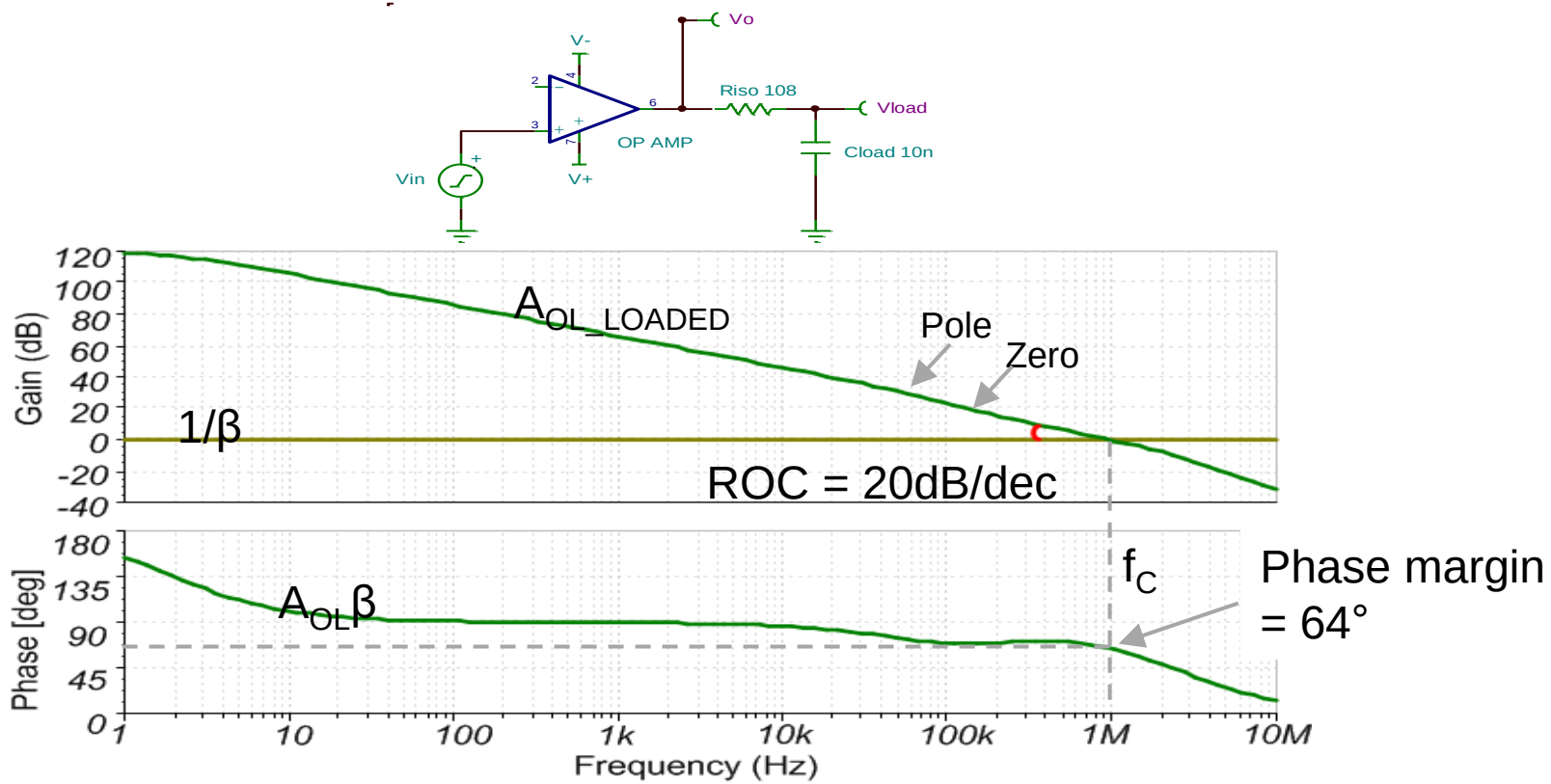
$$R_{iso} = \frac{1}{2 * \pi * f_{ZERO} * C_{LOAD}}$$

$$R_{iso} = \frac{1}{2 * \pi * 146.5kHz * 10nF}$$

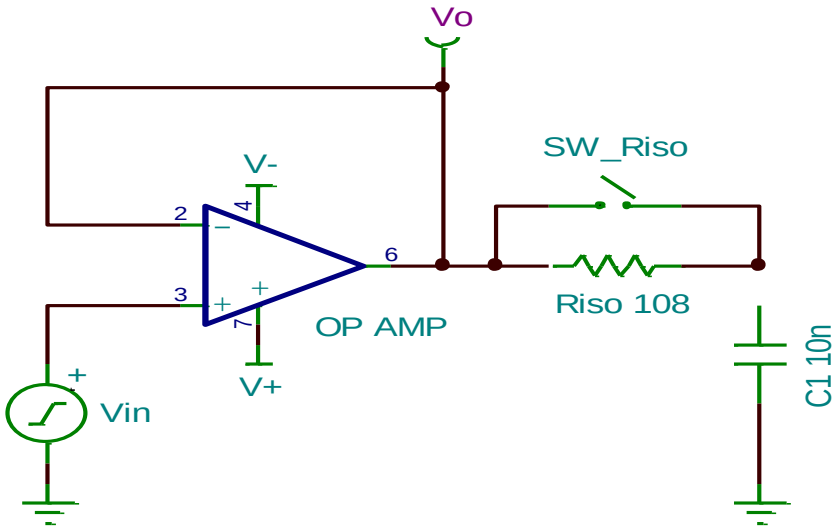
$$R_{iso} = 108\Omega$$

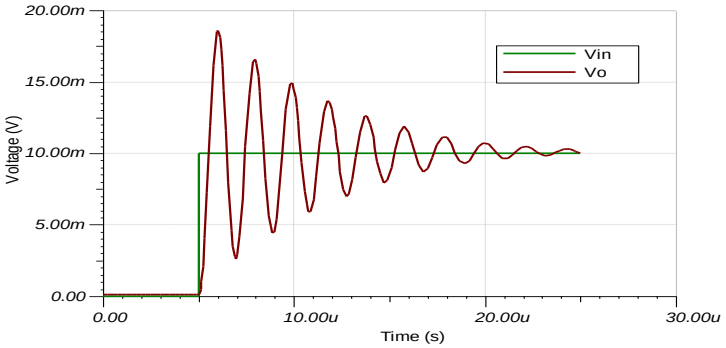


Method 1: R_{ISO} – design summary

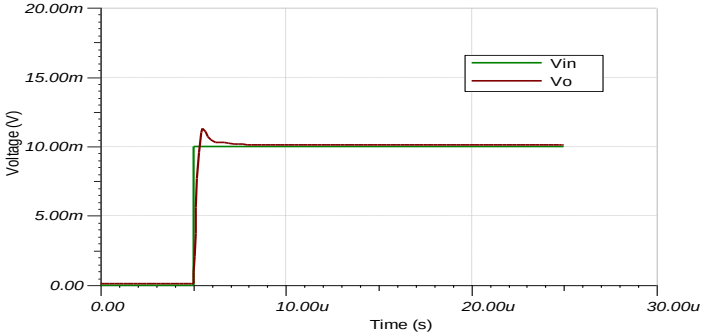


Unstable vs. stable transient results





No compensation - unstable

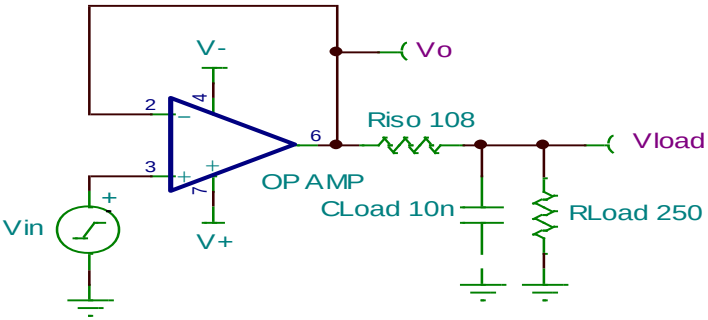


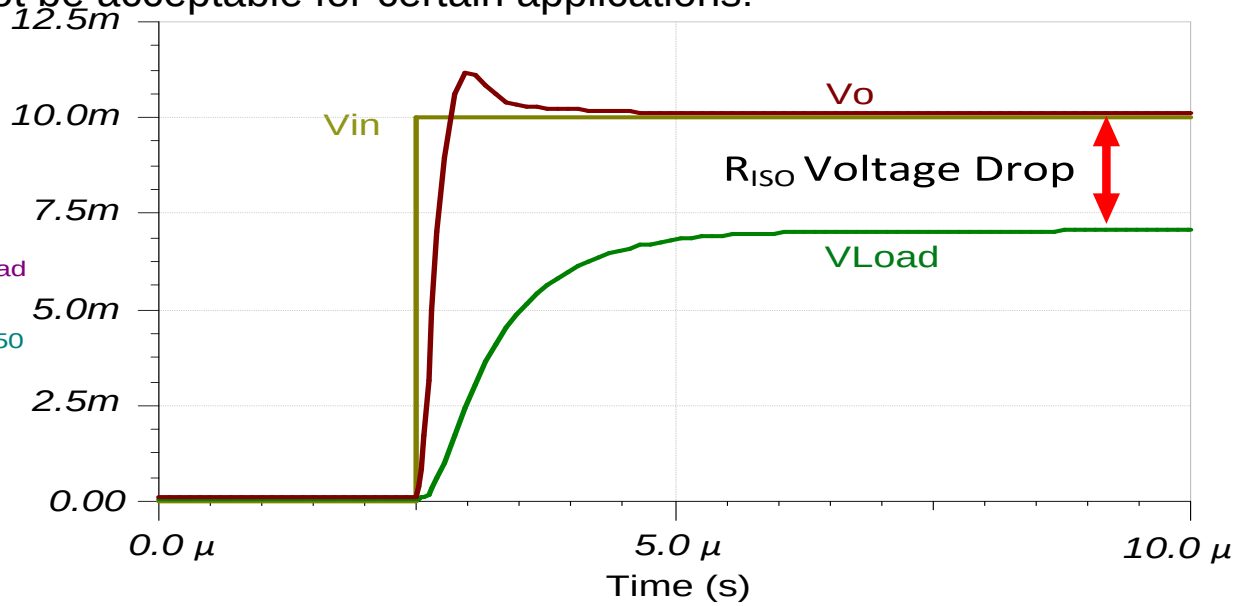
Riso compensation - stable

Method 1: R_{ISO} – disadvantage

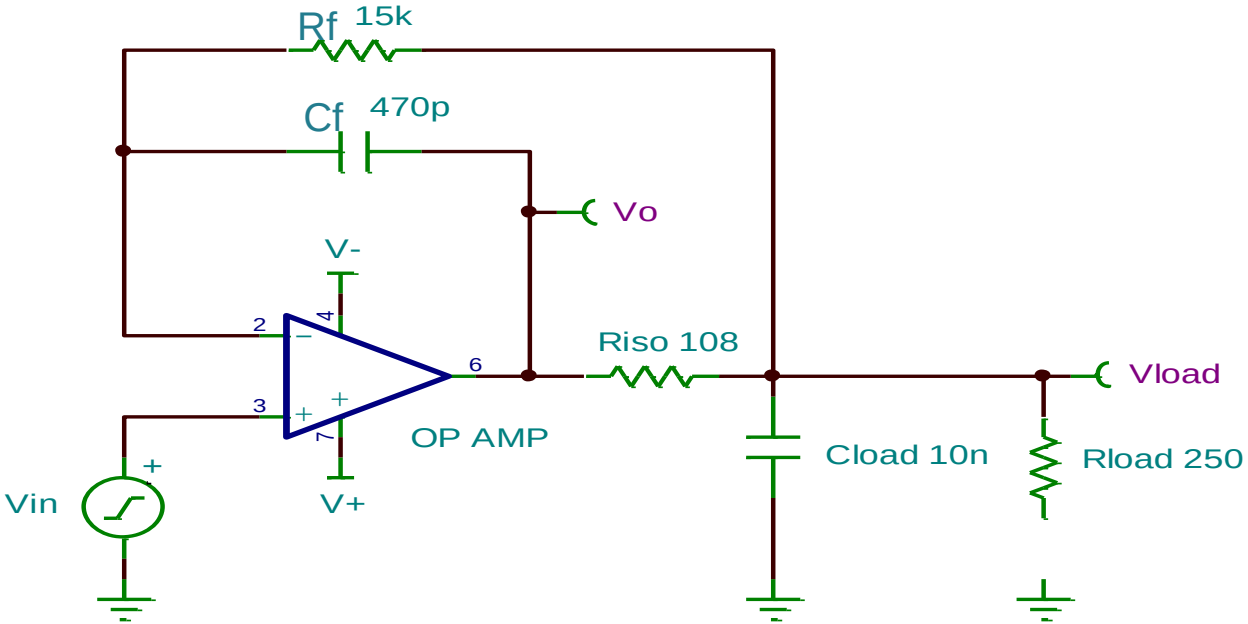
Disadvantage:

Voltage drop across R_{ISO} may not be acceptable for certain applications!





Method 2:
R_{ISO} + dual feedback



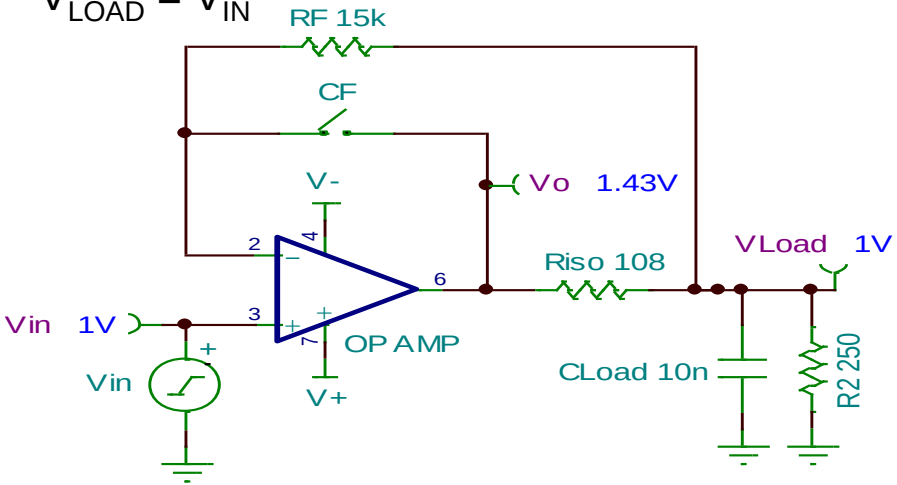
Method 2: R_{ISO} + dual feedback – theory

DC circuit

C_F: Open

R_F: Closes the feedback around R_{ISO}

$V_{LOAD} = V_{IN}$

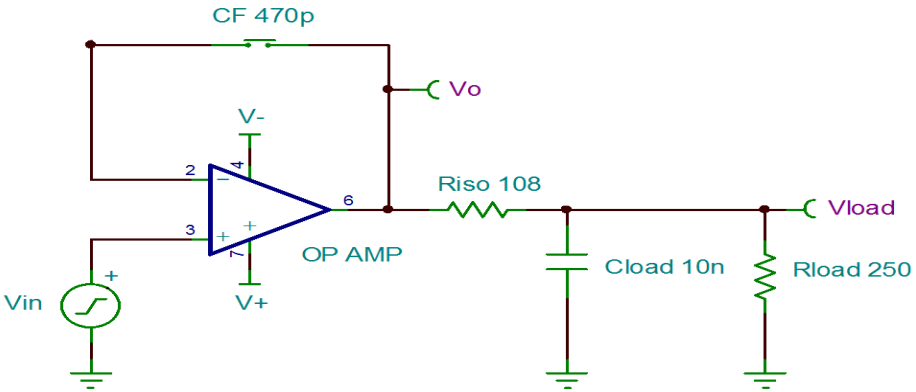


AC circuit

C_F: Short

R_F >> Z_{CF}, therefore R_F is effectively open

Behaves like R... circuit



Method 2: R_{ISO} + dual feedback - design

Design steps:

1) Set R_{ISO} using Method 1: R_{ISO} techniques
2) Set R_F: $\frac{5 \times R_{iso} \times C_L}{R_F} \leq C_F \leq \frac{10 \times R_{iso} \times C_L}{R_F}$
3) Set C_F: $\frac{5 \times R_{ISO} \times C_{LOAD}}{C_F} \leq C_F \leq \frac{10 \times R_{ISO} \times C_{LOAD}}{C_F}$ lower values of C_F = faster settling, higher overshoot

Rule 3 ensures that the two feedback paths will never create a resonance that would cause instability

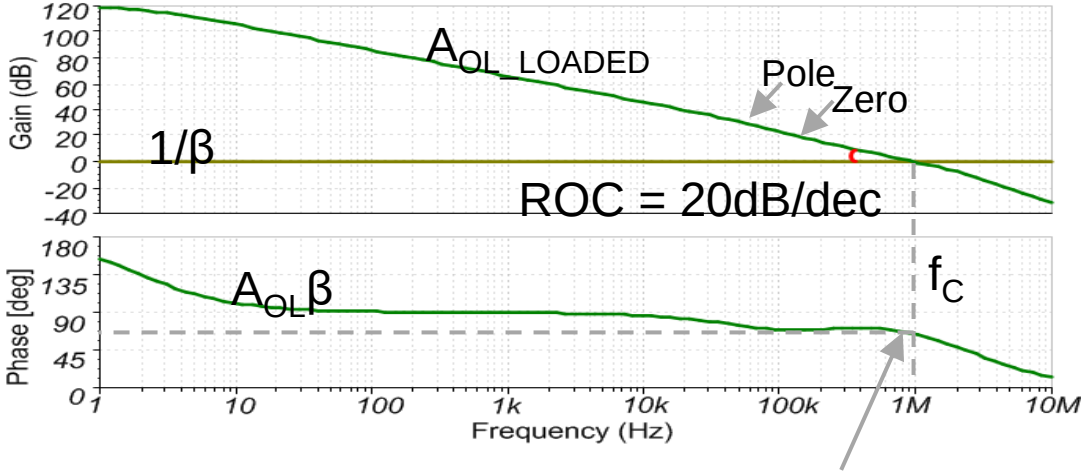
$$R_{ISO} = 108\Omega$$

$$R_F \geq R_{ISO} * 100$$

$$R_F \geq 10.8k\Omega$$

$$\frac{5 \times R_{iso} \times C_L}{R_F} \leq C_F \leq \frac{10 \times R_{iso} \times C_L}{R_F}$$

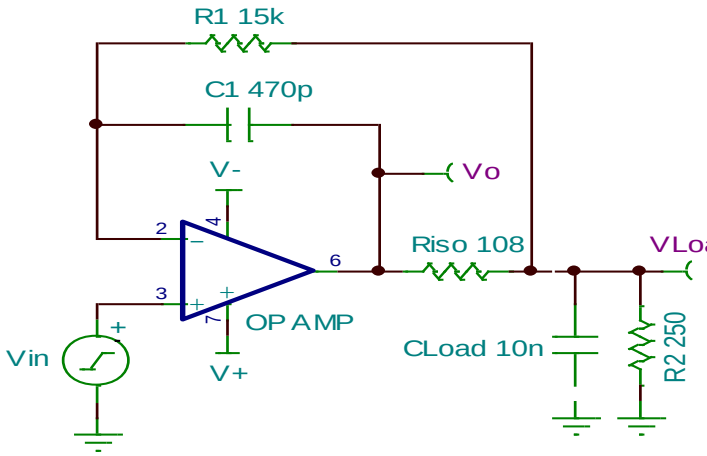
$$420pF \leq C_F \leq 720pF$$

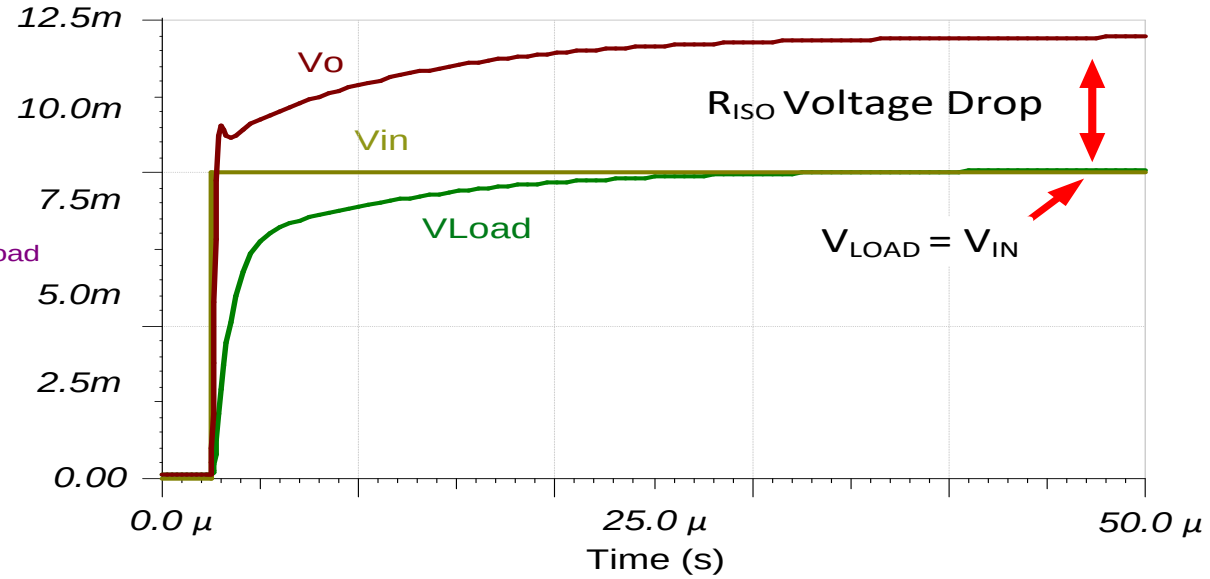


Phase Margin = 66°

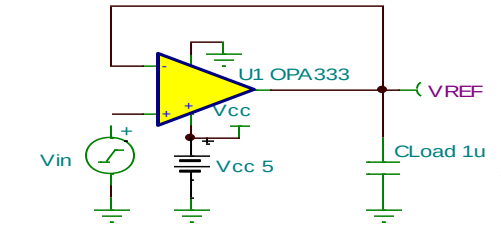
Method 2: R_{ISO} + dual feedback - results

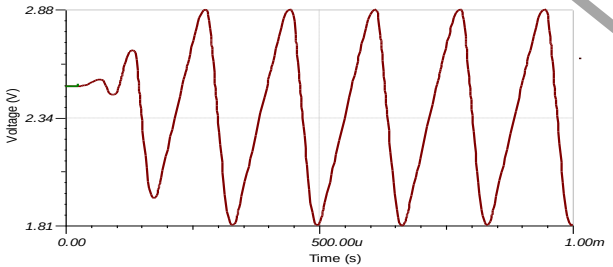
- V_{LOAD} matches V_{IN} – No voltage divider error!
- This topology has some limitations on settling time and capacitive load range

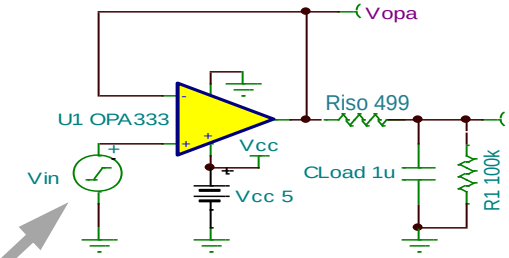


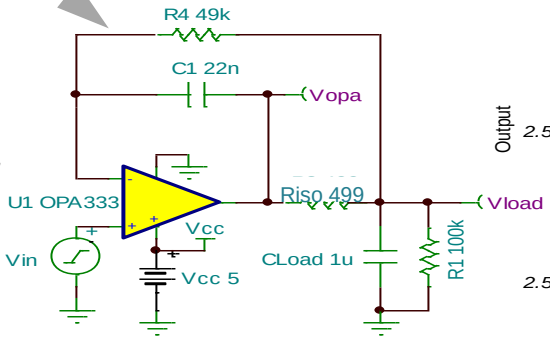


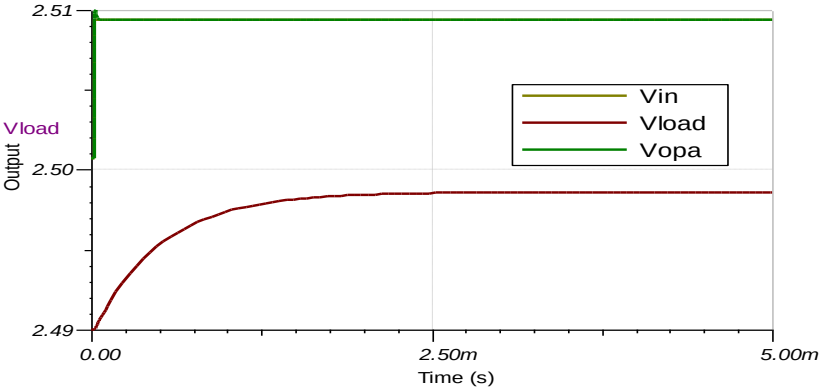
Summary – solving op amp stability

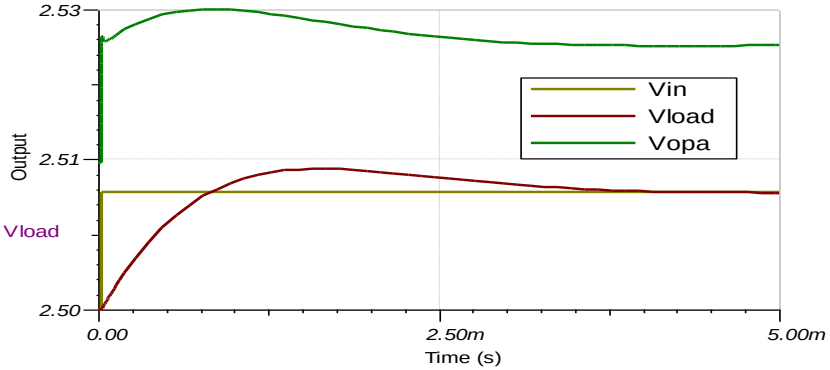




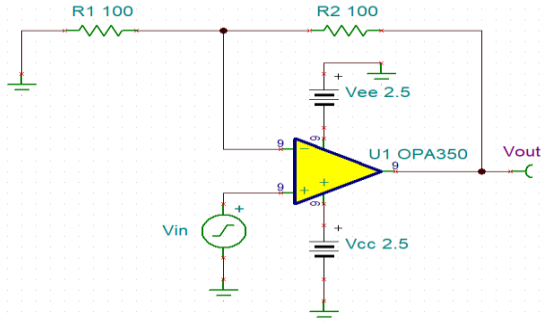


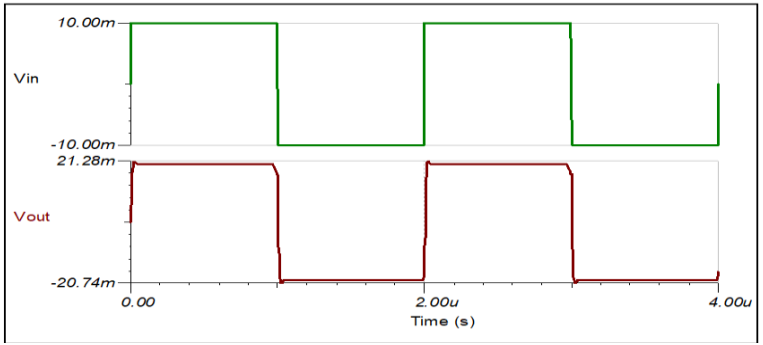


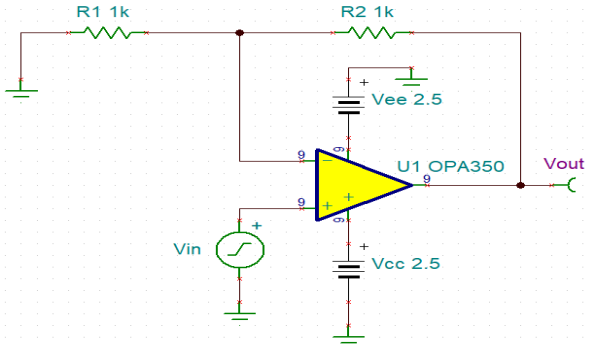


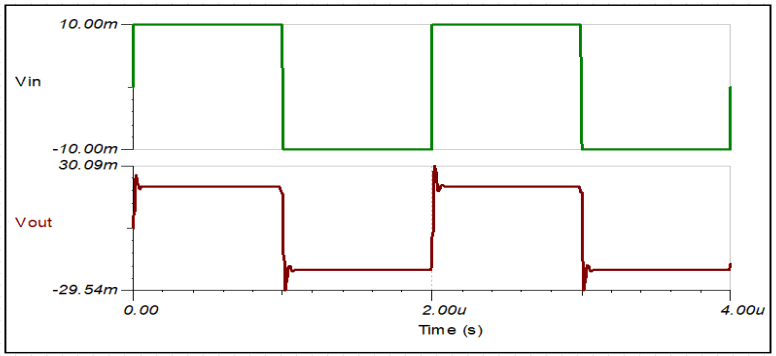


Solving op amp stability

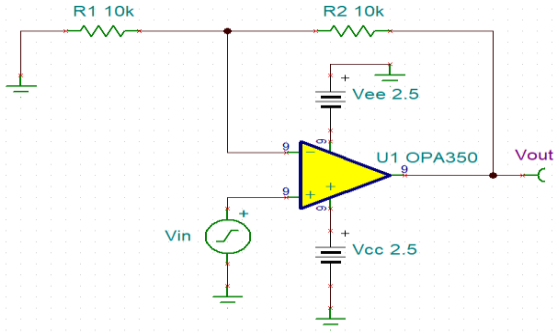


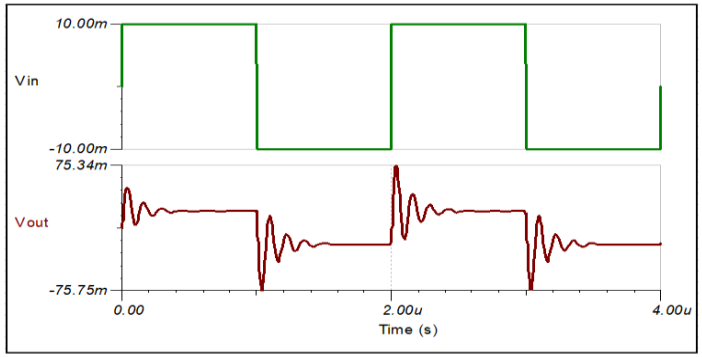


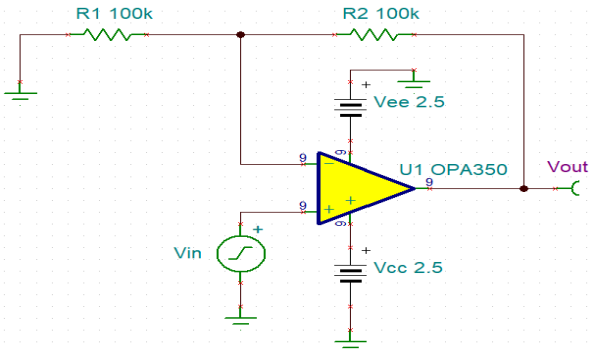


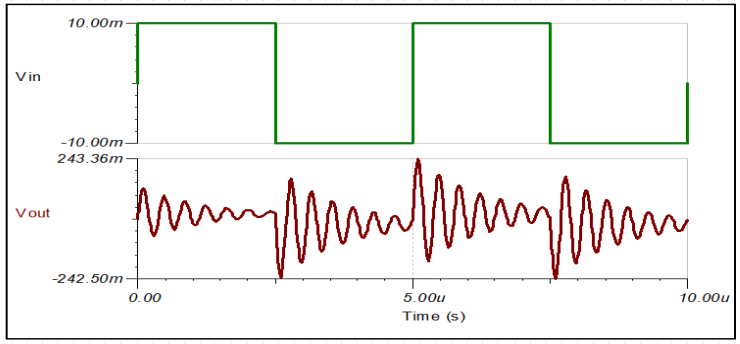


Solving Op Amp Stability

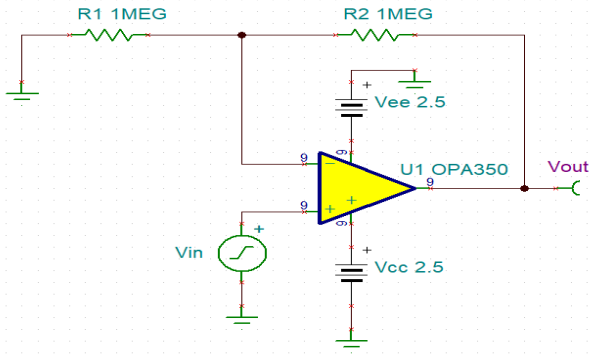


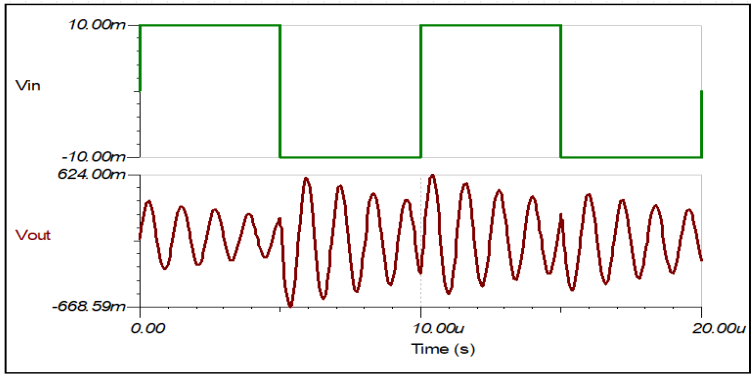


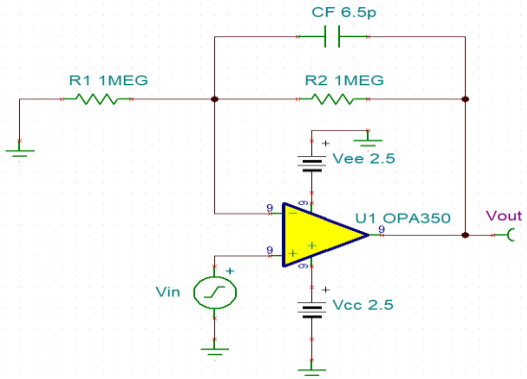


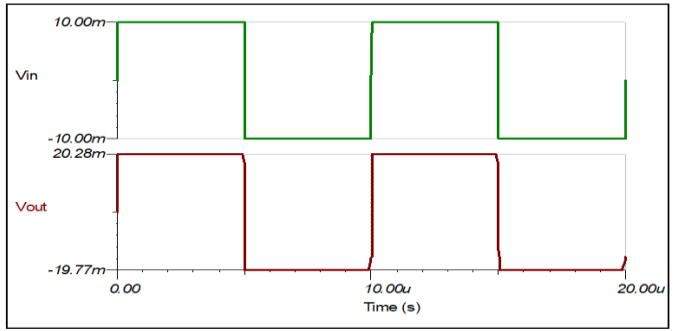


Solving op amp stability









Questions?

Thanks for your time!

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