TI Precision Labs Seminar

Amplifier fundamentals and specifications

Texas Instruments

Anatomy of a data sheet

- Introduction
- Absolute maximum specifications
- Specification tables
- Typical graphs
- Detailed description overview
- Applications information
- Layout recommendations
- Package and ordering information

OPA928 16-V, Femtoampere Input Bias, Precision, Rail-to-Rail Input/Output, e-trim™ Operational Amplifier

1 Features

- Ultra-low input bias current:
  - 20 fA (tested max) at 25°C and 85°C
- Low noise:
  - 0.05 fA/√Hz at 0.1 Hz
  - 15 nV/√Hz at 1 kHz
- High dc precision:
  - ±5 µV input offset voltage
  - ±0.1 µV/°C offset voltage drift
- Wide bandwidth: 2.5-MHz GBW
- Low quiescent current: 275 µA
- EMI and RFI filtered inputs
- High precision guard buffer
- Wide supply: ±2.25 V to ±8 V, 4.5 V to 16 V
- Rail-to-rail input and output
- High capacitive load drive capability: 1 nF
- Operating temperature range: –40°C to +125°C
- Industry standard package:
  - 8-pin SOIC

2 Applications

- Electrochemical meter - pH meter
- Lab and field Instrumentation
- Mass spectrometer
- Ion chromatography (IC) instrument
- Spectrophotometer

3 Description

The OPA928 is a new generation, 16-V, femtoampere input bias, e-trim™ operational amplifier. This device offers an ultra-low input bias current of 20 fA (max) at 25°C and 85°C. The OPA928 input bias performance is tested at production at both temperatures.

The device features near-zero input bias plus outstanding dc precision and ac performance, including rail-to-rail input/output, low offset voltage (±5 µV, typical), low offset drift (±0.1 µV/°C, typical), and low current noise (0.05 fA/√Hz at 0.1 Hz). These features make the OPA928 an excellent choice for low-light photodiode and high source-impedance applications.

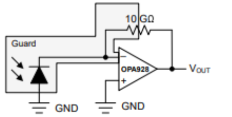
The OPA928 features an internal, high precision guard buffer to protect high impedance input traces from undesirable current leakage in sensitive applications. The OPA928 packaging and pin out is designed to support low-leakage circuit designs.

The OPA928 is specified from –40°C to +125°C.

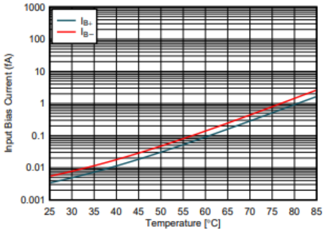
Package Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
OPA928	D (SOIC, 8)	4.90 mm × 3.90 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



High Gain Transimpedance Amplifier



Input Bias Current vs Temperature (V_S = 16 V, V_{CM} = Mid-Supply)

Data Sheet: absolute maximum specification

6.1 Absolute maximum ratings

Over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
V_s	Supply voltage, V_s = (V+) – (V-)	-0.3	6	V
	Input voltage, all pins	(V-) – 0.3	(V+) + 0.3	V
	Input current (INA+, INA-, INB+, INB-, INSA/B, OUTSA/B/1/2/3)	-10	10	mA
	Output short-circuit[2]	Cont.	Cont.	
T_A	Operating temperature	-55	150	°C
T_J	Junction temperature	-55	150	°C
T_{stg}	Storage temperature	-55	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Short-circuit to ground, one amplifier

Applying signals above absolute maximum can damage the device.

Inputs are often limited by ESD diodes

Excerpt from OPA328 data sheet

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	2000	V
		Charge-device model (CDM), per ANSI/ESDA/JEDEDC JS-002[2]	500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

ESD ratings indicate how robust a device is to electrostatic discharge

Data Sheet: specification table

Test conditions at the top apply to all parameters unless otherwise specified.

6.6 Electrical characteristics

at T_A = 25°C, V_S = ±1.1V to ±2.75V (V_S = 2.2V to 5.5V), R_L = 10kΩ connected to V_S / 2, V_{CM} = V_{OUT} = V_s / 2, and min and max specification established from manufacturing final test (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OPAx328 | OFFSET VOLTAGE						
V_{OS}	Input offset voltage	OPA2328DGK		±3	±50	μV
		OPA328DBV		±3	±75	
dV_{OS}/dT	Input offset voltage drift	T_A = -40°C to 125°C		±0.15	±1	μV/°C
PSRR	Power-supply rejection ratio	V_S = ±1.1 V to ±2.75 V		±1	±10	μV/V
		V_S = ±1.1 V to ±2.75 V, T_A = -40°C to +125°C		±15	±40	

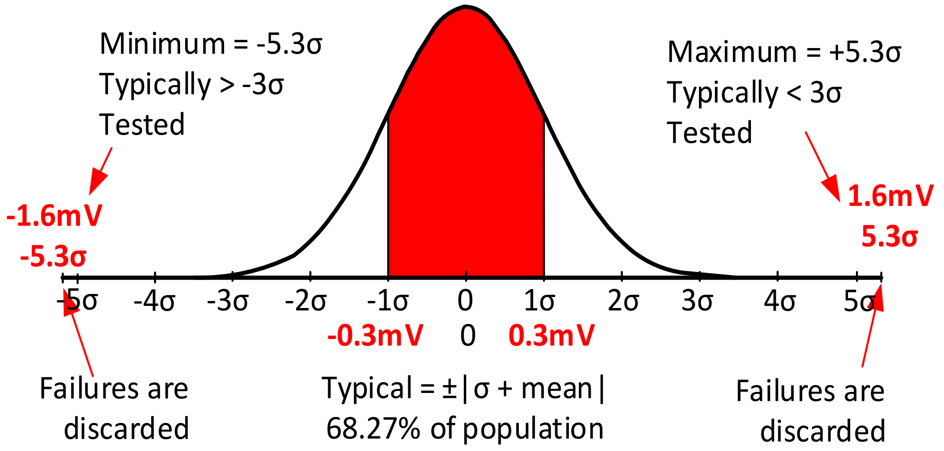
Overrides test condition at top of table

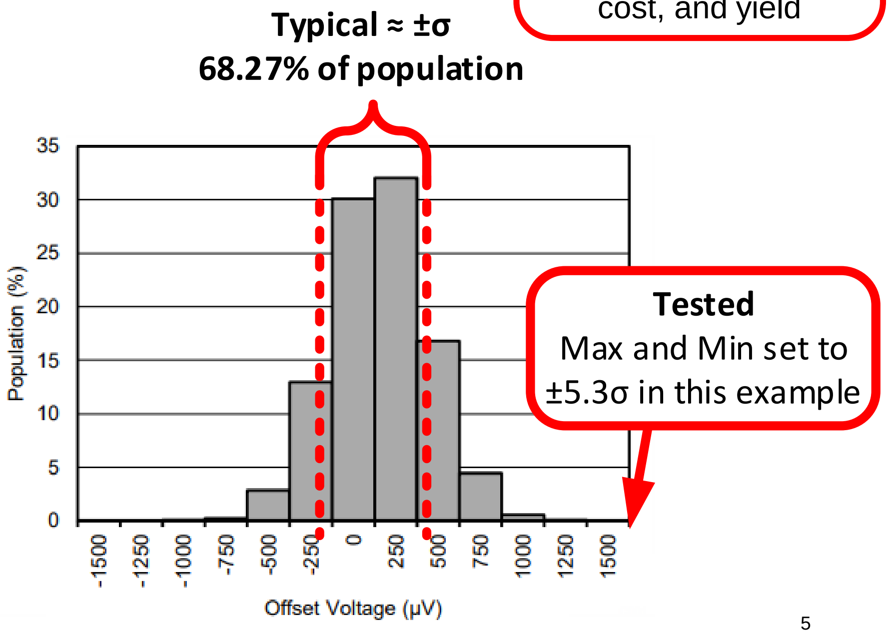
Data sheet: specification table

PARAMETER TLV9062		MIN	TYP	MAX	UNITS
V_{OS}	Input offset voltage		±0.3	+1.6	mV

σ value to set min and max limit can vary device-to-device based on application, cost, and yield

Gaussian Distribution





Methods for generating specifications

Final test or probe

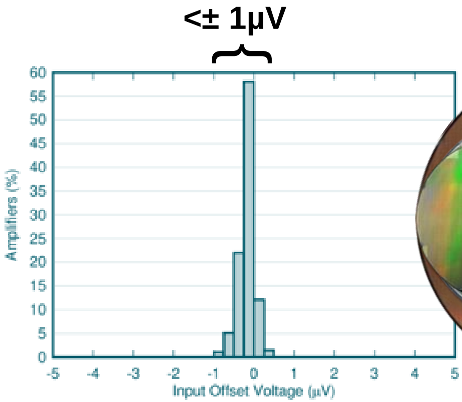
- This is done for each product before we ship it
- Automated test - very fast, millions tested each year
- Devices outside the limit are discarded
- Normally done at room temperature
- Wafer probe may be done across temperature

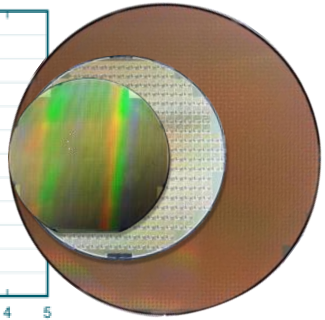
Characterization

- One time manual bench test for statistical sample of devices
- Used to generate curves and some table specifications

IC design across process corners

- Used for very few parameters in table
- Usually done for parameters difficult to measure (e.g. internal switch resistance, current noise in fA)
- Simulated across process corners
- All measured data is typically compared to simulation



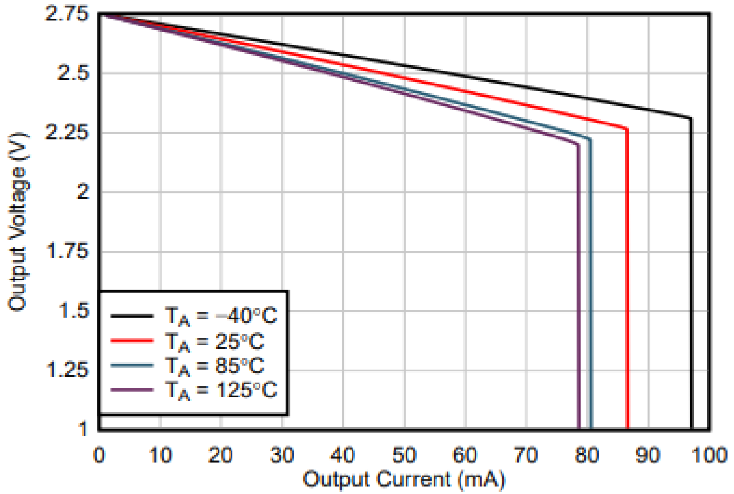


Data sheet: typical plots

Test conditions at the top apply to all curves unless otherwise specified.

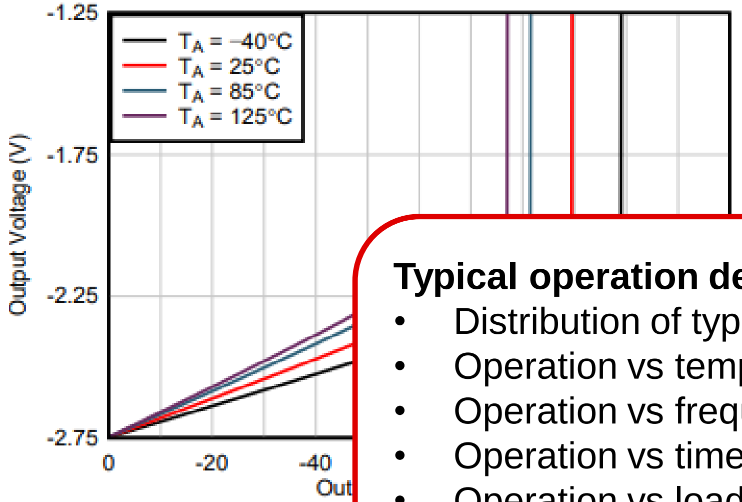
6.7 Typical characteristics (continued)

At T_A = 25°C, V_S = 5.5 V, V_{CM} = V_{OUT} = mid-supply, C_L = 20pF, and R_L = 10kΩ (unless otherwise noted)



V_{V+} = 2.75 V, $V_{V–}$ = –2.75 V, current source load

Figure 5-21. Output Voltage Swing vs Output Current



V_{V+} = 2.75 V, $V_{V–}$ =

Figure 5-22. Output Voltag

Typical operation details for:

- Distribution of typical error
- Operation vs temperature
- Operation vs frequency
- Operation vs time
- Operation vs load current
- Operation vs load capacitance

Excerpt from OPA328 data sheet

Data sheet: detailed description

8.3 Feature Description

8.3.1 Input Overvoltage Protection

The inputs of the OPAx206 are individually protected for voltages up to ±40 V beyond either supply. For example, a common-mode voltage anywhere between –55 V and +55 V does not cause damage when powered from ±15-V supplies. Internal circuitry on each input provides low series impedance under normal signal conditions thus maintaining high performance under normal operating conditions. If the input is overloaded, the protection circuitry limits the input current to a value of approximately 4.8 mA.

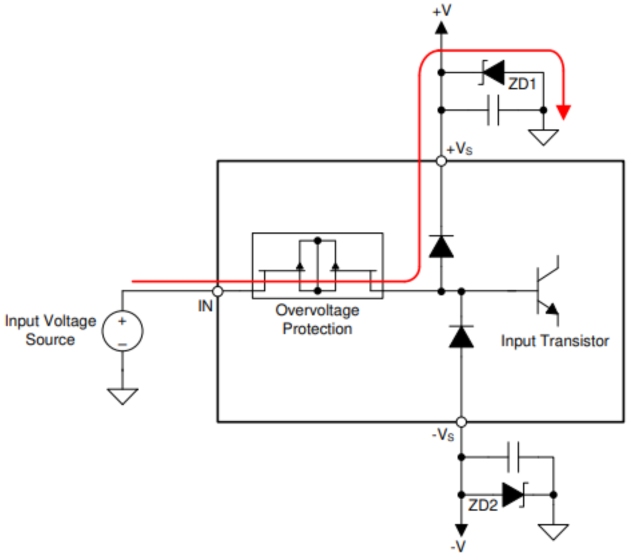


Figure 8-1. OPAx206 Input Overvoltage Current Path

Differentiating features explained

- Trim methods
- ESD and protection
- Background on key specification

Excerpt from OPA206 data sheet

Data Sheet: layout

8.4.2 Layout Examples

Excerpt from OPA928 data sheet

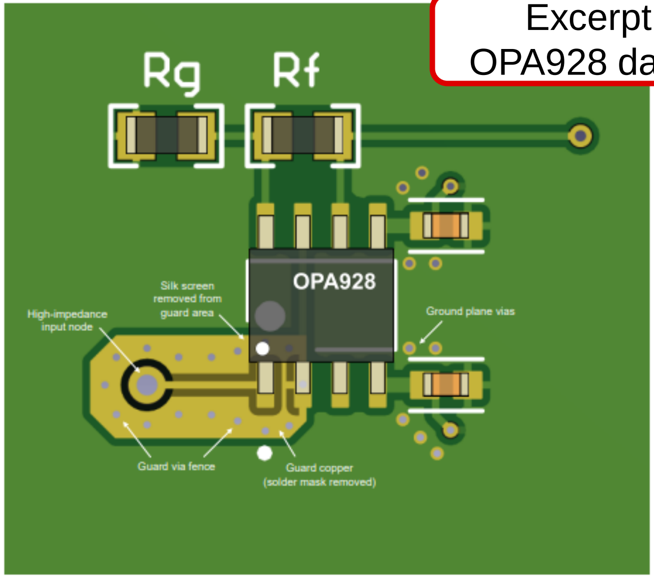


Figure 8-7. Layout Example: Noninverting Configuration

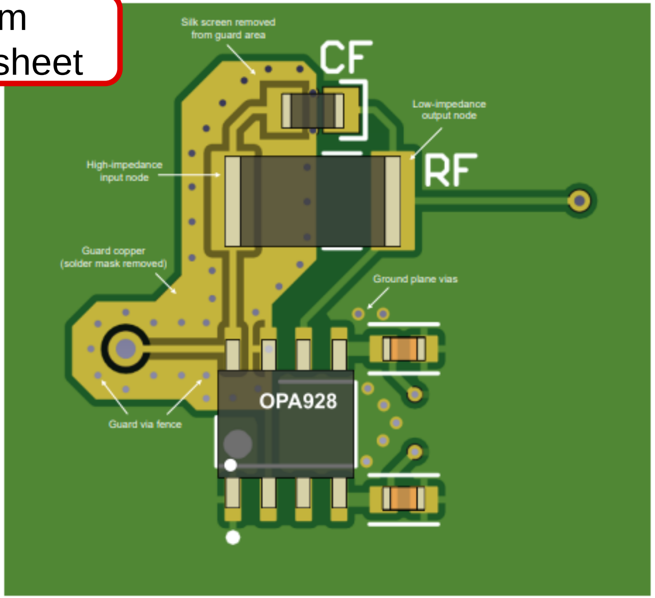
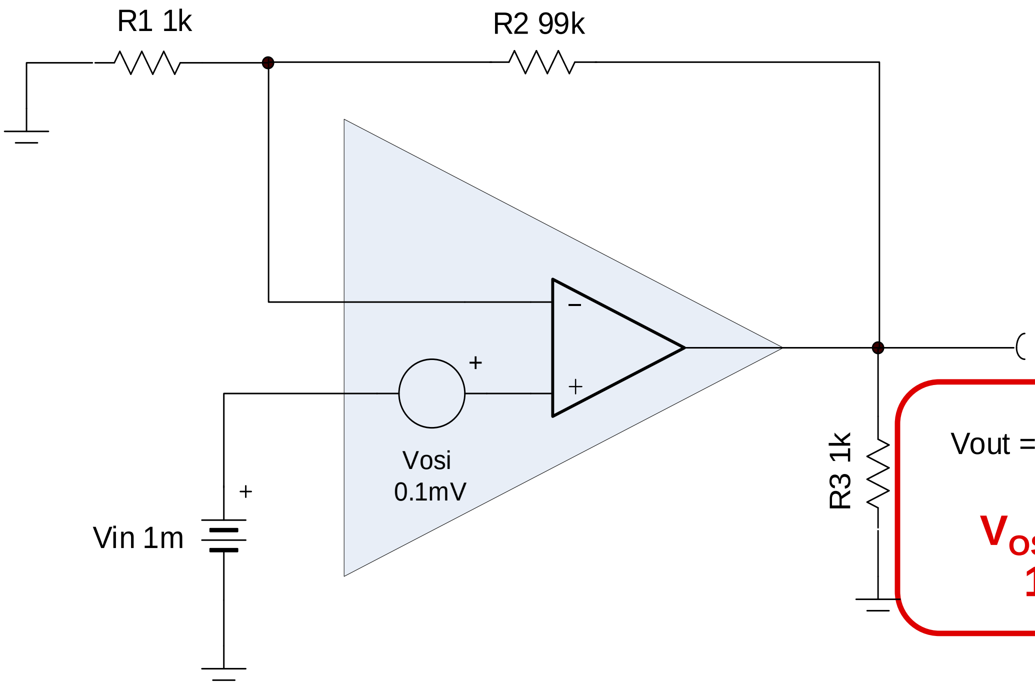


Figure 8-8. Layout Example: Inverting Configuration

Offset voltage and bias current

DC error type

Application example



Calculation of error due to Vos:

$$G_{ideal} = \frac{R_2}{R_1} + 1 = \frac{99k}{1k} + 1 = 100\ \frac{V}{V}$$

$$Vout_{actual} = G_{ideal} * (Vin + Vosi)$$

$$Vout_{actual} = 100\frac{V}{V} * (1\ mV + 0.1\ mV) = 110\ mV$$

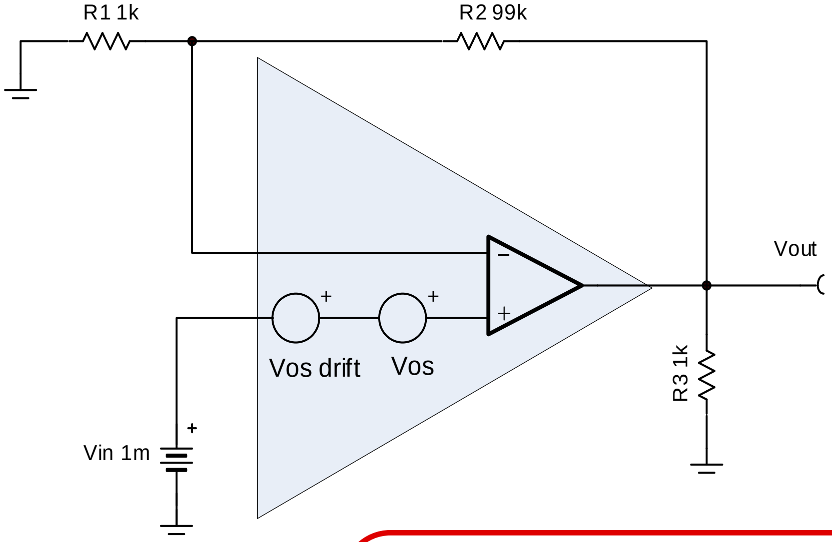
$$Error\% = \frac{Vout_{actual} - Vout_{ideal}}{Vout_{ideal}} * 100$$

$$Error\% = \frac{110\ mV - 100\ mV}{100\ mV} * 100\% = 10\%$$

Vout = (1mV+ 0.1mV)*(100)
Vout = 110mV

V_{OS} introduces 10% error!

Input offset drift calculations



Temp (°C)	V_{OS} Initial + drift + 3.5μV/C	V_{OS} Initial + drift - 3.5μV/C
-25°C	125μV	285μV
0°C	212.5μV	387.5μV
25°C	300μV	300μV
50°C	387.5μV	212.5μV
85°C	510μV	90μV
125°C	650μV	-50μV

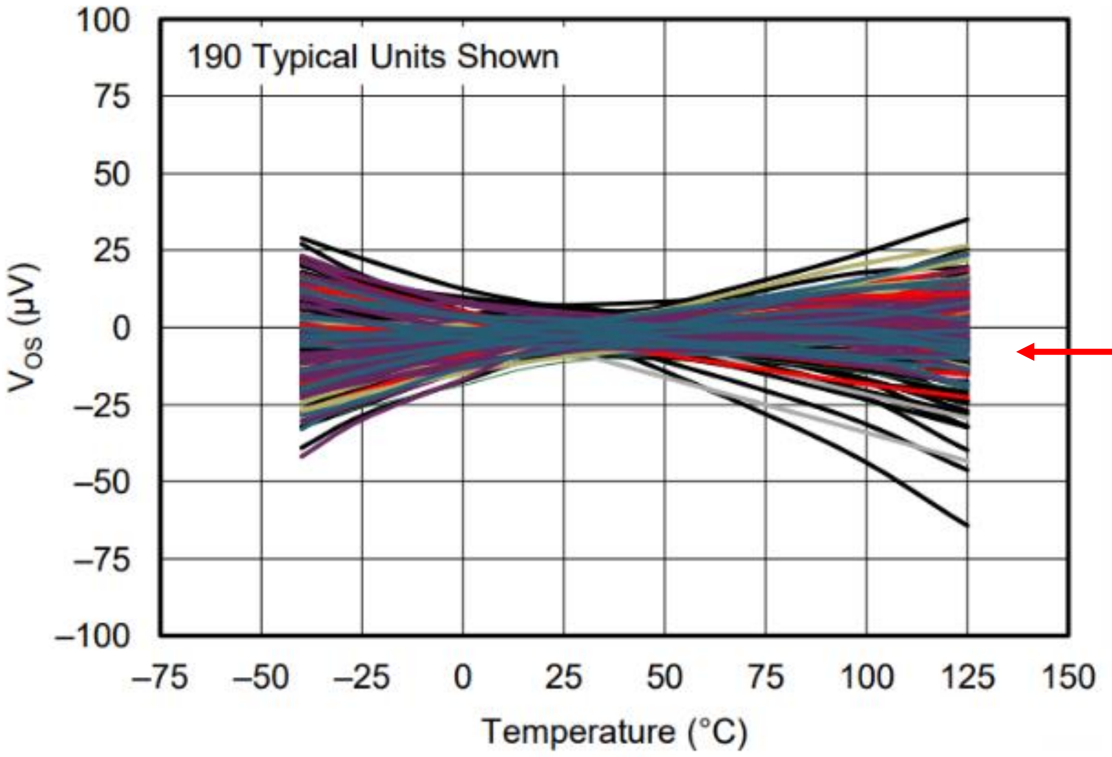
$$\boldsymbol{Vos = Vos_{room} + Vos_{drift} * (T - 25^{\circ}C)}$$

Example calculations:

$$Vos = 300\ \mu V \pm 3.5\ \frac{\mu V}{^{\circ}C} * (25^{\circ}C - 25^{\circ}C) = 300\ \mu V \qquad @\ 25^{\circ}C$$

$$Vos = 300\ \mu V \pm 3.5\ \frac{\mu V}{^{\circ}C} * (125^{\circ}C - 25^{\circ}C) = 650\ \mu V, -50\ \mu V \qquad @\ 125^{\circ}C$$

Offset drift may be non-linear

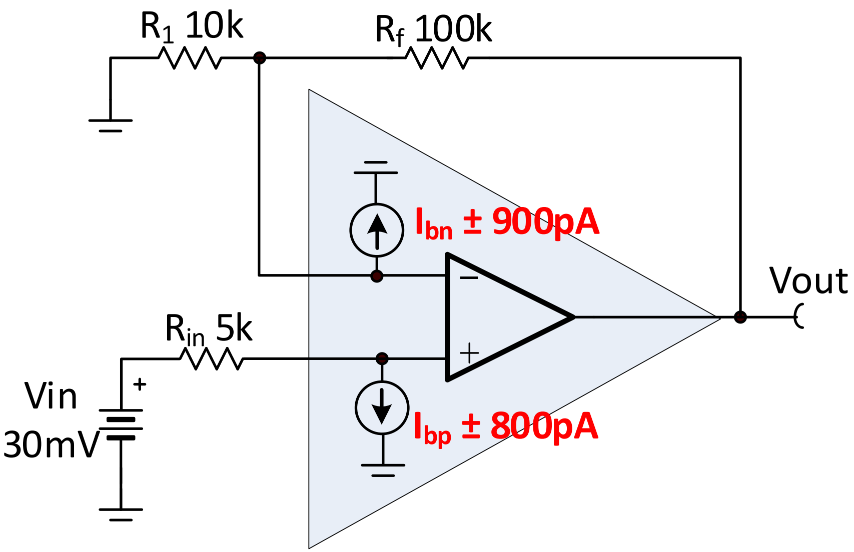


The previous example assumed that the drift was linear but it may be nonlinear

Range of input offset voltage (μV to mV)

Op amp	V_{OS} (max) (high grade)	V_{OS} drift (max) (high grade)	Technology
OPA387	2μV	0.012μV/°C	Low voltage zero drift CMOS
OPA182	4μV	0.012μV/°C	High Voltage zero drift CMOS
OPA2186	10μV	0.04μV/°C	24V zero drift CMOS
OPA192	25μV	0.5μV/°C	e-Trim™ High doltage CMOS
OPA210	35μV	0.5μV/°C	Super-beta bipolar
OPA863A	95μV	1.2μV/°C	e-Trim™ high speed bipolar
OPA827	150μV	1.5 μV/°C	JFET input, laser trim, bipolar
OPA828	300μV	1.3μV/°C	DiFET (JFET), laser trimmed
LMV841	500μV	5μV/°C	12V CMOS
OPA835	1.85mV	13.5μV/°C	High speed bipolar
LM741	3mV	15μV/°C	Bipolar commodity (lower cost)

Input bias current - I_B



Input offset current

$I_{OS} = I_{bp} - I_{bn}$

Bias current through Rin translates to offset voltage

$$R_{eq} = \frac{R_f \,.\, R_1}{R_f \,.+ R_1} = 9.09\text{k}\Omega$$

$$V_{os\_Ibn} = i_{bn} \cdot R_{eq} = (\pm 900pA) \cdot (9.09k\Omega) = \pm 8.18\mu V$$

$$V_{os\_Ibp} = i_{bp} \cdot R_{in} = (\pm 800pA) \cdot (5\ k\Omega) = \pm 4.0\mu V$$

$$V_{os\_Ib} = V_{os\_Ibp} + V_{os\_Ibn} = \pm 12.18\mu V$$

$$G_n = \frac{R_f}{R_1} + 1 = \frac{100\ k\Omega}{10\ k\Omega} + 1 = 11$$

$$V_{outIb} = V_{os\_Ib} \cdot G_n = (\pm 12.18\mu V) \cdot (11) = \pm 133.98\mu V$$

Range of input bias current (fA to µA)

Op Amp	I_B (max) (high grade)	Max I_B over temp.	Technology
OPA928	20 fA	20 fA	High Voltage CMOS (Internal Guard Buffer)
LMC6001	100 fA	4 pA	High Voltage CMOS
OPA392	0.8 pA	5 pA	Low Voltage CMOS
OPA2328	1 pA	10 pA	Low Voltage CMOS
OPA828	8 pA	400 pA	High Voltage JFET
OPA350	10 pA	500 pA	Low Voltage CMOS
OPA310	1 pA	30 pA	Low Voltage CMOS
OPA205	400 pA	600 pA	Super Beta Bipolar
OPA210	2 nA	4 nA	Very low noise Bipolar
LM2902B	35 nA	60 nA	Bipolar commodity (lower cost)
OPA863A	730 nA	1.2 µA	High Speed Bipolar

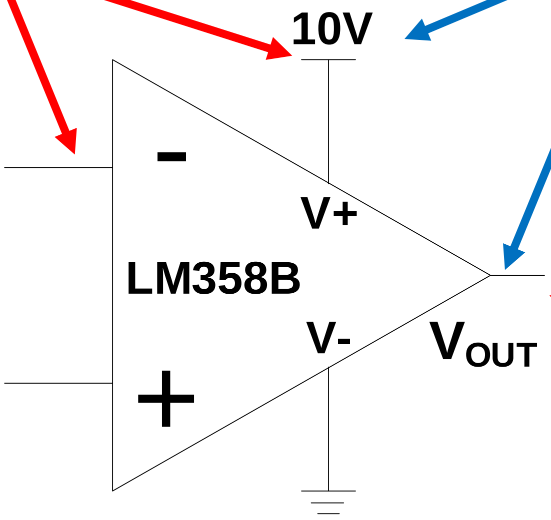
Common mode and output swing range

Functional operation requirement

Input and output voltage swing

Common mode range (V_{cm})
How close can the input get to either supply?

V_{cm} is the voltage either input.
Vin+ ≈ Vin-



Output swing
How close the output can get to either supply?

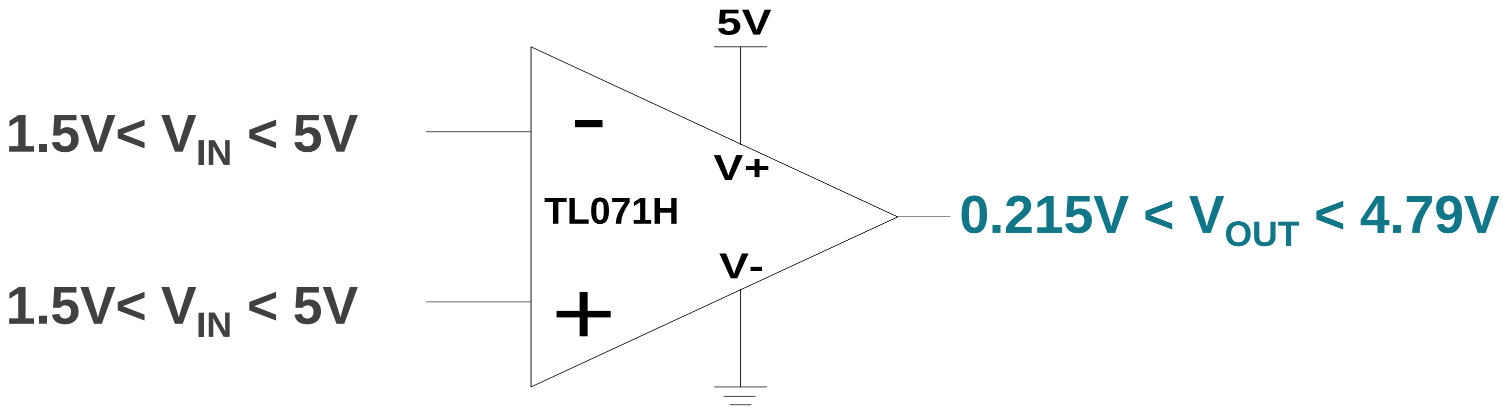
The output will clip or distort when either limit is violated

Translating the data sheet

6.7 Electrical characteristics TL07xH

For $V_S = (V_{CC+}) – (V_{CC–})$ = 4.5V to 40 V (±2.25V to ±20V) at T_A = 25°C, R_L = 10kΩ connected to V_S / 2, $V_{CM} = V_S$ / 2, and $V_{OUT} = V_S$ / 2, unless otherwise noted.

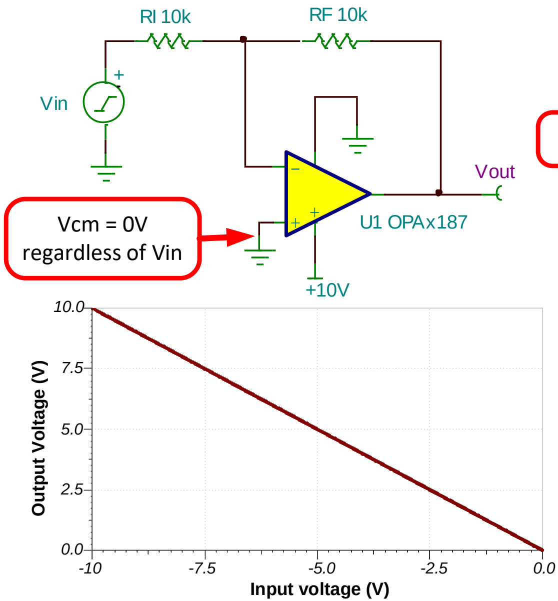
Parameter	Conditions	Min	Typ	Max	Unit
Input voltage range					
Common-mode voltage range V_{CM}		(V-) + 1.5V		(V+)	V
Output					
Voltage output V_{OUT}	I_{OUT} = 50 µA	(V-) + 0.215		(V+) – 0.21	V



V_{CM} versus configuration

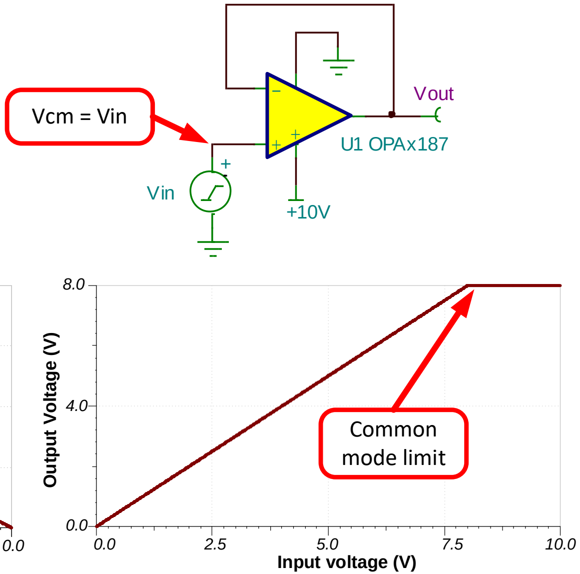
Inverting

(No Common mode limit)



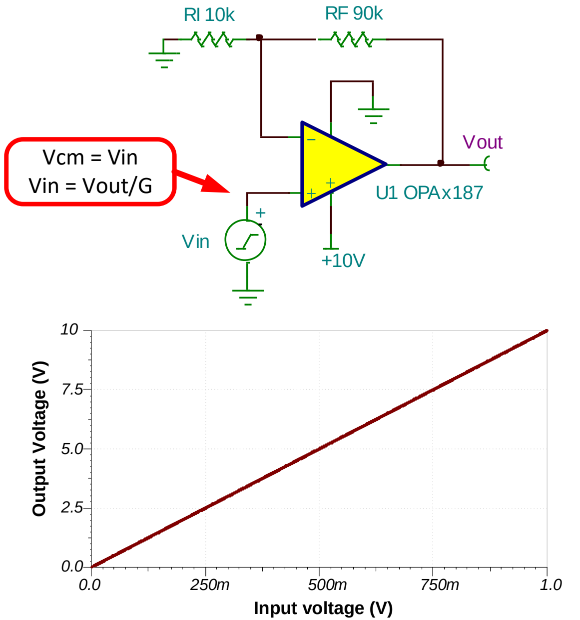
Non inverting low Gain

(be careful of Vcm limit)



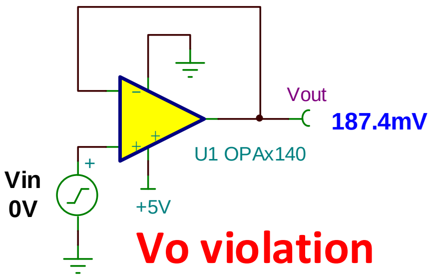
Non inverting high Gain

(may have Vcm limit, but Vin range is small)



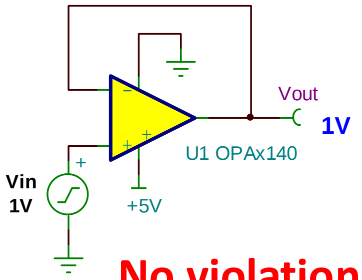
Common Mode Range for OPA187: **-0.1V < Vcm < 8V**, for Vcc = 10V, and Vee = 0V

Common mode and output swing limit examples



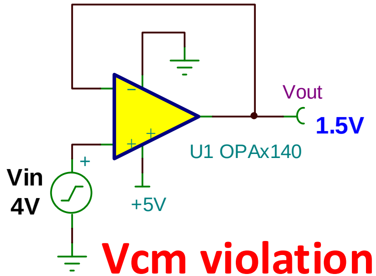
Vo violation

(Vin < 0.2V)



No violation

(Vin & Vout inside both ranges)



Vcm violation

(Vin > 1.5V)

Common Mode Range: **-0.1V < Vcm < 1.5V**, Output Swing: **0.2V < Vo < 4.8V**,

6.7 Electrical characteristics

OPA140		MIN	TYP	MAX	UNITS
V_{CM}	Common mode voltage	(V-) - 0.1		(V+) - 3.5	V
V_O	Voltage output	(V-) + 0.2		(V+) - 0.2	V

Common mode and output swing overview

Op amp	VCM range (min)	VCM range (max)	Output swing from rails, RL =10kΩ (max)	Technology
OPA2391	(V–) – 0.1	(V+) + 0.1	10mV	CMOS, e-trim™, rail-to-rail
OPA863A	(V–) – 0.2	(V+) + 0.2	15mV	High Speed Bipolar, rail-to-rail
OPA810	(V–) – 0.2	(V+) + 0.2	15mV	JFET/CMOS High Speed, rail-to-rail
TLV9062	(V–) – 0.1	(V+) + 0.1	20mV	CMOS, Cost Optimized, rail-to-rail
TLV387	(V–) – 0.2	(V+) + 0.1	30mV	CMOS, Zero-Drift, rail-to-rail
OPA2992	(V–)	(V+)	60mV	CMOS, High voltage, rail-to-rail
TLV07	(V–) – 0.1	(V+) – 2	120mV	CMOS, High voltage, single supply
OPA206	(V–) + 1	(V+) – 1.4	200mV	Bipolar, e-trim™
OPA140	(V–) – 0.1	(V+) – 3.5	200mV	CMOS, Cost Optimized
OPA251	(V–) – 0.2	(V+) – 0.8	250mV	Low power, Bipolar
OPA627	(V–) + 4	(V+) – 4	3.5V	JFET, Precision

Bandwidth limitations

AC error type

Review: gain, linear vs. decibel

Linear (V/V) to decibels (dB)

$$G_{dB} = 20 \times \log_{10}\left(G_{V/_V}\right)$$

Example: Convert closed-loop gain (G_{CL}) of an op amp circuit from 100V/V to decibels

$$G_{CL\,(dB)} = 20 \times \log_{10}\left(100\, {}^{V}/_{V}\right) = 40\, dB$$

Decibels (dB) to linear (V/V)

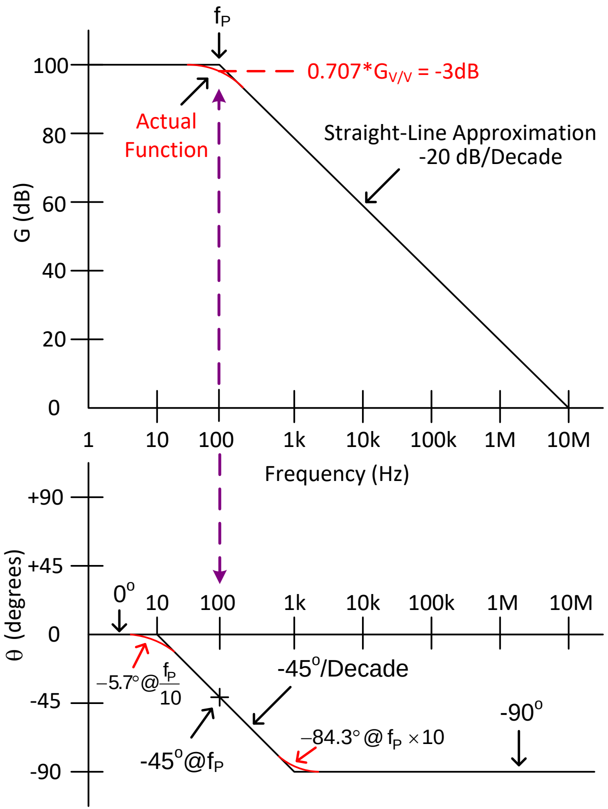
$$G_{V/_V} = 10^{\left(\frac{G_{dB}}{20}\right)}$$

Example: Convert open-loop gain (A_{OL}) range of the OPA828, 140dB to V/V

$$G_{AOL\,@\,1\,Hz} = 10^{\left(\frac{140\,dB}{20}\right)} = 10{,}000{,}000\, {}^{V}/_{V}$$

$$G_{AOL\,@\,14\,MHz} = 10^{\left(\frac{0\,dB}{20}\right)} = 1\, {}^{V}/_{V}$$

Bode plots – pole



$$G_{V/V} = \frac{Vout}{V_{in}} = \frac{G_{DC}}{j\left(\frac{f}{f_p}\right) + 1}$$ As a complex number

$$G_{V/V} = \frac{V_{out}}{V_{in}} = \frac{G_{DC}}{\sqrt{\left(\frac{f}{f_p}\right)^2 + 1}}$$ Magnitude

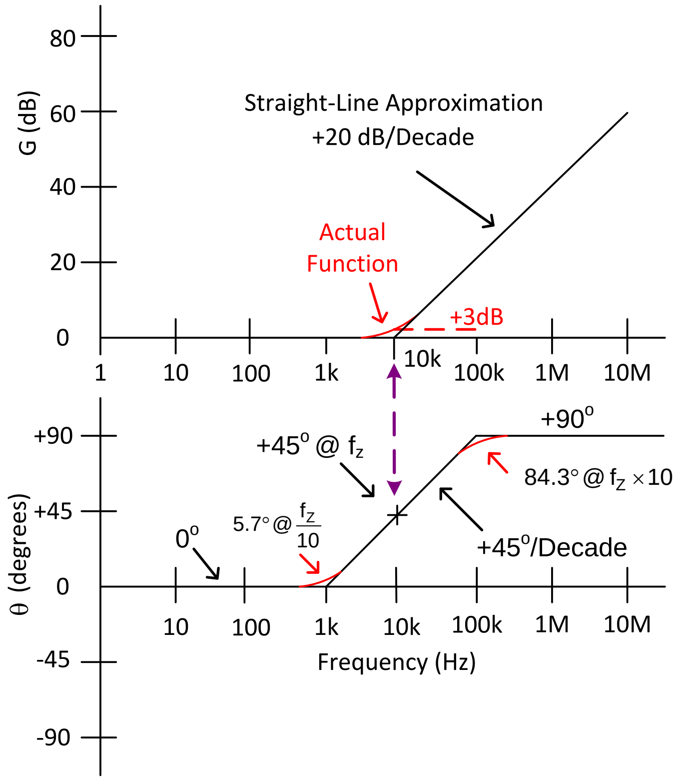
$$\Theta = -\tan^{-1}\left(\frac{f}{f_p}\right)$$ Phase

$$G_{dB} = 20 \times \log_{10}(G_{V/V})$$ Magnitude in dB

Pole location = f_p (cutoff frequency)

	$f \ll f_p$	$f < 0.1f_p$	$f = f_p$	$f > 10f_p$	$f \gg f_p$
Magnitude	G_{DC}	G_{DC}	-3dB	-20dB/dec	-20dB/dec
Phase	0°	-45°/dec	-45°	-45°/dec	-90°

Bode plots – zero



$$G_{V/V} = \frac{Vout}{V_{in}} = G_{DC}\left(\mathrm{i}\left(\frac{f}{f_Z}\right) + 1\right)$$ As a complex number

$$G_{V/V} = \frac{V_{out}}{V_{in}} = G_{DC}\sqrt{\left(\frac{f}{f_p}\right)^2 + 1}$$ Magnitude

$$\Theta = -\tan^{-1}\left(\frac{f}{f_Z}\right)$$ Phase

$$G_{dB} = 20 \times \log_{10}(G_{V/V})$$ Magnitude in dB

Zero location = f_Z

	$f << f_Z$	$f < 0.1f_p$	$f = f_p$	$f > 10f_p$	$f >> f_p$
Magnitude	0dB	0dB	3dB	+20dB/de c	+20dB/dec
Phase	0°	+45°/dec	45°	+45°/dec	90°

Gain bandwidth product

OPAx828

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
GBWP	Gain-bandwidth product			45		MHz
A_{OL}	Open-loop voltage gain	(V–) + 1.6V< VO < (V+) – 1.6V, RL = 600Ω	120	130		dB

$$GBWP = Gain \times BW$$

In this example, for any gain from 0 dB to A_{OL}

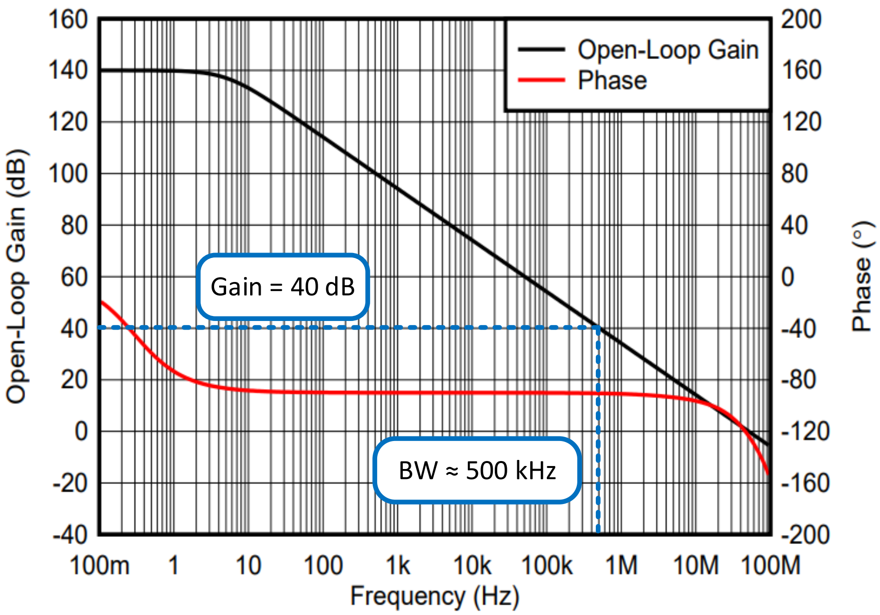
GBWP – gain bandwidth product in Hz
Gain – closed loop voltage gain in V/V
BW – bandwidth in Hz

For example:

$$Gain = 100\,{}^{V}/_{V}\ (G_{dB} = 20 \times \log_{10} 100\,{}^{V}/_{V} = 40dB)$$

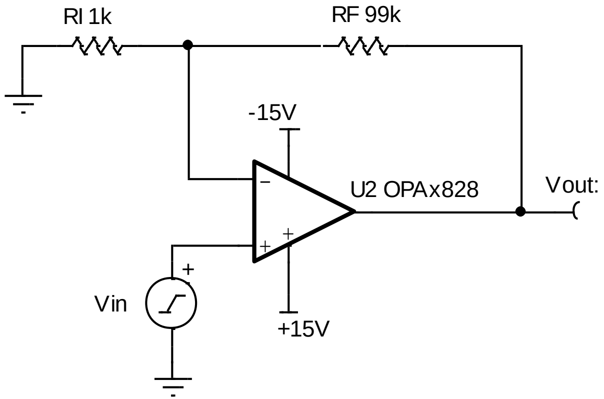
Closed loop bandwidth is calculated:

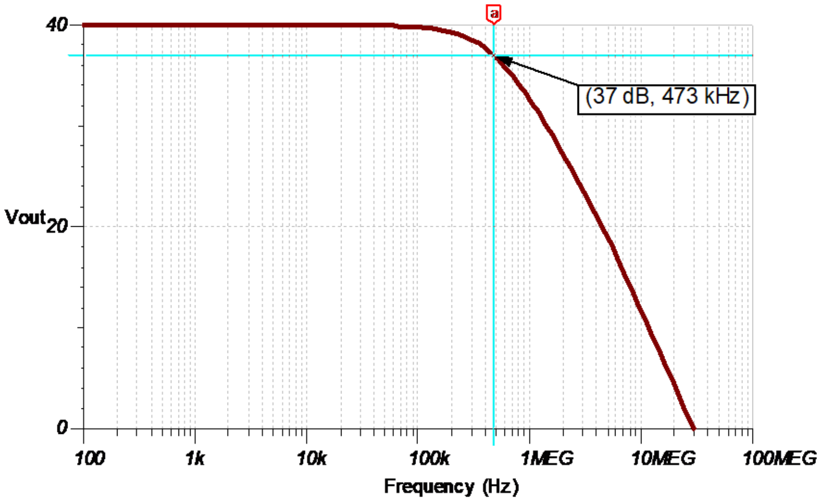
$$BW = \frac{GBWP}{Gain} = \frac{45MHz}{100} = 450kHz$$



TEXAS INSTRUMENTS

Simulation matches calculation





Bandwidth (calculated)	Bandwidth (simulated)
450kHz	473kHz

Bandwidth vs. I_Q

Op amp	GBW (Typ) (MHz)	IQ (Typ) (mA)	Technology
TLV8811	0.006	0.00045	CMOS
OPA379	0.09	0.0029	CMOS
TLV9041	0.35	0.01	CMOS
OPA990	1.1	0.12	CMOS
OPA205	3.6	0.22	Bipolar
TLV9051	5	0.33	CMOS
OPA197	10	1	CMOS
OPA392	13	1.22	CMOS
OPA210	18	2.2	Bipolar
OPA328	40	3.8	CMOS
OPA863	50	0.7	Bipolar

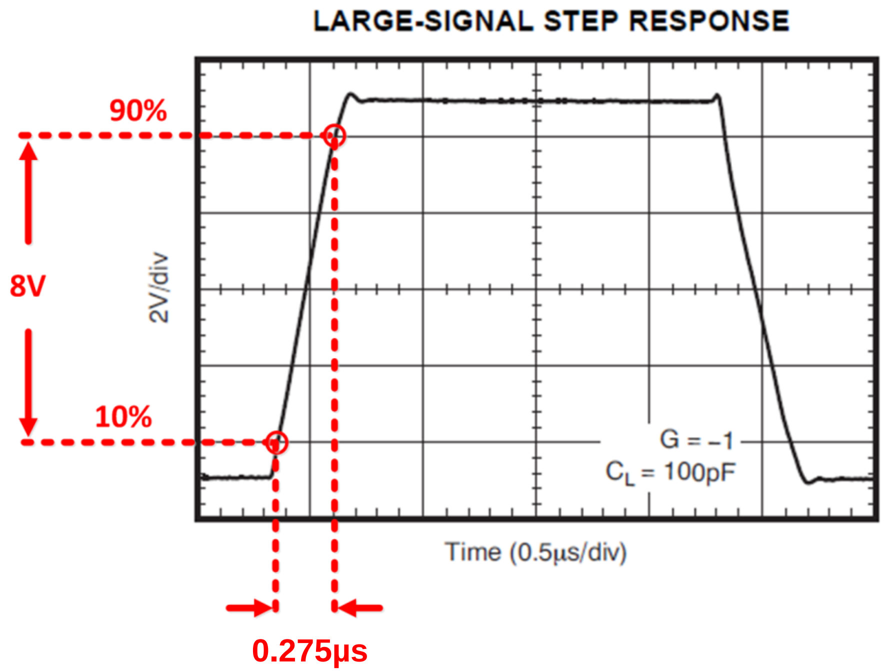
Trade-off (per process): Bandwidth and noise or Iq

Bipolar: $\mathrm{BW} \propto \mathrm{Iq}$ CMOS: $\mathrm{BW} \propto \sqrt{\mathrm{Iq}}$

Slew rate and small signal step response

AC error type

Slew rate defined

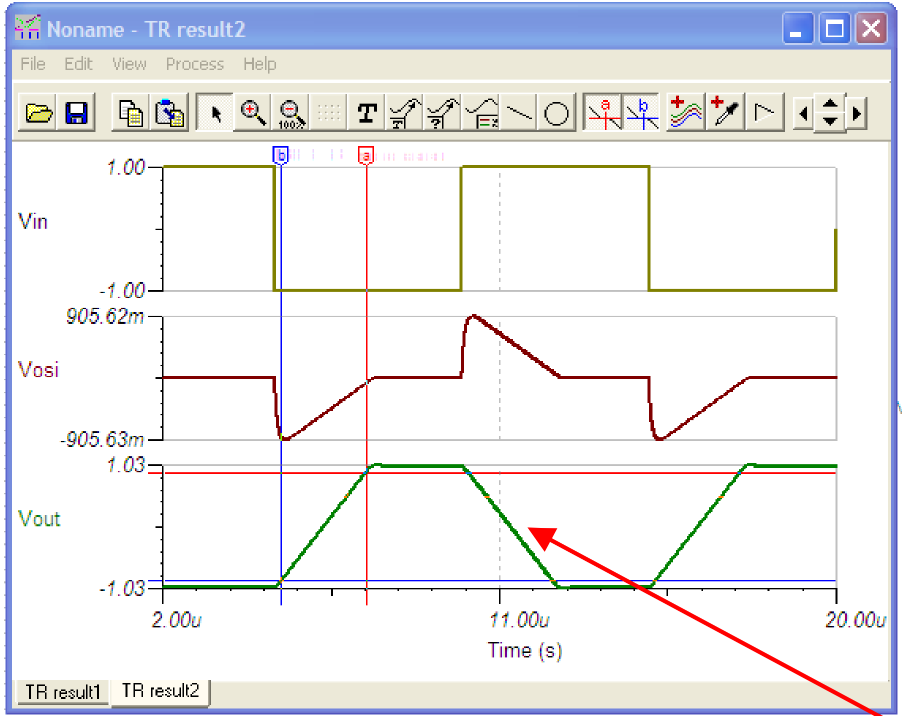


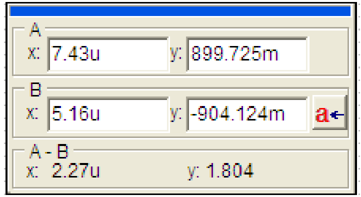
Amplifier in slew limit:

- Output rise maximum rate
- Large signal Vin>100mV
- Output cannot respond linearly to fast input signal
- Input no longer virtual short
- Offset and gain no longer valid

$$Slew_{rate} = \frac{\Delta V_{Out}}{\Delta Time} = \frac{(V_{Out90\%} - V_{Out10\%})}{(t_{90\%} - t_{10\%})} = \frac{(9V - 1V)}{(0.625\mu s - 0.35\mu s)} = 29\ V/\mu s$$

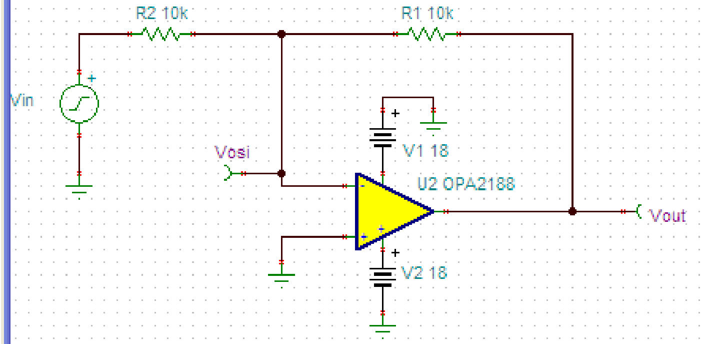
Simulate slew rate – OPA2188





$$SR = \frac{899\text{mV} - (-904\text{mV})}{7.43\mu\text{s} - 5.16\mu\text{s}} = 0.795\frac{\text{V}}{\mu\text{s}}$$

$$SR = 0.8\frac{\text{V}}{\mu\text{S}}$$ From Data Sheet

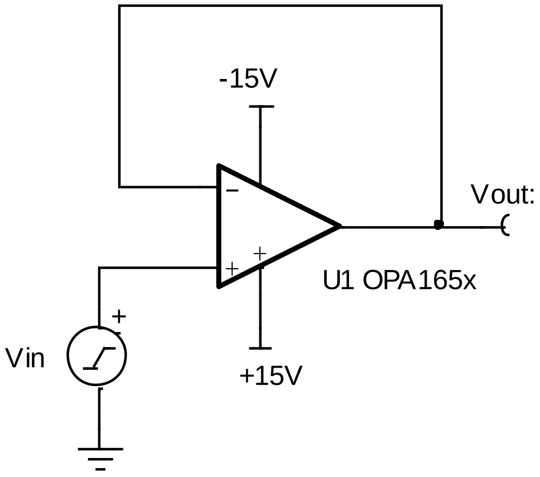


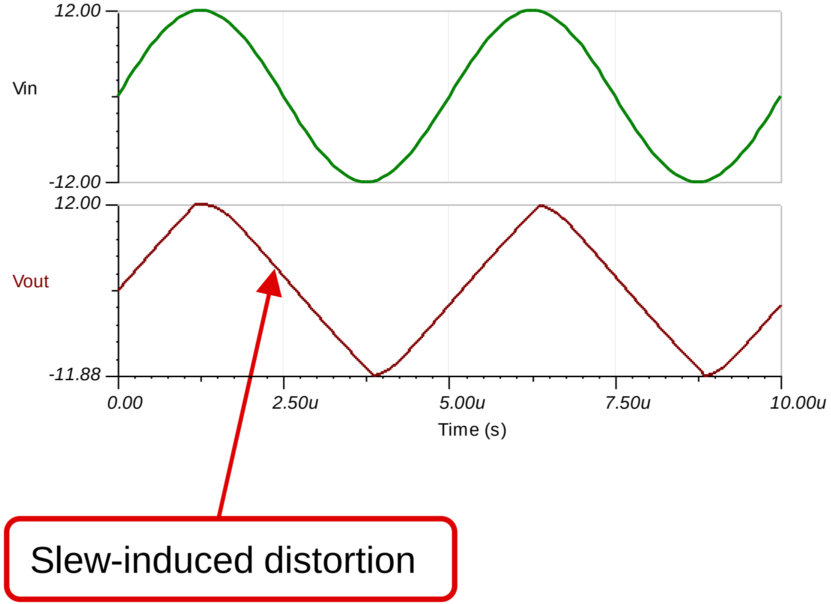
Look at the slope of the output signal. The rate of change is the slew rate.

Slew Rate vs. IQ

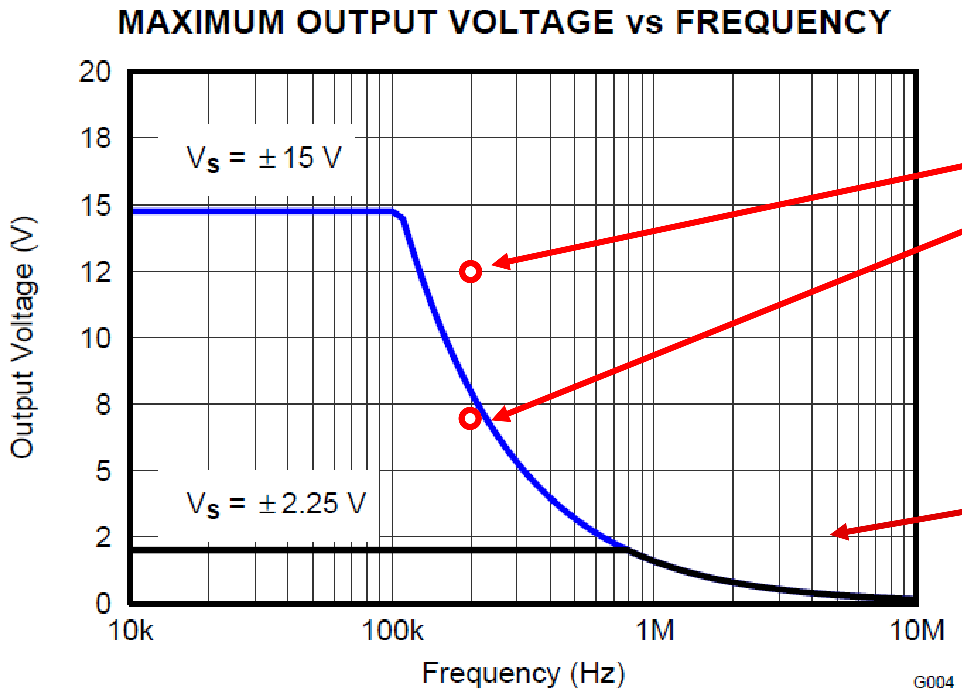
Op amp	Slew Rate (typ)	I_Q (typ)	Technology
TLV8812	0.0015V/µs	0.425µA	
TLV6003	0.025V/µs	1µA	
OPA2186	0.35V/µs	90µA	
TLV9051	15V/µs	0.33mA	Slew Boost
TL071H	20V/µs	0.9mA	Slew Boost
TLV9361	25V/µs	2.6mA	Slew Boost
OPA2328	30V/µs	3.8mA	
OPA994	35V/µs	1.35mA	Slew Boost
OPA593	40V/µs	3.25mA	Slew Boost
OPA863A	100V/µs	0.8mA	
OPA828	150V/µs	5.5mA	Slew Boost
OPA838	350V/µs	0.96mA	Decompensated
OPA830	600V/us	4.25mA	

Effect of slew rate with sine wave input





Full power bandwidth



Example:

For V_S = +/-15V

$12V_{PK}$ → Distortion

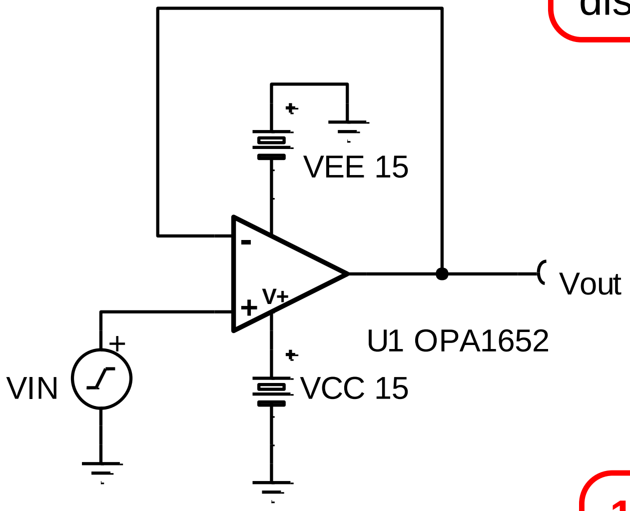
$7.5V_{PK}$ → Low Distortion

Maximum peak sinusoidal signal sr limit low distortion

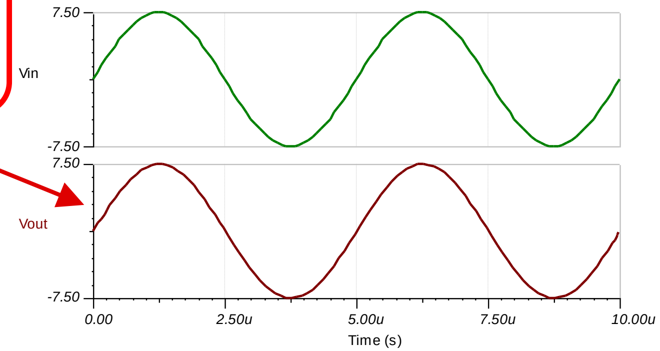
General relationship

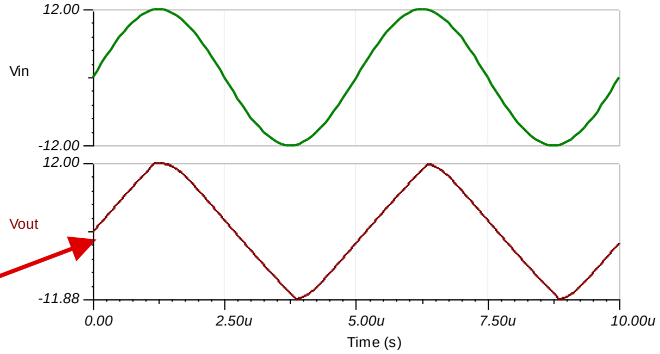
$$V_{pk} = \frac{SR}{2\pi f}$$

Maximum output vs. frequency



$7.5V_{PK}$
No slew-induced distortion



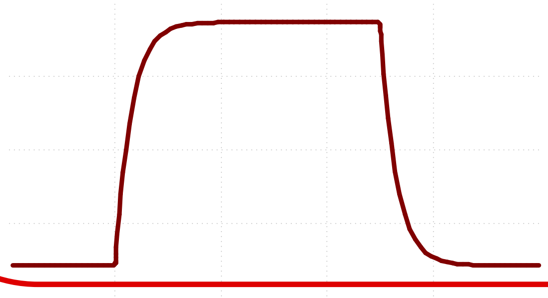


$12V_{PK}$
Slew-induced distortion

Small signal step vs large signal step

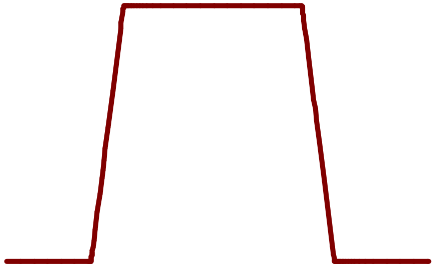
Small signal step

- Input signal < 100mV (approximately)
- Amplifier responds linearly:
  - Gain, and input offset accurate
  - Rise time set by bandwidth
  - $\mathbf{t_R \cong 0.35/f_C}$
- Output signal rises exponentially



Large signal step

- Input signal > 100mV (approximately)
- Amplifier is open loop
  - Gain and offset don't apply
  - Rise time set by slew rate
  - $t_R = \Delta V_{out}/SR$
- Output signal ramps linearly



Small-signal rise time

Rate of change of output:

$\Delta V / \Delta t = 80mV / 70ns$

$\Delta V / \Delta t = 1.1V/\mu s$

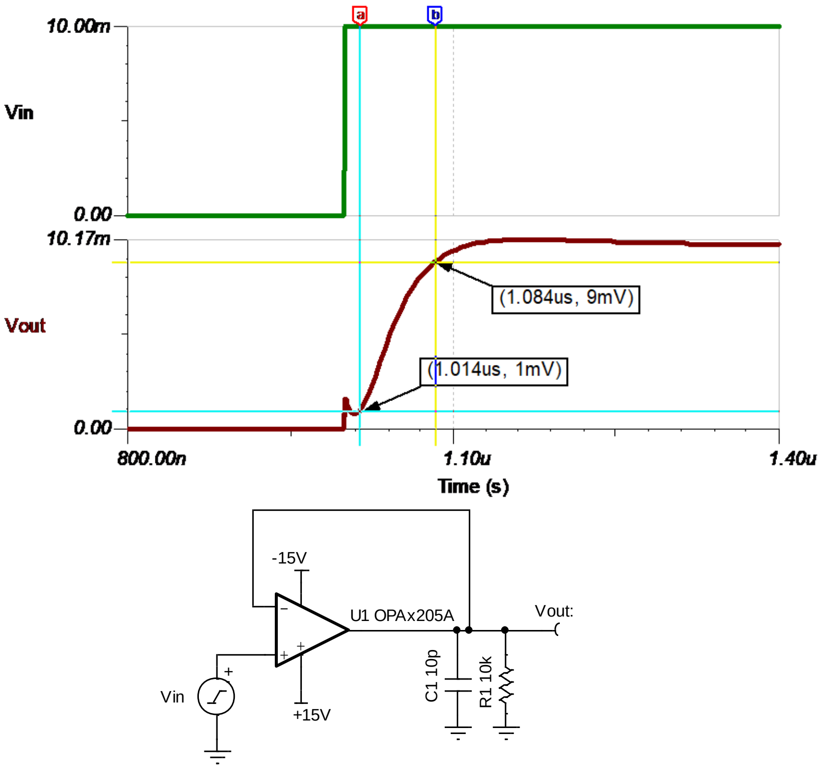
Data sheet SR = 4V/µs
A small signal step will **not** put the amplifier into slew limit.

Small signal equation:

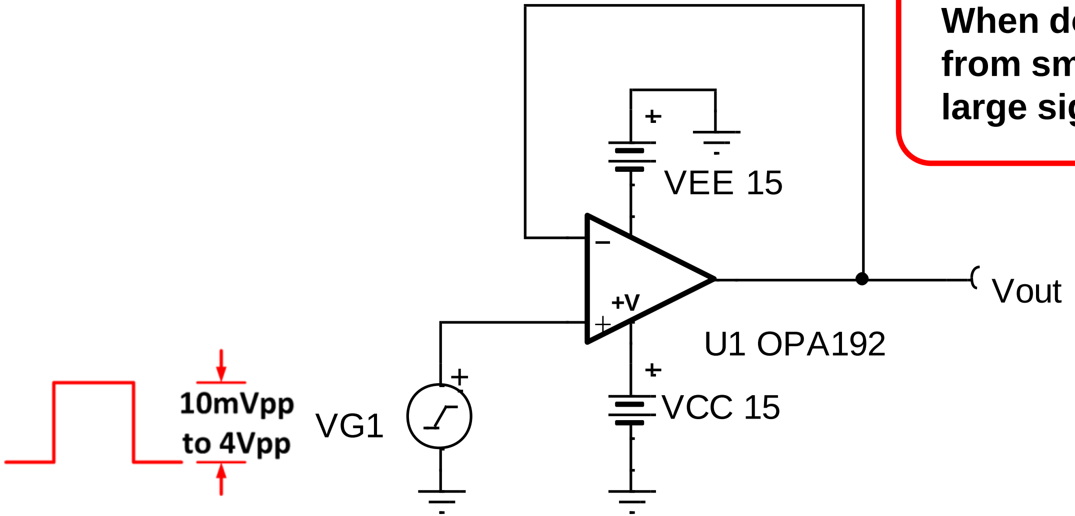
$$f_C = \frac{GBW}{G_{CL}}$$

$$t_R \cong \frac{0.35}{f_C} = \frac{0.35}{3.6MHz} = 97ns$$

Simulated = 70ns



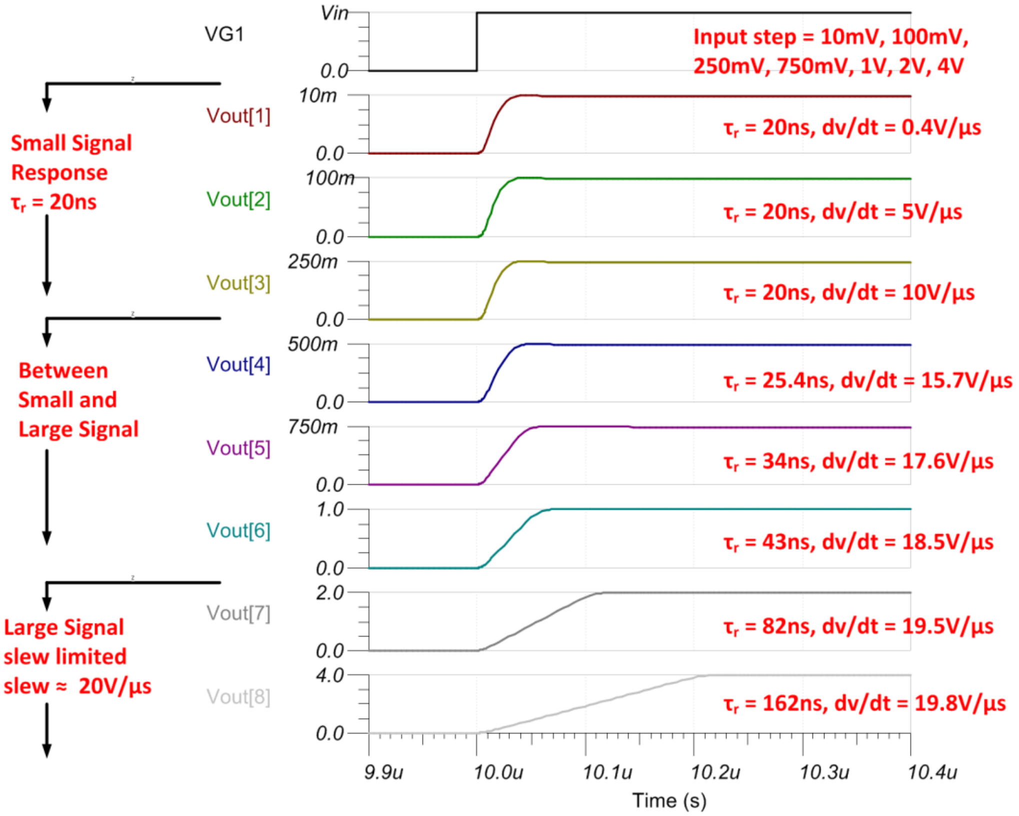
Transition from small-signal to large-signal



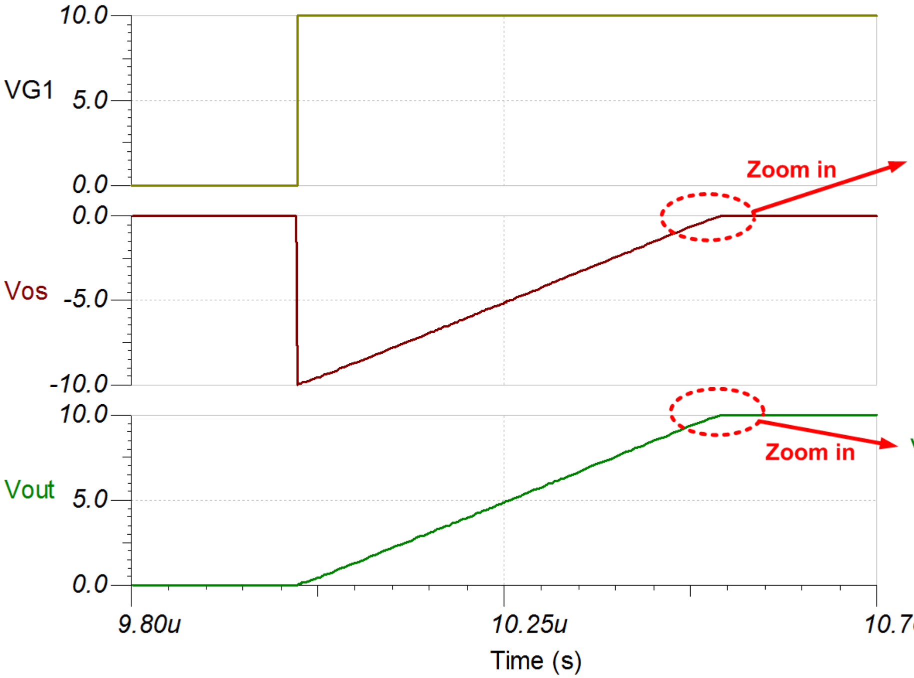
When do we transition from small signal to large signal?

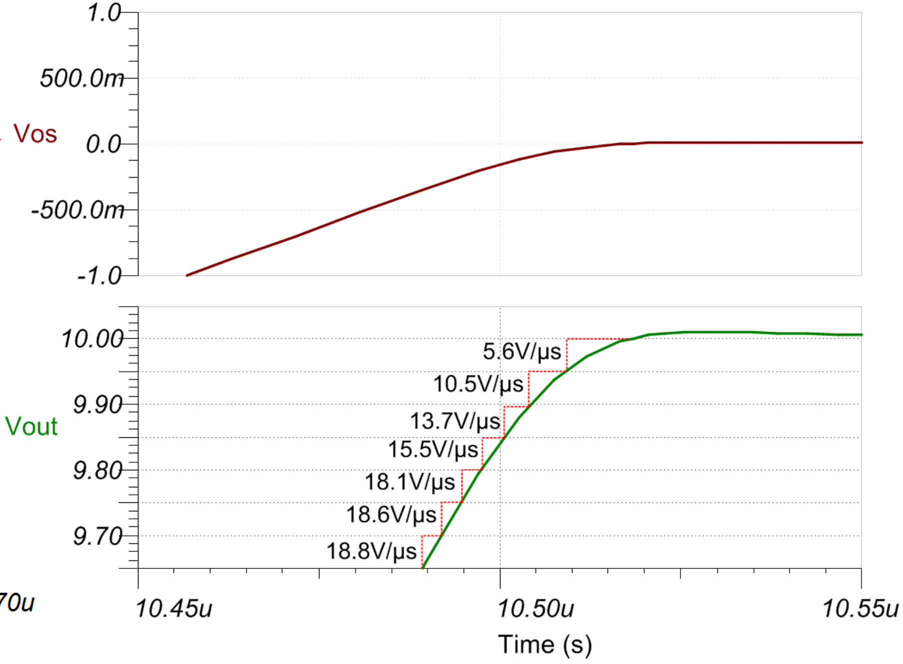
04 - Slew Rate - Large Signal Transition - OPA192.TSC

Transition from small-signal to large-signal

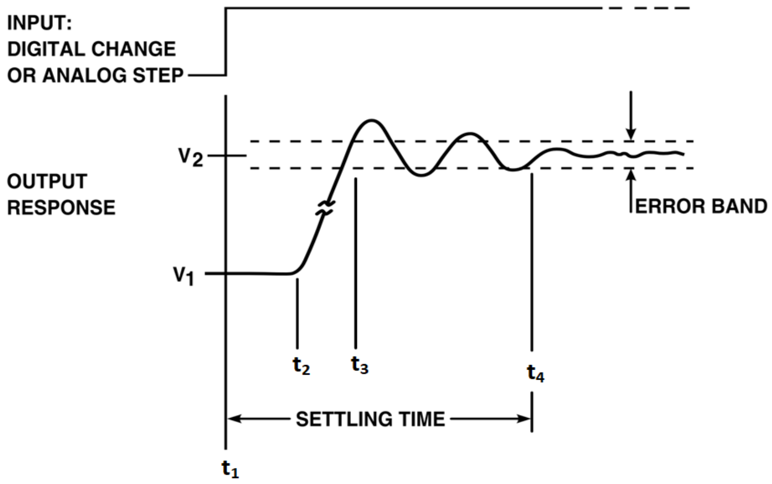


Transition from slew rate to small-signal





Settling time



Large signal settling has three components:

- t1 to t2 is the propagation delay (typically very small)
- t2 to t3 is limited by the slew rate
- t3 to t4 is bandwidth limited

Allowable error band, closed loop gain, and loading also determine settling time

6.5 Electrical Characteristics (continued)

at T_A = 25°C, (V+) = 15 V, (V–) = –15 V, V_{CM} = V_O = midsupply, C_L = 20 pF, and R_L = 2 kΩ connected to midsupply (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SR	Slew rate	V_O = 10-V step	G = +1		150		V/µs
			G = –1		150		

Thank you for your time!