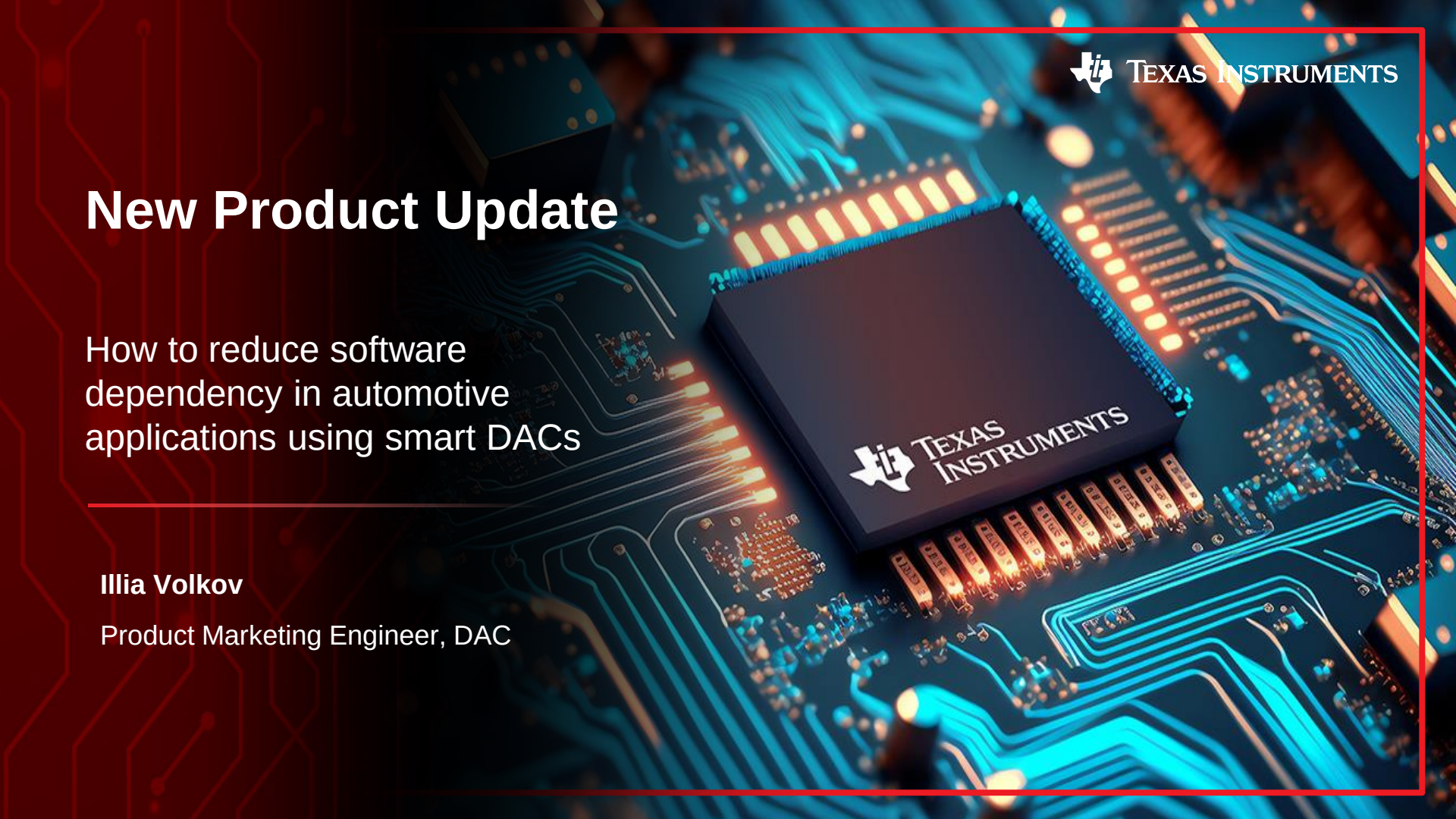
New Product Update

How to reduce software dependency in automotive applications using smart DACs



Illia Volkov

Product Marketing Engineer, DAC

System level

What is DC-link capacitor?

- Positioned in parallel between battery and power stage
- Voltage stabilization
  - Filters voltage ripples and fluctuation
- Energy storage
  - Supplies power during transient conditions or sudden demand changes
- Harmonic filtering
  - Reduction of high-frequency switching produced by the inverter

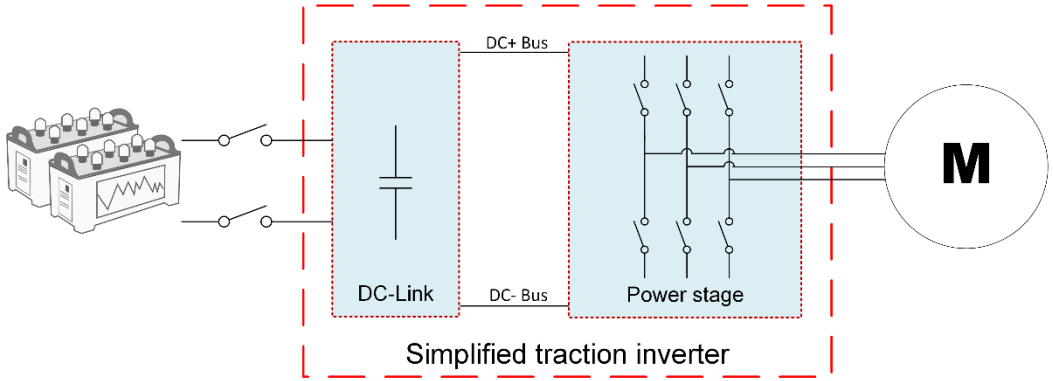
Capacitor requirement

- Max voltage: 1000 V_{DC}
- Cap size: 1mF
- Dissipation time: < 5s
- Safe voltage threshold: 60 V_{DC}

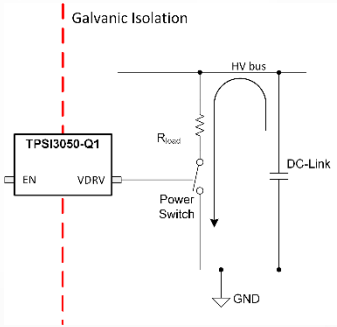
Design problem statement

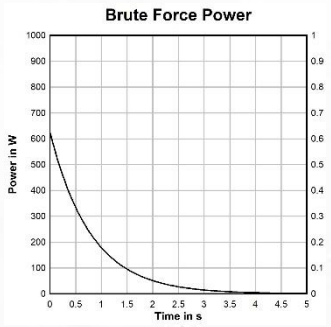
To provide operational safety (post-vehicle collision, maintenance, etc.) DC-link cap must be discharged with-in a **time frame** and usually **independent from software**

Design block diagram



Brute force discharge





- Requires a large power resistor
- No programmability
- Topology could be only used for emergency dissipation due to the resistor power rating

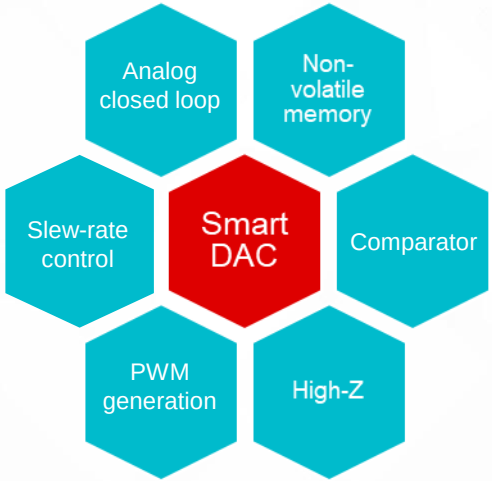
DCC-DAC: Smart DAC and AFE

Smart analog design with no software required

Introduction | Features

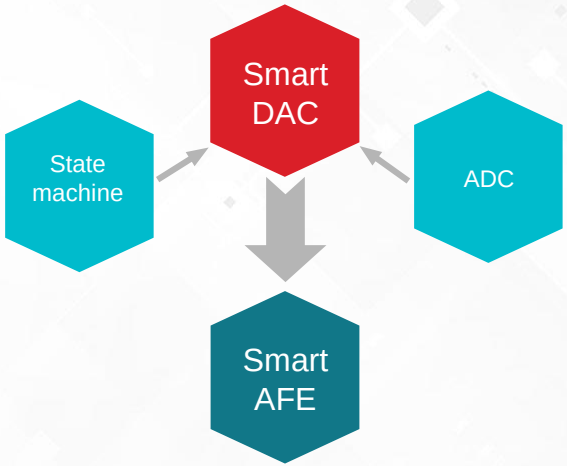
What is a smart DAC?

Reduce software dependency by adding **basic logic** into your analog design through smart DACs



What is a smart AFE?

Smart analog front end (AFE) enables for **real-time closed-loop control** through integrated **state machine** and **sensing capability**

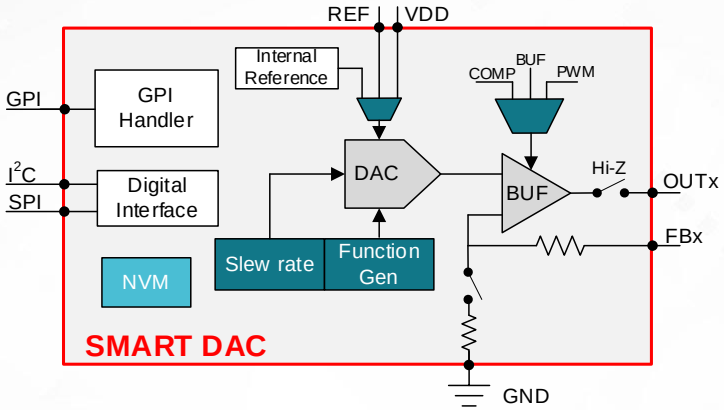


Smart DACs and **Smart AFE**

Reduce software *dependency* by adding hardware *controllability*

Introduction | Block diagram

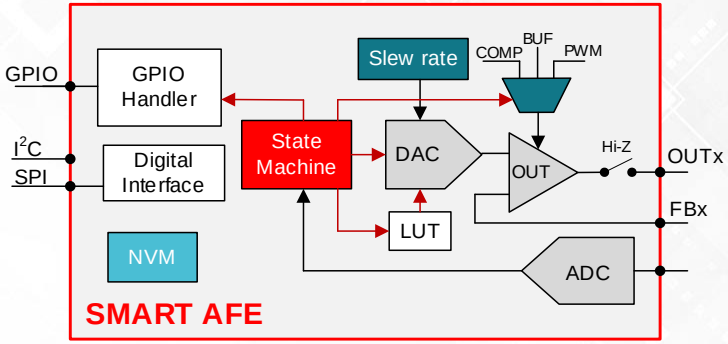
Smart DAC



Features

- **Configurable buffer**:
  - Comparator with hysteresis
  - PWM output
- **Function generation**
  - Sawtooth, triangular, sinusoidal, square
- **GPI trigger**
  - Power down/up, margin high/low trigger, start/stop function generation
- **Reference options**: internal, external, VDD
- **Programmable slew rate control** (DAC ramp-up speed)
- **User programmable non-volatile memory** (NVM) that stores all configurations

Smart AFE

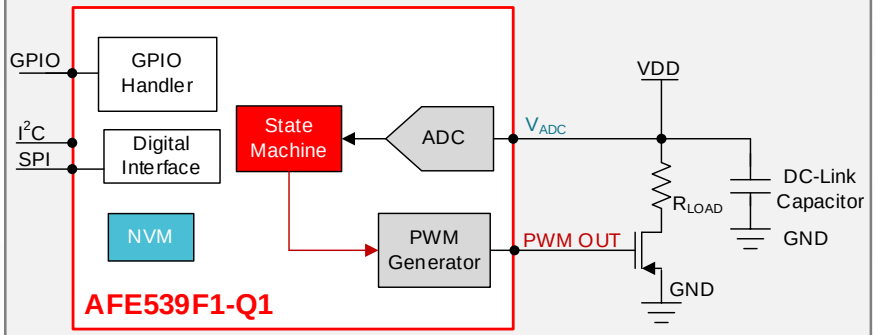


Features

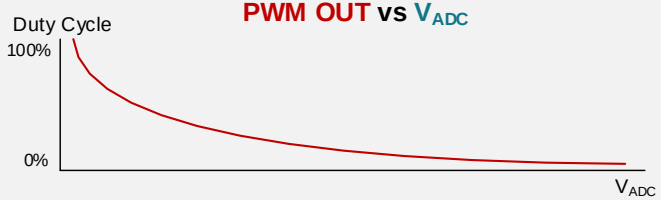
- **All smart DAC features**
- **Programmable state machine**
  - Controls input/output
  - Real-time closed loop control
- **10-bit SAR ADC**
- **Fully configurable look-up table (LUT)**
- **GPIO** with configurable output option
- **User programmable non-volatile memory** (NVM) that stores all configurations

Active discharge | Overview

Block diagram



PWM OUT vs V_{ADC}



Features

AFE539F1 provides a constant power dissipation control across a load independently from the applied voltage. The state machine could be programmed with a transfer function by modifying register values and all of the parameters are stored in the non-volatile memory.

End equipment

- DC-link capacitor discharge
- Control panel
- Heat dissipation control

Benefits

- ADC that monitors the power
- State machine that regulates PWM output
- Configurable transfer function
- NVM that stores all of the configurations for software free operation

Recommended devices	
AFE539F1-Q1	10-bit, 1-ch ADC and PWM

System | AFE539F1-Q1 approach

State machine overview

State machine parameters:

- PWM frequency
- Function coefficient (K)
- Min/max duty cycle

$$D = \frac{K * 2^{15}}{ADC\_DATA^2}$$

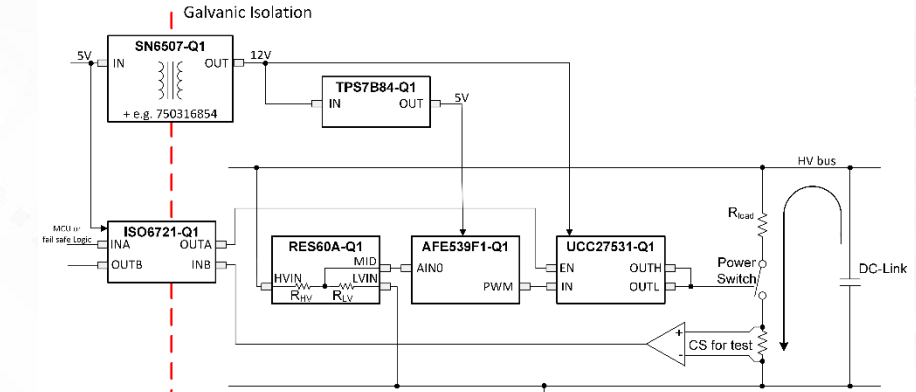
State machine control:

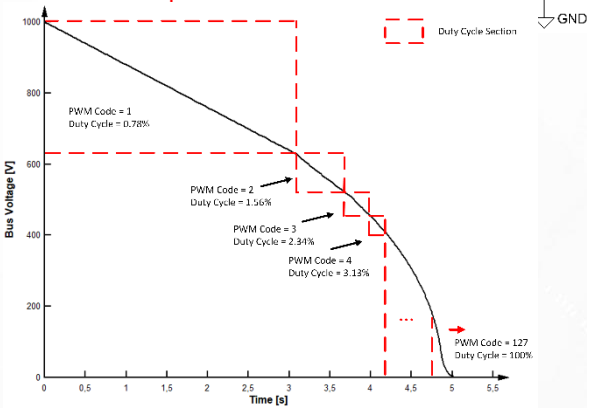
- PWM duty cycle (D)

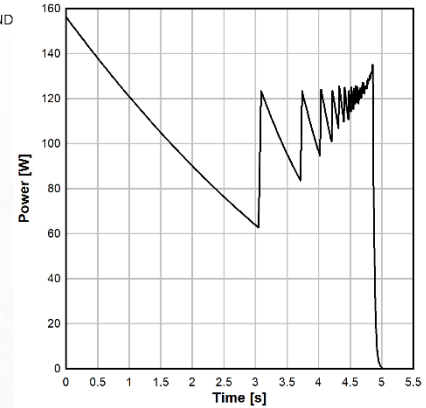
Design benefits

- Smaller load resistor -> lower BOM price by 50%
- Programmability without software
  - Configurable discharge rate and power dissipation rate
  - Discharge control is done independently from MCU

Design block diagram







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